Analysis of Simple Half-Shared Transimpedance Amplifier for Picoampere Biosensor Measurements

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***Abstract*—High-throughput recordings of small current are becoming more common in biosensor applications, including *in vivo* dopamine measurements, single-cell electrophysiology, photoplethysmography, pulse oximetry, and nanopore recordings. Thus, a highly scalable transimpedance amplifier design is in demand. Half-shared amplifier design is one way to improve the scalability by sharing the non-inverting side of the operational amplifier design for many inverting halves. This method reduces silicon area and power by nearly half compared to using independent operational amplifiers. In this paper, we analyze the scalability of a simple half-shared amplifier structure while investigating the tradeoff of increasing the number of inverting half amplifiers sharing a single non-inverting half. A transimpedance amplifier is designed using the half-shared structure to minimize the size per amplifier. The transimpedance amplifier is based on a current integration of a capacitor. The noise analysis of the integration amplifier is a challenging task because it does not reach a steady-state, thus, being a non-stationary circuit. For frequency analysis, a conversion method is discussed to estimate the noise characteristic in the simulation. The array design of 1024 transimpedance amplifiers is fabricated using a standard 0.35 μm process and is tested to confirm the validity of above analysis. The amplifier array exhibits high linearity in transimpedance gain (7.00 mV/pA for high gain and 0.86 mV/pA for low gain), low mismatch of 1.65 mV across the entire 1024 amplifier array, and extremely low noise. The technique will be crucial in enabling the fabrication of larger arrays to enable higher throughput measurement tools for biosensor applications.**

***Index Terms*—Amperometric sensors, biosensors, CMOS analog integrated circuits, electrophysiology, operational amplifiers.**

I. Introduction

A TRANSIMPEDANCE amplifier (TIA) is used in bioelectronic systems to measure currents in biological applications, including *in vivo* and *ex vivo* dopamine measurements [1]–[3], single-cell amperometry [4]–[8], photoplethysmography (PPG) [9]–[11], pulse oximetry [12], and nanopore recordings [13], [14]. They traditionally consist of a circuit to transform the current into the electrode into a voltage measurement. To implement a TIA, most low-noise measurements use an operational amplifier (OPA) to hold an electrode or a photodiode at a reference voltage while converting the current at the electrode or photodiode into voltage, thus forming a transimpedance amplifier. As such, TIAs on integrated CMOS devices usually contain OPAs within them. For high-throughput (large-scale) measurements from an array of detectors, a larger number of amplifiers is required. Thus, it is crucial to minimize the size requirements of each TIA if a larger scale recording is desired. One approach for minimization of TIAs is the half-shared structure of the OPA, which is explored and analyzed in this paper. The approach is powerful, as it enables the doubling of amplifiers on a single chip, increasing throughput for demanding applications. However, few in the field have been using the technique for their designs, possibly due to a lack of awareness and analysis of the concept which will be addressed by this paper.

The half-shared design has been successfully adapted in previous studies to yield large-scale recordings, ranging from tens to thousands of amplifiers [4], [7], [8], [15]–[17]. The design principle of a half-shared OPA is to allow for the non-inverting half to be shared between multiple OPAs, reducing the required die area for multiple OPAs by nearly a factor of two. In an effort to have high bandwidth and a wide dynamic range, a folded-cascode architecture was used for the early half-shared amplifiers [4]. This folded-cascode architecture achieves wide dynamic range and bandwidth at the cost of high power (nearly double) and area consumption. However, if used for most electrophysiology or photodiode applications, the required bandwidth is small ($<$ 20 kHz). Additionally, many CMOS detector arrays for biomedical applications operate below 20 kHz, usually in the 10 kHz region [15], [18]. This low bandwidth can be easily obtained with a traditional five transistor (5T) OPA, further eliminating significant benefits to the folded-cascode architecture. Thus, the 5T OPA design is adapted in this work to minimize the power and area consumption.

The half-shared structure has been analyzed in the past for a limited amount of scalability, usually, two OPAs sharing one non-inverting half [4], [19]. In this paper, we will expand the analysis for an unspecified number of sharing branches to evaluate the effect and implications for larger scale recordings (Section II.). Using the half-shared design, an integration-based TIA is designed and tested. The noise analysis of non-stationary circuits, such as an integration amplifier, is a challenging task. This is because most noise simulations assume a steady-state in the time-domain for the frequency-domain analysis. In order to evaluate the noise characteristics of non-stationary TIAs, we

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produced a simple approach to convert the integration amplifier to a stationary circuit for the noise analysis and applied post-signal-processing to simulate the non-stationary effect (Section III.). To study the 5T half-shared OPA structure, a CMOS chip [7] was designed and fabricated using a 0.35 μm 4M2P process. Since the techniques described in this paper are valid for all process nodes, a 0.35 μm process was chosen as a cost-effective means to fabricate this proof-of-concept work. These techniques can be implemented on any modern analog CMOS process to further reduce die area required for large arrays. In biological applications, the voltage required to monitor or stimulate the electrophysiological processes is often larger than few volts and the larger dynamic range of large process nodes, such as 0.18 and 0.35 μm, is useful. Section II discusses the design of the TIAs, OPAs, and array in detail. In short, the CMOS chip consists of a total of 1024 array elements arranged into a 32 $\times$ 32 grid. The TIAs within each array element are based on OPAs utilizing the half-shared design and have additional circuitry allowing for reconfiguration for testing and different modes of operation. Although each TIA relies on the half-shared OPA architecture, they are effectively independent from the others, allowing 1024 parallel measurements. The fabricated circuit is used to characterize the performance of the half-shared design, including gain, linearity, noise, mismatch, bandwidth, and crosstalk (Section IV.).

II. Transimpedance Amplifier Array Design

The half-shared OPA design is described within this section along with how they are used within the TIAs and array elements and the overall structure of the array. The TIAs used rely on a rather simple design of OPA. Although rudimentary, the 5T OPA's lend themselves well to half-sharing, use low power, require little die area, and their performance within the presented TIA design is sufficient as will be demonstrated in sections III and IV.

A. Half-Shared Amplifier Design

The enabling feature of this array's high density is the half-shared architecture used for the OPAs within the TIAs. The basis of the half-shared design exploits redundancies that occur when traditional 5T OPAs in the negative feedback configuration are used in parallel, and their non-inverting inputs share the same voltage. A half-shared OPA schematic is presented in Fig. 1. Here, M_0 and M_1 form a differential pair, where $M_{\rm bias}$ provides a bias current, and M_{L0} and M_{L1} form a current mirror load for the differential pair. The non-inverting and inverting inputs are the gates of M_0 and M_1, respectively. The output is taken at the drains of M_{L1} and M_1.

Usually, if a second 5T OPA is added, five additional transistors would be required. However, if the bias current and the non-inverting input voltage are the same for the two OPAs, the only two additional transistors are required. This is due to the redundancy within the non-inverting half. Thus M_{L0} and M_0 can be shared between the two OPAs. In this example, M_{L2} and M_2 are all that is required to add a second OPA. For the second OPA, M_2 and M_0 form the differential pair where M_2's gate is the second inverting input. Conceptually, this method can be extended to any amount of additional OPAs.

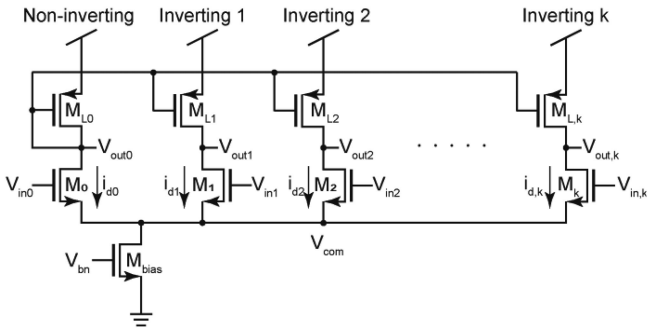

Fig. 1. A half-shared design with k-counts of inverting amplifier shared a single non-inverting half. Transistors M_0 and M_{L0} form the non-inverting half and M_1-M_k, M_{L1}-$M_{L,k}$ form inverting halves of additional OPAs. All NMOS and PMOS bulk connections are to ground and V_{DD} respectively.

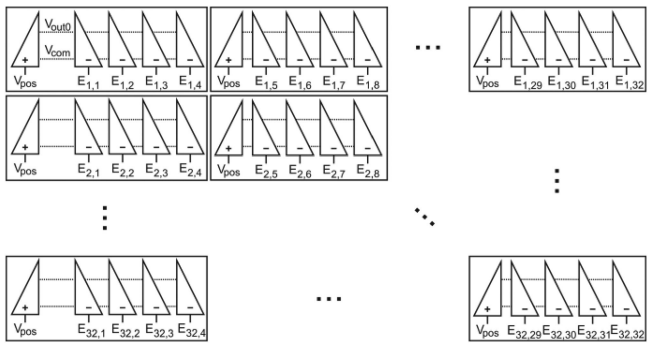

Fig. 2. Block diagram of the CMOS design containing 1024 half-shared amplifier array elements. Each block consists of a group of four amplifiers using the half-shared architecture to save silicon area while increasing the number of on-chip amplifiers. Each OPA is represented as cut in half, with the right half being the inverting side located within a corresponding TIA, and the left half being the non-inverting half common to each block of four amplifiers. The array is eight groups of four amplifiers wide and 32 rows tall to create a total of 1024 amplifiers. Each inverting inputs are labeled with its *row*- and *column*-coordinate position as their indices.

B. Analysis of Half-Shared Structure

The circuit in Fig. 2 shows multiple inverting half amplifiers sharing a single non-inverting half. To examine the tradeoff of multiple inverting halves sharing a single non-inverting half, the small signal gain of each branch is analyzed. The purpose of this analysis is to evaluate the performance of the half-shared structures before it is placed and used as a part of our TIA. The current in the non-inverting half can be expressed:

$$i_{d0} = g_{m0}\left(v_{in0} - v_{com}\right) \tag{1}$$

where g_{m0} is the transconductance of M_0.

Assuming the transconductances of M_0, M_1, M_2, and M_k are equal, currents in inverting halves can be generally expressed:

$$i_{d,k} = g_m\left(v_{in,k} - v_{com}\right). \tag{2}$$

where *k* is the *k*th inverting half amplifier sharing the common non-inverting half. Because $M_{\rm bias}$ supplies constant current for

biasing, it is removed from the small signal circuit, thus

$$i_{d0} + i_{d1} + i_{d2} + \cdots + i_{d,k} = \sum_{n=0}^{k} i_{d,n} = 0. \tag{3}$$

From Eqs. (1), (2) and (3), we can establish V_{com}:

$$V_{com} = \frac{\sum_{n=0}^{k} v_{in,n}}{k+1}. \tag{4}$$

Load transistors, M_{L0}, M_{L1}, M_{L2}, and $M_{L,k}$, form a current mirror and thus currents through these transistors are equal.

$$i_{L0} = i_{L1} = i_{L2} = i_{L,k} = i_{d0}. \tag{5}$$

The current entering the node V_{out1} is

$$i_{out,1} = i_{L0} - i_{d1} = i_{d0} - i_{d1}, \tag{6}$$

and this current used to generalize other halves' output current,

$$i_{out,k} = i_{d0} - i_{d,k}. \tag{7}$$

Because $v_{out,k}$ is loaded by the output resistance of $M_{L,k}$ and M_k, $r_{L,k}$ and r_k, $v_{out,k}$ can expressed:

$$v_{out,k} = (r_{L,k} // r_k) \cdot i_{out,k}. \tag{8}$$

Using Eqs. (2), (3), (4), and (7),

$$\begin{aligned} v_{out,k} &= -(r_{L,k} // r_k) \cdot \left(\sum_{n=1}^{k} i_{d,n} + i_{d,k} \right) \\ &= -g_m \cdot (r_{L,k} // r_k) \\ &\quad \cdot \left[\left(\sum_{n=1}^{k} v_{in,n} \right) + v_{in,k} - (k+1) \cdot v_{com} \right] \\ &= -g_m \cdot (r_{L,k} // r_k) \\ &\quad \cdot \left[\left(\sum_{n=1}^{k} v_{in,n} \right) + v_{in,k} - \left(\sum_{n=0}^{k} v_{in,n} \right) \right] \\ &= -g_m \cdot (r_{L,k} // r_k) \cdot (v_{in,k} - v_{in0}). \end{aligned} \tag{9}$$

In Eq. (9), we can see that the output ($v_{out,k}$) of a particular inverting half is only dependent on $v_{in,k}$ and v_{in0}, not related to other inverting halves' inputs. Thus, multiple inverting halves can operate independently without suffering crosstalk. This analysis also reveals that there is no obvious limit on how many inverting halves can be attached to share a single non-inverting half.

In the half-shared design, the bias current of each amplifier is provided from M_{bias}. Therefore, if the number of inverting half amplifiers increases to share the single non-inverting half, the current level through M_{bias} should linearly increase to supply consistent levels of bias to individual amplifiers. This requires V_{bn} to be elevated. To operate M_{bias} in saturation, V_{com} needs to be increased with V_{bn}, which will limit V_{bn}–V_{com} to be less than the threshold voltage. Thus, one apparent tradeoff of increasing the number of sharing amplifiers is the reduced dynamic range of $V_{in,k}$ and $V_{out,k}$. This effect could be reduced by increasing the width of M_{bias}, however, since the objective of half-sharing is to reduce die area, M_{bias} must be sized as a compromise between size and number of shared branches.

C. Large Array Design Using Half-Shared Structure

The large array of densely packed TIAs consisting of 1024 amplifiers on a single CMOS chip uses the half-shared structure to its advantage. In this case, we chose to have four inverting amplifiers to share one non-inverting half considering the required dynamic range for biomedical applications. For the large array, an important design requirement is that, for this architecture to work properly, transistors M_0, M_1, M_2, M_3, and M_4 must all be matched sizes, as well as load transistors M_{L0}, M_{L1}, M_{L2}, M_{L3}, and M_{L4}. If the sizes are not matched, then the individual half currents will be unequal and Eqs. (5), (6), (7), and ultimately (9) will be invalid. The consequence of poor matching is that the inverting halves will no longer be independent. The arrangement of the TIAs for the large array is shown in Fig. 2. A 32 × 32 grid is used to arrange the 1024 amplifiers as densely as possible. Along any given row, eight half-shared blocks are used where every group of four amplifiers along the row are part of a half-shared block. Using this arrangement of eight half-shared blocks allows 32 TIAs to fit in the same die area that could fit only 17 TIAs using traditional 5T OPAs. This increase in packing density provides an effective method for increasing the throughput of parallel measurements. The V_{pos} terminals of the eight half-shared blocks in each row are connected together and are additionally connected to all 32 rows. This enables a global V_{pos} for setting all 1024 electrode potentials when performing current measurements in electrolytic solutions. Such measurements are the basis for single-cell electrophysiology and amperometry experiments. Each column has its own analog output enabling entire rows of 32 TIAs to be read out simultaneously row after row. While one row is being read out, the other 31 in the same column are performing integration of their electrode currents, enabling a true 1024 simultaneous measurements without deadtime. The detail of the staggered time-division multiplexing is previously described by the authors [8], [16].

D. Programmable TIA

Fig. 3 shows the schematic for one of the 1024 TIAs using the half-shared amplifier. Each TIA contains 11 MOSFETs, a half-shared OPA, an SRAM and two capacitors. The TIA design is based on a regulated cascode amplifier (RCA). The current at the electrode is integrated at the drain node of M_9 which is then measured as a voltage by M_{10} and M_{11}, periodically (t_{int}). Normally, an integrating capacitor (C_{int}) should be placed at the drain node of M_9 which sets the transimpedance gain (G_Z) of the RCA. The gain can be expressed:

$$G_Z = \frac{t_{int}}{C_{int}} \ (V/I). \tag{10}$$

To maximize the transimpedance gain, the parasitic capacitance (<10 fF) which exists at the drain node of M_9 is used. The integrating TIA design achieves similar or better noise

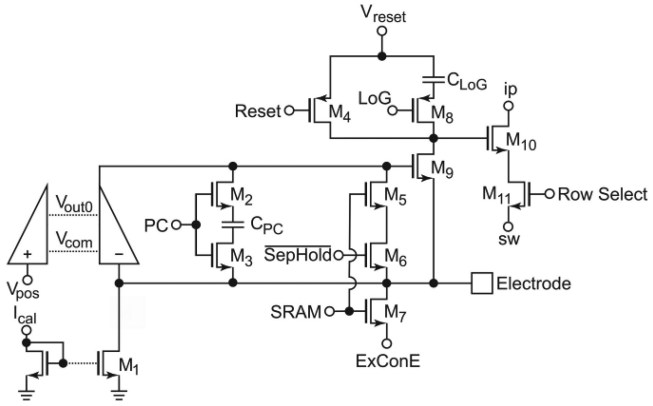

Fig. 3. Schematic of an individual transimpedance amplifier element. The circuit is a reconfigurable and programmable using the embedded SRAM. The design includes the inverting half of an OPA and shares the non-inverting half which is separated so it can be shared with three other amplifiers. Similar to Fig. 1 and Fig. 2, the shared nodes V_{out0} and V_{com} are represented as dashed lines, showing the connections of the half-shared OPA blocks. $V_{out,k}$ is the output of the non-inverting OPA half for this TIA element.

performance compared to a resistive TIA, but with a high area efficiency due to the lack of the resistor. M_1 forms half of a current mirror used to set a calibration current through the TIA via I_{cal}, mainly for testing the transimpedance gain but also to allow the measurement of negative currents. Because we intended to operate the OPA with extremely low power, the phase margin of the RCA can be low with poles from the OPA and M_9 source, closely overlapping. Optional phase compensation can be enabled when PC (phase compensation switch enable) is high by turning on switches, M_2 and M_3 and inserting C_{PC} into the feedback loop, thus increasing the phase margin. The integration capacitance is reset by switch M_4 every integration period (t_{int}). The TIA has two programmable gain settings enabled by C_{LoG}. C_{LoG} can be added to the parasitic integration capacitance by turning on switch M_8 to decrease the gain in low-gain mode by setting LoG low. Thus, in the low-gain mode, the integration capacitance is a summation of C_{LoG} and the parasitic capacitance. The TIA can be connected to an external electrode pad, ExConE, by turning on switch M_7 when the SRAM is set high. An additional function of the SRAM is to use the OPA to be in the unity-gain mode when $\overline{\text{SepHold}}$ and the SRAM are both high. When both M_5 and M_6 are on, the inverting input of the OPA and the output are shorted, enabling unity-gain. Every TIA has a dedicated SRAM within the 900 μm^2 for the fully-addressable programmable array. Switch M_{11} allows for connection to the column's output buffer, where M_{10} is one of the output buffer transistors when Row Select is high. The minimum dimension is used for all switch transistors. For best matching characteristics, analog transistors M_9 and M_{10} are square.

For this array design, each array element is set to be 30 μm $\times$ 30 μm. This is to integrate the entire 1024 amplifier array in less than a 1-mm^2 area. Transistors for the OPAs, M_{bias}, $M_{k,}$ and $M_{L,k}$, are sized at 10 μm $\times$ 10 μm to minimize mismatch. Without the half-shared architecture, the gates of the transistors alone for a single OPA require 500 μm^2 or 55.8% of the 900 μm^2 available for each array element. This would leave insufficient area for the remaining circuitry shown in Fig. 3. However, with the half-shared structure, only 2 OPA transistors must fit into each array element, requiring 200 μm^2 or 22.2% of the array element area, allowing for the addition of the extra circuitry.

III. Noise Analysis of Non-Stationary Circuit

The integration TIA has an integrating node where voltage can swing up to 2 volts within the integration period, which then resets after each integration cycle. Thus, this circuit is non-stationary in the time-domain and the simulation in the frequency-domain is difficult to implement. Thus, in this section, we are exploring a conversion method to estimate the noise performance for a non-stationary circuit using a typical simulation tool.

A. Non-Stationary Circuit

The integrating circuit is only functional if the integration capacitor is periodically reset. Without the periodical reset, the charge in the integration node discharges completely which disables the TIA. Thus, the circuit in Fig. 3 cannot be used for a typical AC/noise analysis. This non-stationary circuit can be converted to a stationary circuit by replacing the integration capacitor to a resistor. The value of the resistor should be:

$$R = G_Z = \frac{t_{int}}{C_{int}} \ (V/I) \tag{11}$$

where the resistance is identical to the transimpedance gain set by the integration period and integration capacitance. The resistor-based circuit is then used for the noise analysis with the noise model provided by the semiconductor manufacturer. The noise measured at the integration node consists of various noise sources from the OPA, cascode transistor (M_9), and the resistor. This analysis does offer some insight into the characteristics of the TIA's noise but fails to capture the effect of the current integration. The current integration for the set duration in a time domain creates a convolution of a rectangular pulse (Fig. 4a).

$$i_{TIA} \ (t) = i_{int}\,(t) * rect\,(t) \tag{12}$$

where the *rect(t)* is the rectangular function (1 for arguments within a window of period t_{int}, and 0 for all arguments outside of the window) and i_{int} is the current measured at the integration node. This expression can be transformed to the following equation:

$$I_{TIA} \ (f) = I_{int}\,(f)\,Y\,(f) \tag{13}$$

where Y(f) is the Fourier transform of the rectangular function. The unitary Fourier transform of *rect(t)* is

$$Y\,(f) = \int_{-\infty}^{\infty} rect\,(t) \cdot e^{-i2\pi ft} dt\,. \tag{14}$$

Thus, the frequency response can be expressed as a *sinc()* function.

$$Y\,(f) = \frac{\sin\,(f \cdot \pi \cdot t_{int})}{f \cdot \pi \cdot t_{int}} = sinc\,(f \cdot \pi \cdot t_{int})\,. \tag{15}$$

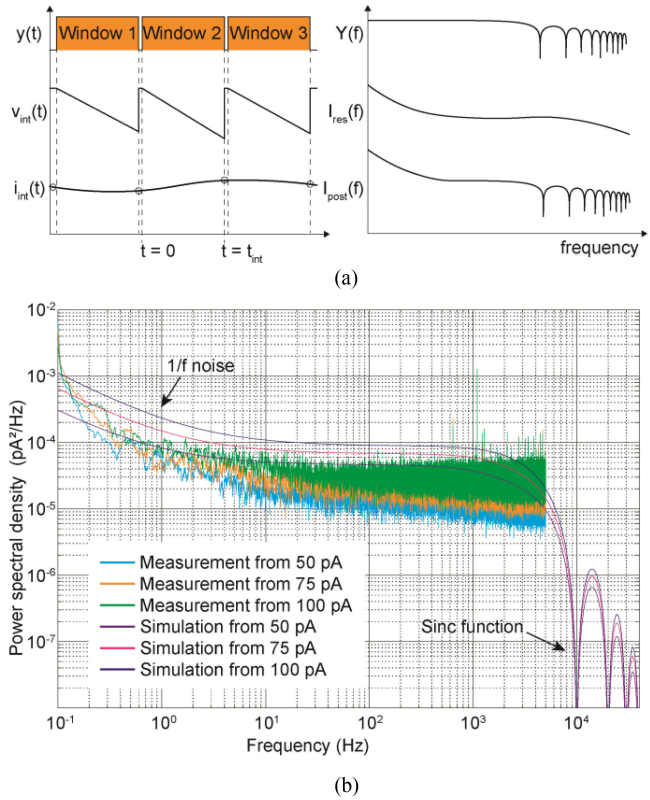

Fig. 4. Characterization of noise using simulation and chip measurement. (a) The current integration creates windows for each integration period and reports the current level at the end of each integration cycle. The window in time-domain generates a *sinc()* function in the frequency domain which can be used to estimate the noise performance in the non-stationary circuit. (b) Noise analysis from the simulation is compared with the chip measurements for various input current levels, 50 pA, 75 pA and 100 pA.

The multiplier, $\pi \cdot t_{\mathrm{int}}$, is to adjust the *sinc()* filter for the specific rectangular function which has the t_{int} window. Any input passing Y(f) with $1/t_{\mathrm{int}}$ interval frequencies should have zero output. To generate the equivalent noise analysis from the stationary circuit to the non-stationary circuit, a post-signal-processing can be applied by multiplying the noise measurement from the simulation with Eq. 15.

$$I_{post}(f) = I_{res}(f)\, Y(f). \tag{16}$$

Therefore, $I_{\mathrm{post}}(f)$ closely estimates $I_{\mathrm{TIA}}(f)$ in Eq. 13. One difference is the thermal noise added by the resistor in the simulation. This effect can be extracted from Eq. 16 if relevant. Since the gain we are simulating is 7.00 mV/pA, the resistor we use is 7 GΩ. The thermal noise of the 7 GΩ resistor is only $\sim 2 \times 10^{-6}$ pA^2/Hz and is significantly smaller than the typical noise in the TIA, so we have ignored it in the analysis.

The simulated noise is shown in Fig. 4b with the measured noise from the CMOS chip at various input current levels, 50 pA, 75 pA, and 100 pA. All noise measurements show 1/f noise at low frequencies. At high frequency, the effect of post-signal-processing of adding *sinc()* response is observed as expected. For all three input current levels, the noise levels between the measurement and the simulation are within a factor of 5, which reveal the discrepancy of the noise characteristic in deep weak inversion. The input current below nano-ampere is considered deep weak inversion and the noise model provided by the manufacturer are generally optimized for strong inversion transistors. Therefore, for any amplifiers operating with pico-ampere current levels, the noise characteristic can be better evaluated by measurements, rather than modeling and simulation. Nonetheless, the simulation method presented here does provide a viable method to estimate the noise level and the frequency characteristics within a factor of 5 before the CMOS fabrication.

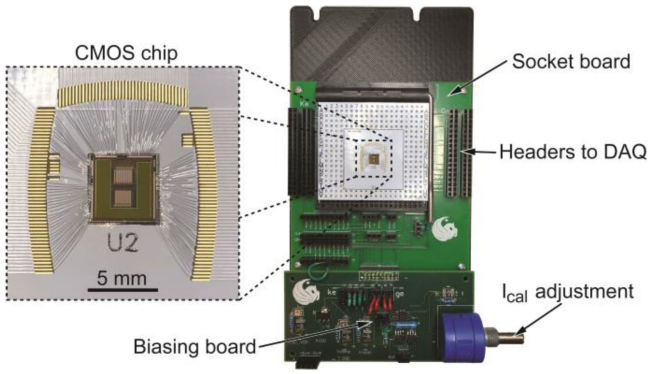

Fig. 5. Overview of the measurement system. The CMOS chip is bonded to a PCB which is inserted into a socket on the socket board. The socket board allows for connections to the National Instruments DAQ unit and to the biasing board. The biasing board converts battery or power supply voltage into V_{DD}, V_{reset}, V_{pos}, and I_{cal}. I_{cal} is easily adjustable via the 10-turn potentiometer.

IV. Characterization and Measurement

To demonstrate the effectiveness of the half-shared architecture, the fabricated CMOS array was used for several experiments using the test setup shown in Fig. 5. This section contains measurements of a representative column's output, transimpedance linearity, amplifier mismatch of the 1024 TIAs, and frequency response.

A. Transimpedance Measurement

The half-shared TIA's transimpedance conversion performance is studied by first configuring the amplifiers to low gain mode, applying a known DC I_{cal} input (from 0 to 1000 pA), and measuring the output waveforms. The array is equipped with multiplexers as previously described in [7], [16] to reduce the number of outputs. 32 TIAs in a column share a 32-to-1 time-division multiplexer. The waveforms resulting from this multiplexed transimpedance measurement are shown in Fig. 6. The separate traces represent the voltage output versus time of a single column's output at a specific I_{cal} level. The square shape of the pulses resulting from the correlated double sampling (CDS) output stage are clearly shown. CDS allows for the removal of the offset produced by V_{reset} by sampling at both the reset and output values and performing a subtraction. The left plot shows the output from a single column measurement (the pulses are the 32 TIAs in that column). The inset plot shows only four rows of the same output, which more clearly shows the linearity of the output voltages for the first four TIAs in the column. The different heights of the pulses indicates a difference in gain of each of the amplifiers. The difference in gain between the amplifiers is likely caused by process variations

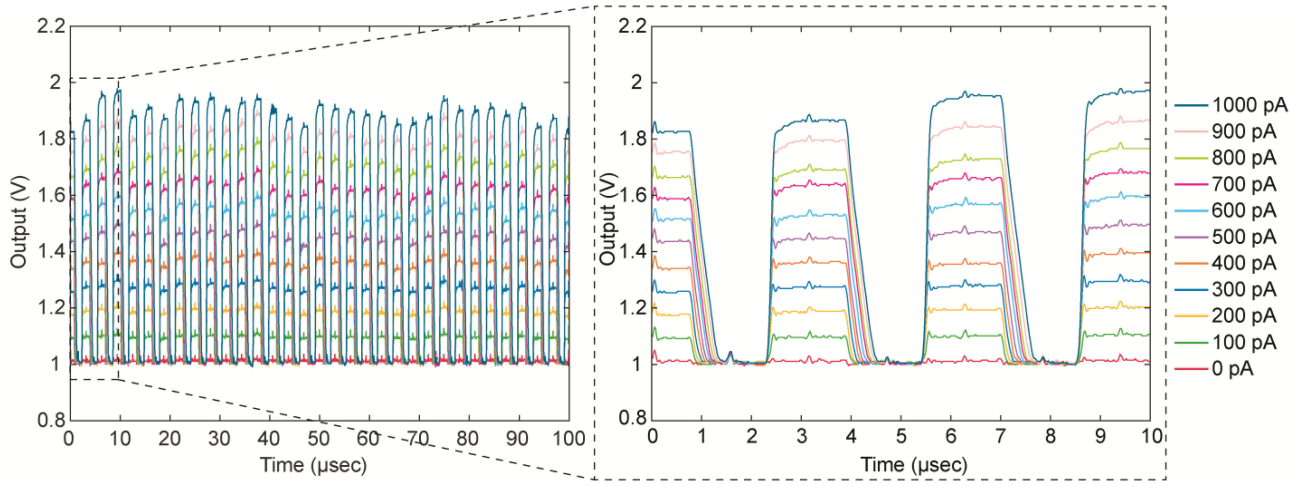

Fig. 6. Chip's output waveforms show a multiplexed output of 32 TIAs for various input current levels into I_{cal} from 0 pA to 1000 pA. Each pulse represents the output of a single TIA.

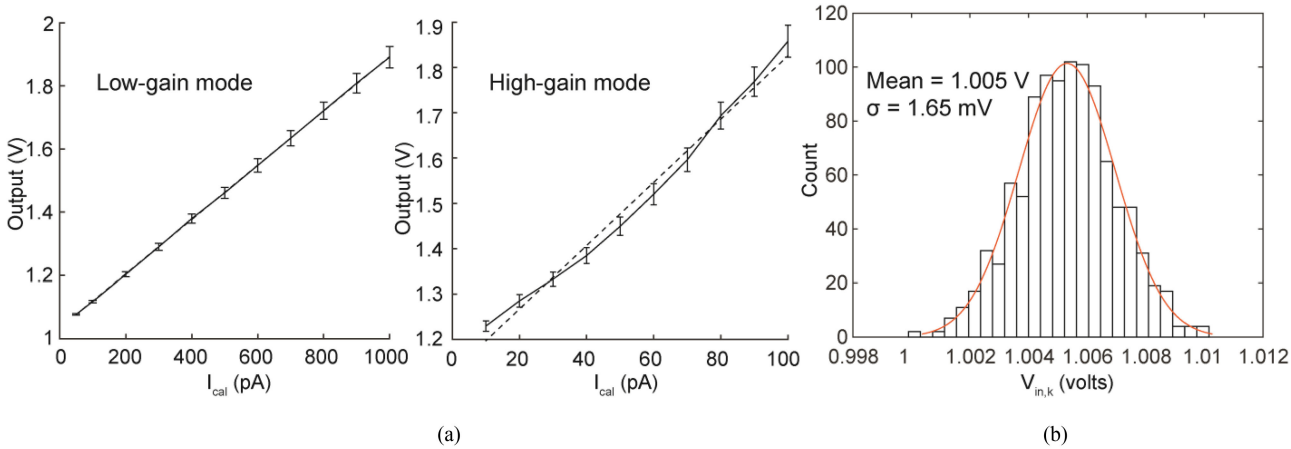

Fig. 7. The current-to-voltage and mismatch characteristics of TIAs. (a) For each input current between 0 pA–1000 pA, TIAs' outputs are plotted for both high-gain mode and low-gain mode. Based on the linear fittings, the transimpedance gains of each mode are 0.86 mV/pA and 7.00 mV/pA, for low-gain and high-gain modes, respectively. Linearity fittings indicate a high-quality linearity. The error bars are used to show the standard deviation of 32 TIAs. The dashed line shows the linear fits. The line's equation is $V_{out} = a + b \cdot I_{cal}$, where a = 1.03 V, b = 0.86 mV/pA for the low-gain mode, and a = 1.13 V, b = 7.00 mV/pA for the high-gain mode. (b) The voltage mismatch of each TIA for the entire array is 1.65 mV, which is a small variation due to the closely-matching transistor size (input transistor and load transistor).

such as the dimensions of the transistors, causing mismatch of the OPA inputs, and the dimensions of the integrating capacitors. Parasitic capacitance variation across the array could also affect the gain, so care must be taken in the layout to ensure that the array elements are identical. It is important to note however, that these variations may vary between array elements but should be consistent within any given array element. As a result, the variations can be calibrated out by applying known signals via I_{cal} and recording the gain of each amplifier before taking measurements.

B. Transimpedance Gain Linearity

The TIA's linearity performance is evaluated by using the data from the transimpedance recording shown in Fig. 6 and creating the voltage versus current plot shown in Fig. 7a. The results from all 32 TIAs' outputs are used to create a least-squares linear fit of V_{out} against I_{cal}. Based on the fit, the transimpedance gain of the low-gain mode is 0.86 mV/pA. The resulting fit has an R^2 value of 0.999, indicating a high-quality linear performance of the TIAs. We have performed the same measurement for the high-gain mode. The transimpedance gain of the high-gain mode is 7.00 mV/pA, and the R^2 value is 0.988. The relatively low coefficient of determination in the linear fitting for the high-gain mode is apparent in Fig. 7a which has a small curvature around 50–60 pA. This is likely due to the nature of parasitic capacitance which is mainly composed of junction and gate capacitors at the integration node. To study the linearity of the entire array, I_{cal} is also measured from all 1024 amplifiers at 700 pA and 200 pA and the gain of each amplifier is calculated. For this measurement, the gain is 0.862 mV/pA with a standard deviation of 0.034 mV/pA.

C. Mismatch

Small differences in transistors' sizes within the OPA can cause a voltage mismatch between the inverting and non-inverting inputs. The mismatch is due to the fabrication process variation. Depending on the application, the inverting inputs control the electrode voltage and accuracy of this voltage can be important. Because the CMOS chip designed in this work features 1024 OPAs, the matching performance is worth evaluating. To test this, the array elements are programmed to unity gain mode and individually connected to the external electrode so that a simple mismatch measurement could be performed. As discussed in Section II. D. and shown in Fig. 3, unity gain mode connects the OPA's output directly to the inverting input. The non-inverting input is held at V_{pos}, and the output voltage is measured at the ExConE. If the OPAs have no mismatch, every OPA will produce exactly V_{pos} at its output.

A custom-made LabVIEW program is used to control a National Instruments data acquisition system automating the SRAM programming and measurement of each individual array element's output as quickly as possible to reduce deviation due to environmental variables such as temperature. Each measurement is used to plot a histogram of output voltage measured at the ExConE (Fig. 7b). The measurement results in a mean output voltage of 1.005 V and a mismatch standard deviation of 1.65 mV for the entire 1024 TIAs. Mainly, the large area investment to $M_{L,k}$ and M_k in each OPA (Fig. 2) contributes to the small deviation.

D. Bandwidth

In operating the TIA design, it is ideal to have the dominant pole of the transimpedance measurement to be determined by the *sinc()* function created by the current integration (discussed in Section III. A.) This can only be achieved if the other poles from the OPA and M_9 (in Fig. 3) are higher than the pole from the *sinc()* function. The pole from the *sinc()* function is a function of the integration window size based on Eq. 15,

$$sinc^2\left(f_{BW}\cdot\pi\cdot t_{int}\right)=\frac{1}{2}. \tag{17}$$

Thus, the pole can be determined based on the following expression,

$$sin\left(f_{BW}\cdot\pi\cdot t_{int}\right)-\frac{1}{2}\cdot f_{BW}\cdot\pi\cdot t_{int}=0. \tag{18}$$

In the case when t_{int} is 100 μs, f_{BW} is ~4.43 kHz. So long as the other poles do not fall below 4.43 kHz, the dominant pole of this TIA design is the pole from the *sinc()* function.

The bandwidth of the half-shared TIA is measured using three different bias currents, 36.8 nA, 45.9 nA, and 55.4 nA, for each TIA. Phase compensation is also enabled. V_{pos} is set to 1 V. A TIA is set to connect to ExConE, and the ExConE terminal is connected through a 1 MΩ resistor to an analog output of a National Instruments data acquisition unit, allowing for the generation of an AC sinusoid current to be applied to the amplifier. Various frequencies are input while the TIA outputs are measured and plotted as shown in Fig. 8. When t_{int} is set to 100 μs, the TIA produces the expected ~4.4 kHz bandwidth as well as the expected $sinc^2()$ aliasing sidelobes caused by the integration period. For all three measurements, no observable difference is shown indicating that for any tested biasing levels, the OPA's pole remains higher than 4.4 kHz.

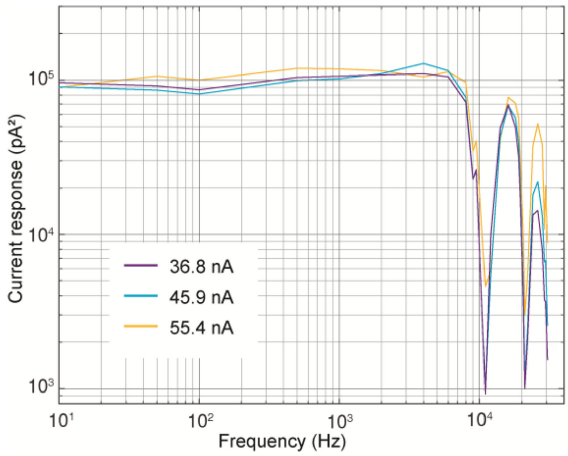

Fig. 8. Frequency response showing the bandwidth of the TIA at different subthreshold biasing levels, 36.8 nA, 45.9 nA, and 55.4 nA. All recordings show near 4.4 kHz bandwidth which is caused by the dominant pole generated by the current integration performed at 10 kHz. This measurement indicates at any given biasing levels, the dominant pole is produced by the *sinc()* function, instead of the pole from the OPA.

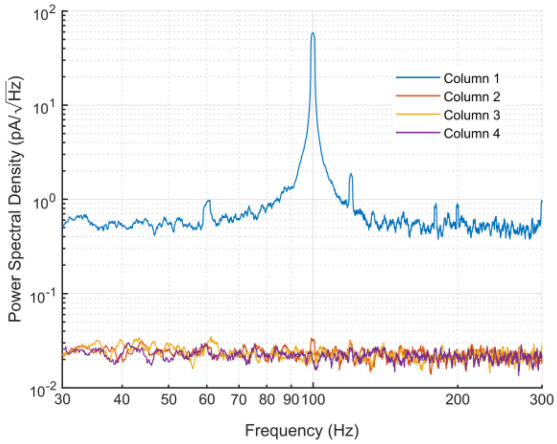

Fig. 9. Measurement of a half-shared block's crosstalk performance. A 100 Hz signal is injected into column 1 via ExConE, the three shared amplifiers show a heavily attenuated signal present at 100 Hz. The rise in noise floor between column 1 and the others is due to the extra capacitance noise caused by connection to ExConE and the wire to the signal generator.

E. Crosstalk

A major concern for the half-sharing concept is crosstalk between shared channels. Although the small signal analysis from section II. B. shows that the design should not suffer from crosstalk, a measurement is presented in Fig. 9. For this measurement, row one columns one through four are measured. A 100 Hz sine wave of 400 μV peak-to-peak is injected into the chip's ExConE through a 1 MΩ resistor to produce a 400 pA peak-to-peak current signal. The row one column one TIA is configured to connect to ExConE so the TIA received this current input. Columns two, three, and four exhibit little to no crosstalk from the 100 Hz signal as demonstrated by Fig. 9. The noise floor discrepancy between the four channels is caused by

TABLE I
COMPARISON TO SIMILAR AMPLIFIER ARRAYS

Reference	[4]	[6]	[15]	[16]	[20]	[21]	**This Work [8]**
Technology Node	0.5 μm	0.18 μm	0.5 μm	0.5 μm	0.18 μm	0.13 μm	**0.35 μm**
Die Size	-	12 mm × 8.9 mm	2.5 mm × 2.5 mm	3 mm × 3 mm	5 mm × 2.65 mm	3 mm × 2 mm	**5 mm × 5 mm**
Number of Electrodes	25	59760	100	100	200	1024	**1024**
Amplifier Size	525 μm^2	≥0.04 mm^2	0.06 mm^2	900 μm^2	0.03 mm^2	8000 μm^2	**90 μm^2**
Simultaneous Channels	25	28	25 (4 to 1 multiplex)	100	200	4	**1024**
Noise performance	~ 110 fA_{RMS}	120 pA_{RMS}	7.2 pA_{RMS}	~ 100 fA_{RMS}	480 fA_{RMS} at 110 Hz filtered	56 pA_{RMS}	**415 fA_{RMS}**
Bandwidth	2 kHz	16 kHz	11.5 kHz	~1 kHz	110 Hz - 10 kHz	700 Hz	**4.4 kHz**
Total Power	-	86 mW	2.1 mW	-	3.21 mW	-	**12.5 mW**

parasitic capacitance being added to the input of the amplifier for column one due to its connection to ExConE and the wire leading to the signal generator.

V. CONCLUSION

In this paper, we are presenting a simple half-shared amplifier structure which can be used for large-scale recordings. Analytical evaluation as well as simulation, and measurement of the fabricated circuit are discussed in detail to show the efficacy of the half-shared design and how it can scale into a large array without a significant trade-off. Many similar arrays require more die area for their amplifiers [4], [6], [15], [16], [20], [21]. Several arrays have increased throughput and reduced die area by using the half-shared architecture [4], [16]. Others have high electrode count, but a low amplifier count, disabling simultaneous full-array measurement [6], [15], [20]. This work builds on previous work and has a high electrode count, with simultaneous full-array measurement, enabled by the half-shared architecture. The performance of the array is compared with other similar arrays in Table I. As discussed in Section II. B., the measurement of each TIA does not suffer from crosstalk because the gain is completely independent (Eq. 9). One notable trade-off is the reduced dynamic range on each inverting inputs, due to the elevated V_{com}. A simulation method is presented which can closely estimate the noise performance of a non-stationary circuit, which has been traditionally difficult to analyze in the frequency domain. The transimpedance gain, mismatch performance, bandwidth, and crosstalk performance are measured from the fabricated circuit to validate the performance. This minimal deviation in mismatch will allow this CMOS device to be useful for most biosensor applications, including single-cell amperometry and nanopore-based nucleic acid measurements. It is interesting to note that, the common-mode rejection ratio (CMRR) of current-measurement amplifiers is not often discussed because the current signal source does not typically carry common-mode signals, in contrast to the voltage sources which almost always have a common-mode signal. However, the implication of the sharing structure to CMRR is worth studying and we are planning on conducting a future research project to investigate the CMRR of a TIA and how it can be quantified in both analytical and experimental settings.

The presented method for reducing die area required for OPAs in TIAs by half-sharing is an effective technique as demonstrated by measurements taken from the fabricated 0.35 μm CMOS chip. A four-way half-shared OPA scheme has proven to enable the miniaturization of 32 TIAs into the same space that would traditionally only be able to fit 17 TIAs, which is nearly 50% area reduction while retaining the similar performance. This enables future chips to be designed with an even higher number of electrodes and amplifiers for high-throughput biomedical measurements.

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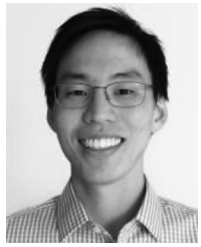

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