Parallel 1024-ch Cyclic Voltammetry on Monolithic CMOS Electrochemical Detector Array

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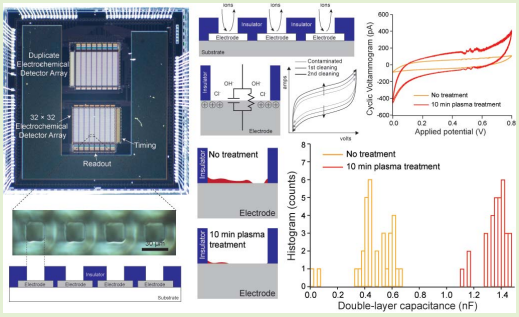
***Abstract*—Large-scale microelectrode arrays offers enhanced spatiotemporal resolution in electrophysiology studies. In this paper, we discuss the design and performance of an electrochemical detector array which is capable of 1024-ch parallel cyclic voltammetry. The electrochemical detector is fabricated using a custom-designed CMOS chip, which integrates both the circuity and on-chip microelectrode array, to operate the array and record electrochemical signals. For parallel 1024-ch recordings, 1024 capacitor-based integrating transimpedance amplifiers are designed. The amplifier design features bipolar capabilities for measuring both negative and positive electrochemical currents due to reduction and oxidation reactions. The cyclic voltammetry functionality was validated by measuring the double-layer capacitance of the on-chip electrode array. Cyclic voltammetry can be used to examine the quality of electrochemical electrodes by measuring the double-layer capacitance that forms at the electrode-electrolyte interface. Double-layer capacitance is a function of the effective area of the electrode. A contaminated electrode can have smaller effective area resulting in smaller double-layer capacitance. Using the parallel cyclic voltammetry capability of the monolithic CMOS device, the double layer capacitance of all 1024 electrodes can be simultaneously measured to examine the status of the electrode array in real time. The initial measurement of the electrode array showed a mean capacitance of 0.47 nF. After plasma treatment to remove contamination on the electrode's surface, the increased capacitance was 1.36 nF nearly tripling the effective surface area. This method can accelerate the characterization of an electrode array before analytical experiments to provide well-controlled electrochemical electrodes, which are crucial in conducting reliable electrochemical measurements.**



***Index Terms*—Bipolar integrated circuits, electrochemical devices, electrochemical sensors, microelectrodes, sensor phenomena and characterization, surface contamination.**

I. Introduction

LARGE-SCALE microelectrode arrays (MEA) offer high spatiotemporal resolution for electrophysiology studies. MEAs have been useful in enhancing the spatial resolution of electrochemical recordings, such as mapping the level of H_2O_2 in relation to neurological diseases in a brain slice [1], electrochemical imaging of redox molecules diffusing across an MEA [2], and imaging of metabolites in biofilms [3]. Large-scale MEA is especially useful in single-cell electrophysiology in which a large number of simultaneous recordings take place in order to account for heterogeneity in the characteristics of quantal release among the cell population [4]. For these reasons, high-throughput simultaneous measurements from a large number of cells would result in a tremendous benefit in enabling rapid studies of neurodegenerative disorders, the effects of therapies as well as new drug discoveries that target neurotransmitter release. Significant cost reduction in the single-cell electrophysiological analysis will also allow the evaluation of emerging treatments for side effects on molecular and cellular levels before it is clinically used.

A large number of electrodes in the MEA must be connected to external electronic amplifiers for signal amplification and processing. The use of external amplifiers becomes prohibitively expensive as the number of simultaneous recordings grows (for single-cell electrophysiology ~$15,000 per amplifier), but more importantly, it sets a limit

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on the total number of electrodes in an array because the external wiring becomes impractical. To resolve this challenge, complementary metal-oxide-silicon (CMOS) chips which monolithically integrate an amplifier for every on-chip electrode can be used. This method drastically lowers the cost per amplifier and removes the need of external wiring because the on-chip electrode and on-chip amplifier establish a connection within the chip. Therefore, the monolithic CMOS-based MEA opens opportunity to increase the electrode count of a MEA to above 1000s. Previously, we have developed a monolithic CMOS-based MEA [5]–[7] using a 0.35-μm CMOS process for electrochemically measuring neurotransmitter secretions from single cells. We designed high-quality transimpedance amplifiers which can measure transient amperometric currents, resulted from the quantal dopamine release with sub-millisecond time resolution and pA current resolution. Half-shared operational amplifiers were designed to maximize the number of amplifiers that can fit into a single CMOS chip to 1024 amplifiers, arranged in 32 columns $\times$ 32 rows. Measurements from the chip revealed low RMS amplifier noise levels $\sim$400 fA at 10-kHz sampling rate [7]. The noise performance of individual amplifiers in the CMOS chip closely matched that of high-end electrophysiology amplifiers [5]–[8].

The quality control of individual electrodes (sensitivity and other electrical properties of electrode-electrolyte interface) becomes difficult as the number of electrodes increases beyond 1000. Microelectrodes are prone to damage or contamination which can affect the sensitivity and background noise. This is especially true if the device is made reusable and the device is used repeatedly. Therefore, the quality of microelectrodes must be individually evaluated after fabrication or repeated use by characterizing the electrodes for possible contamination and its effective surface area. This evaluation step is crucial to perform controlled analytical experiments using the well-characterized electrodes [9]–[11]. Because nanoscopic contaminations are not visible under the microscope, one of the effective ways of characterizing is using cyclic voltammetry (CV) which monitors the electrochemical reaction of the electrode while sweeping the applied potential (Fig. 1a). As such, it can be used to study various characteristics of the electrode, such as its impedance as well as sensitivity to oxidation and reduction reactions [9]–[11]. The large portion of the measured impedance is from the double-layer capacitance, created by the interface created between an electrode and the electrolyte, which is proportional to the effective surface area of the electrode-electrolyte interface (Fig. 1b). When the electrode is contaminated, the effective area to interface with the electrolyte is reduced, diminishing the sensitivity of the electrode. As the contamination is removed from the surface of the electrode, the increased area of the electrode-electrolyte interface can be measured through the larger double-layer capacitance by CV (Fig. 1c). In order to evaluate a large electrode array with 1000s of electrodes, parallel CV can be performed to collect the electrode-electrolyte interface capacitance from 1000s of electrodes simultaneously. This way the researcher can quickly determine the quality of the electrode array and apply an appropriate cleaning procedure, such as short piranha etching or plasma etching, before reevaluating the electrode quality until satisfactory.

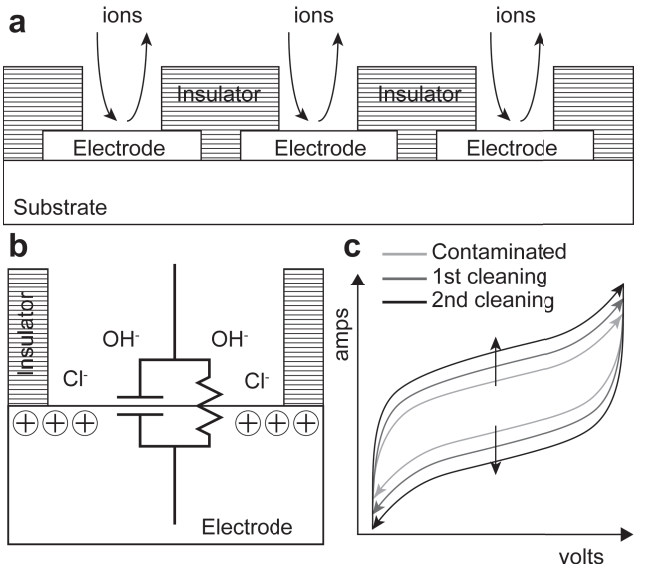

Fig. 1. Double-layer capacitance and cyclic voltammetry progression of a contaminated electrode. (a) The electrolytic solution put on the CMOS electrochemical device introduces ions to the electrode. (b) The electrode is held at a potential for electrochemical measurements, attracting oppositely charged ions in the electrolytic solution and creating a double-layer capacitance at the electrode-electrolyte interface. (c) A contaminated electrode exhibits less sensitivity compared to a pristine electrode. As the electrode is cleaned, the progression of the response shows an increase in sensitivity.

In this paper, we present the design of a monolithic CMOS-based MEA which has the parallel CV capability to perform the characterization of the integrated electrode array. Characterization of the electrode array reveals the state of the surface of individual electrodes. Also, the effectiveness of plasma treatment towards removing contaminants is quantified through characterization of the electrode. In this paper, electrode characterization is performed on the monolithic CMOS electrochemical detector array using parallel CV measurements. In Section II, the design and performance of the designed bipolar transimpedance amplifier (TIA) are discussed as well as the methodology used to integrate the TIA into an electrochemical detector array. In Section III, we discuss the post-CMOS processing used to integrate the electrodes and insulation onto the CMOS chip as well as parallel CV measurements on an electrode array. In Section IV, we discuss the characterization of the integrated electrode array on the monolithic CMOS device using CV before and after a plasma cleaning process.

II. Design of Bipolar Transimpedance Amplifier

To identify oxidation and reduction reactions using CV, bipolar current measurement is required. In this section, we detail the design of a bipolar TIA and its integration into a 1024 electrochemical detector array which enable CV measurements.

A. Bipolar Capacitive Transimpedance Amplifier

A TIA design based on the regulated cascode amplifier allows for a high-injection efficiency of input current which

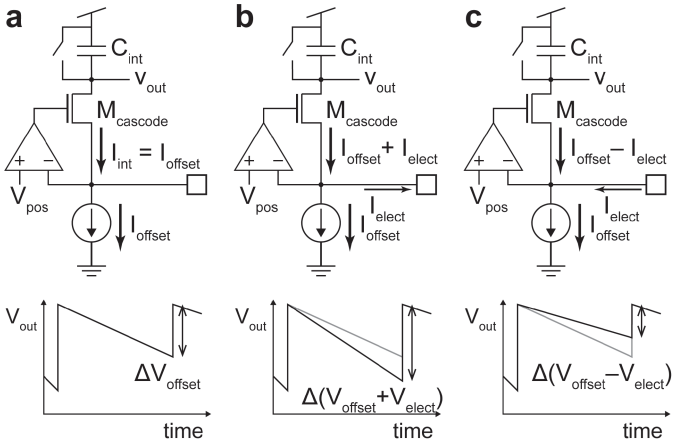

Fig. 2. Designed bipolar capacitive TIA. (a) In the absence of electrons transferred to/from the electrode, only I_{offset} integrated and ΔV_{offset} is readout. (b) During oxidation reactions, the current integrated is increased to $I_{offset} + I_{elect}$, increasing the readout to $\Delta(V_{offset} + V_{elect})$. (c) During reduction reactions, the current integrated is decreased to $I_{offset} - I_{elect}$, reducing the readout to $\Delta(V_{offset} - V_{elect})$.

is beneficial in measuring small picoampere currents [12] (Fig. 2). Our TIA design uses an integrating capacitor to integrate the input current and convert it to voltage using the transimpedance gain. A TIA with a regulated cascode cannot inherently measure bipolar current because the cascode transistor only allows for a downward current direction. To enable bipolar measurement, we introduced a DC offset (I_{offset}) to the input of the TIA (Fig. 2a). With I_{offset} introduced as a baseline measurement, the current from electrochemical reactions at the electrode (I_{elect}) can be either positive ($+I_{elect}$) or negative ($-I_{elect}$) due to oxidation or reduction respectively. Power consumption and area of the amplifier is minimized by using a simple design using five transistors for the operational amplifier (OPA) [7]. Negative feedback through the cascode transistor regulates the potential of the electrode to be the same as the non-inverting input V_{pos}. As the total current (I_{int}) is integrated on the integration capacitor (C_{int}), the voltage of the readout node V_{out} is reduced. At a periodic interval (Δt), the total voltage drop is readout from the amplifier and C_{int} is reset during readout to begin the next integration cycle. This periodic interval determines the sampling rate of the amplifier. To achieve a 10 kS/s sampling rate, the period readout interval is 100 μs. In the absence of electrochemical reactions at the electrode, only I_{offset} is integrated resulting in a readout of ΔV_{offset} (Fig. 2a). During oxidation reactions, electrons are being released into the electrode, creating a current entering the electrode node which results in an integration current above the offset of $I_{int} = I_{offset} + I_{elect}$. The total integrated current is larger during oxidation, resulting in a larger readout of $\Delta(V_{offset} + V_{elect})$ (Fig. 2b). Conversely, in reduction reactions electrons are being taken from the electrode resulting in a total integration current below the offset of $I_{int} = I_{offset} - I_{elect}$. This reduction in integration will result in a smaller readout of $\Delta(V_{offset} - V_{elect})$ (Fig. 2c) during reduction reactions. To sustain the negative feedback of the amplifier, I_{elect} can be as low as $-I_{offset}$ before the TIA effectively turns off. The TIA's transimpedance gain is determined by both C_{int}, estimated to be 116 fF, and Δt. Knowing the transimpedance gain, the bipolar dynamic range of the TIA is $-I_{offset}$ to $+(C_{int} \times (V_{DD} - V_{pos})/\Delta t) - I_{offset}$. With a V_{DD} of 3.3 V, V_{pos} of 1.0 V, I_{offset} of 700 pA, C_{int} of 116 fF, and Δt of 100 μs, the dynamic range is -700 pA – 1968 pA.

B. Bipolar Measurements and Characteristics

To validate the bipolar measurement functionality of the designed amplifier, an external current with both positive and negative polarity is injected into the electrode node of the amplifier while I_{offset} remains constant. The external current is injected by connecting a external l-GΩ resistor to the electrode node and applying a DC voltage to the other terminal of the resistor. Because the voltage at the electrode node is regulated through the feedback, the voltage drop across the resistor can be precisely controlled for current injection into the TIA. The linearity of the amplifier's output is studied by applying various levels of bipolar current. For this particular experiment, the non-inverting input V_{pos}, used to set the electrode potential, is set to 1.0 V. The external input current ranges from -700 pA – 700 pA by applying the DC voltage drop of -0.7 V – 0.7 V on the external resistor. The output of the amplifier, as the voltage applied to the 1-GΩ resistor is changed by a small increment every 5 seconds, is shown in Fig. 3a and the reference of 0 pA corresponds to the integration of only the I_{offset} current, set to 700 pA. The recording showed successful demonstration of bipolar transimpedance measurements. By mapping the output voltage versus the injected current, the linearity of the TIA can be determined as shown in Fig. 3b.The fit shown in the figure gives a transimpedance gain of 0.679 mV/pA with a coefficient of determination, R^2, of 0.998, indicating a high level of linearity for bipolar current measurement from -700 pA to 700 pA.

Further characterization of the amplifier's bipolar capabilities is studied by recording alternating signals. Alternating current is injected into the electrode node using the same method as above. A 1-MΩ resistor is chosen for this experiment to remove the influence of a zero in the frequency response to the circuit. Most component resistors have a parasitic capacitance near 500-fF and thus the zero created by the 1- MΩ resistor is ~318 kHz, which is outside of the sampling rate of 10 kS. The introduction of a zero can result in an inaccurate measurement by increasing the amplitude of the input current and distort the results in the low-frequency range. The tested cases are at frequencies of 10, 100, and 1 kHz with each frequency using the same AC amplitude of 200 μV and at super-imposed DC levels of $+100$pA, 0pA, and -100pA (Fig. 4). The recordings validate the amplifier's ability to measure bipolar alternating current at various frequencies.

C. Integration of 1024-ch Amplifier Array

To integrate an array of amplifiers for parallel electrochemical measurements, a half-shared OPA structure is used, which has been previously studied [6], [7]. The purpose of the half-shared OPA design is to reduce the area required to create a dense sensor array by sharing one non-inverting input with multiple inverting inputs (Fig 5). In the presented device, one non-inverting half of an OPA is shared by groups

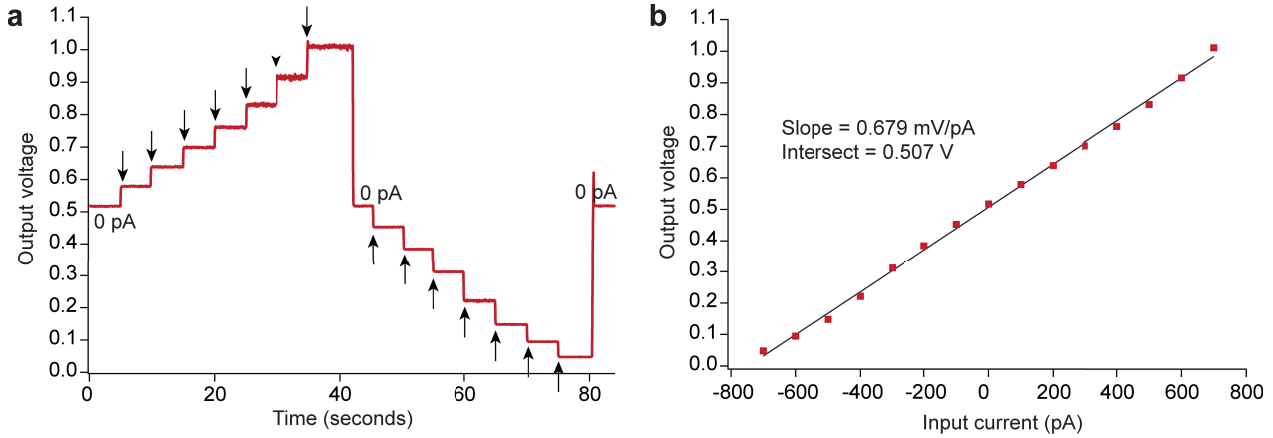

Fig. 3. Bipolar current measurement of the designed TIA (a) Voltage readout of the TIA at different levels of current injected into the electrode. (b) Linear curve fitting illustrating the input current vs output voltage linearity. The TIA used exhibits a transimpedance gain of 0.679 mV/pA with a R^2 value of 0.998, indicating.

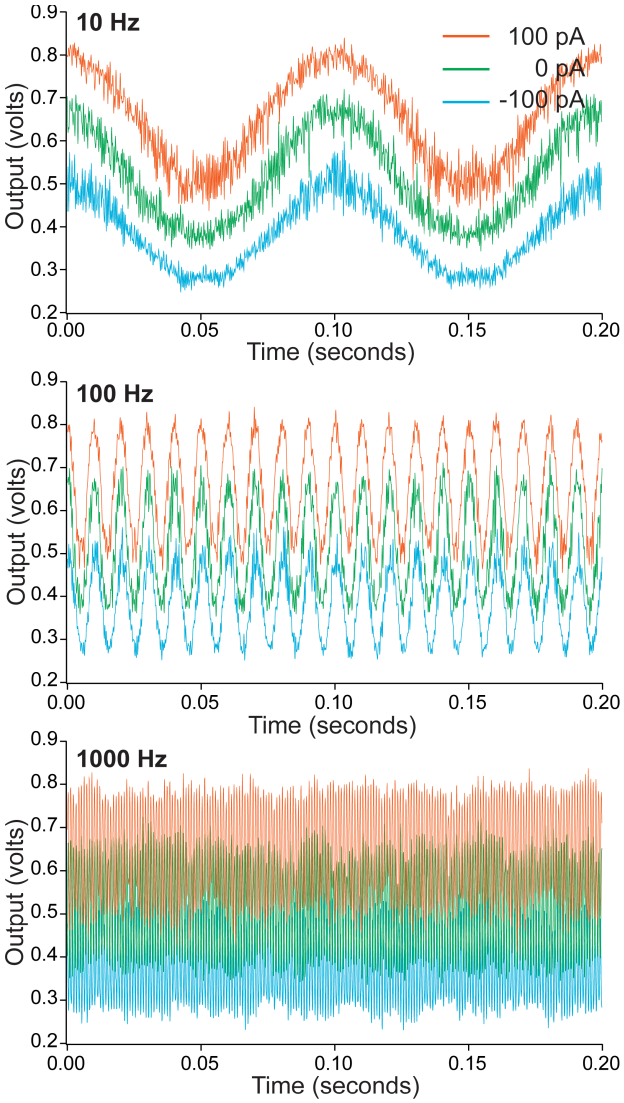

Fig. 4. Measurement of alternating picoampere current at different levels of DC injection and at frequencies of 10, 100, and 1000 Hz.

of 4 TIAs, each of which occupies 30×30 μm^2. The monolithic CMOS device, fabricated in a standard 2-poly 4-metal 0.35-μm process, has an array of 32×32 electrochemical detectors (Fig. 6a).

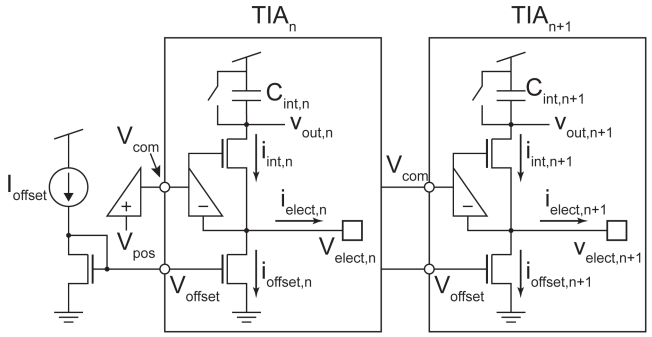

Fig. 5. Half-shared OPA and TIA schematic. The non-inverting half of the OPA is shared among multiple TIAs. Each TIA has a dedicated electrode, integration capacitor, and current mirror generating I_{offset}.

The entire array is operated through the application of two clock signals to the internal timing circuitry which generates a comprehensive set of clock signals required to achieve correlated double sampling, resetting of the integration capacitor in each TIA, and time-division multiplexing. To condense the output of the 1024 electrochemical detectors to 32 parallel outputs on a column basis, time-division multiplexing is used. The time-division multiplexing staggers the readout period, as well as the integration period, of the 32 rows in a column to minimize integration deadtime of the array.

III. Cyclic Voltammetry on an Electrode Array

It is common for semiconductor foundries to fabricate CMOS chips with an aluminum-copper alloy as the top metal layer. However, aluminum is highly reactive to electrolytic solutions and introduces significant offsets and shot noise to electrochemical recordings. To prepare the device for electrochemical measurements, post-CMOS processing is used to integrate polarizable electrode materials with low reactivity, such as platinum or gold, onto the CMOS chip.

A. Monolithic Integration of the Electrode Array

To integrate the platinum electrode array onto the CMOS chip, photolithography is used to perform a lift-off process. The chips are processed individually after they have been attached to a coverslip (25 mm $\times$ 25 mm) to ease the handling

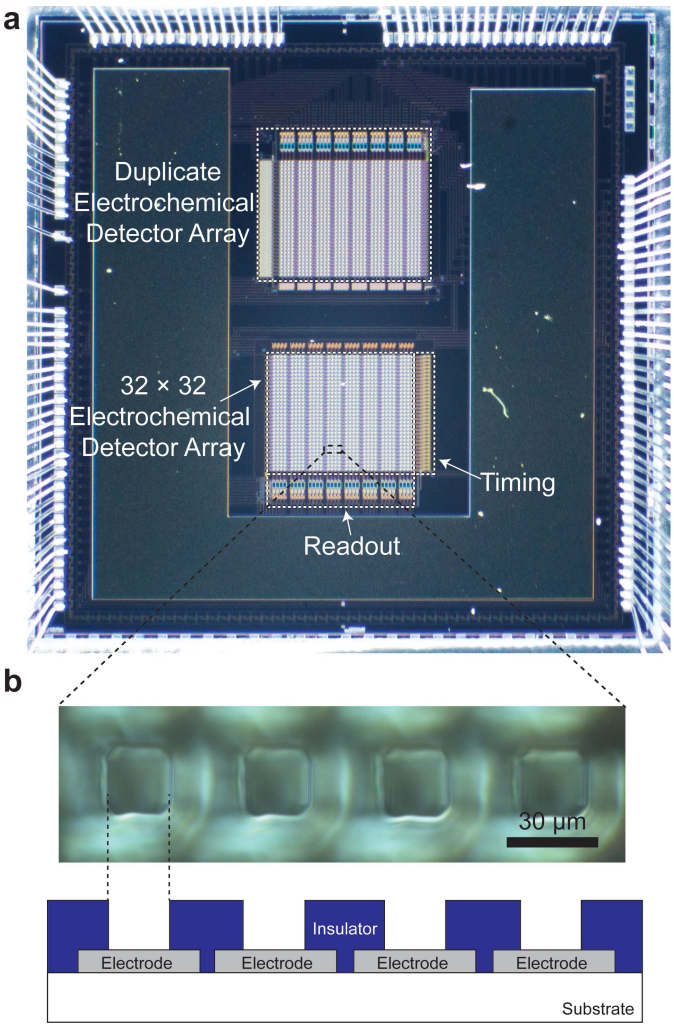

Fig. 6. Photograph of the CMOS chip and the electrochemical detector arrays. (a) Microphotograph of the CMOS chip. To operate the array, two clocks are applied to the timing circuitry. The readout circuitry consists of the 32-to-1 multiplexers and output buffers to drive off-chip ADCs. A duplicate array is on the chip for characterization and testing. (b) The cross-sectional view of the electrode array and four electrodes with the focal plane set to the top of the insulator layer.

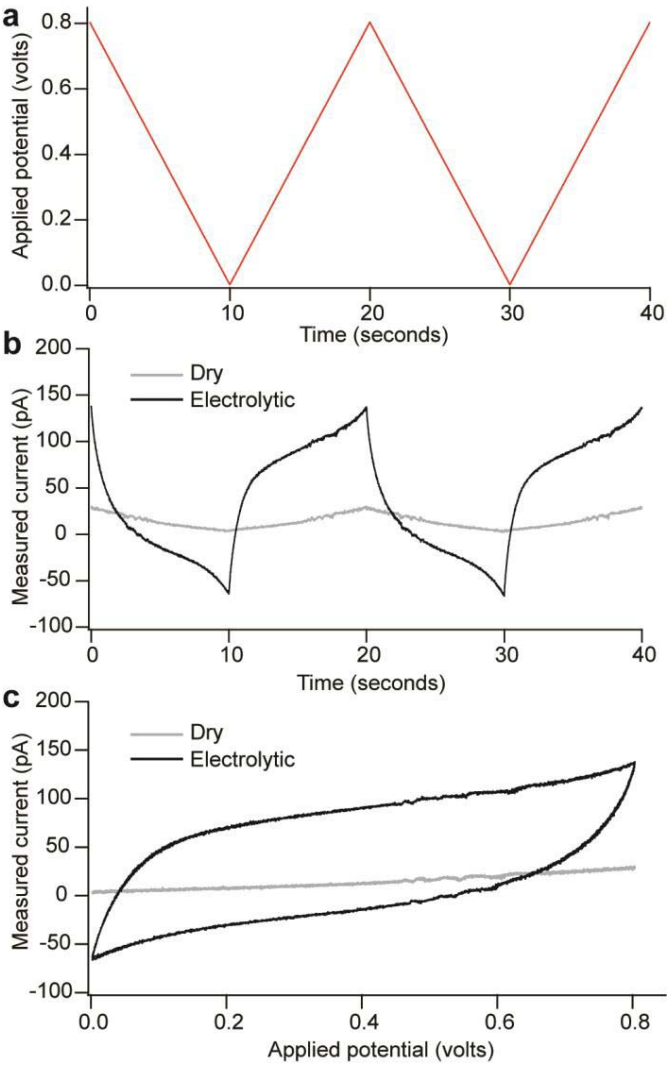

Fig. 7. CV measurement from one TIA electrode. (a) Applied potential vs the reference electrode in the electrolytic solution. (b) Time domain current measurement from a TIA when the device is dry and when PBS is put on the array. (c) Voltammogram of the measured current versus the applied potential. The dry measurement is nearly resistive, and the electrolytic measurement reveals the double-layer capacitance of the electrode.

of the small devices (5 mm × 5 mm). After the chips have been attached to the coverslips, they are cleaned using acetone, isopropanol, and deionized water. For the lift-off process, a sacrificial layer of photoresist is created before metal deposition. This layer is created by spin coating, exposing, and developing a negative photoresist, NR9-1500PY, on the surface of the chip, removing photoresist where the electrodes will be patterned. The electrode materials are then deposited onto the processed chips, starting with the deposition of 20 nm of Ti and then 200 nm of Pt through sputtering (AJA Six-Gun Sputtering System, AJA International Inc., N Scituate, MA). After the metal is deposited onto the chip's surface, the sacrificial layer of photoresist is removed by rinsing the sample with acetone. Removal of the sacrificial layer leaves only the desired electrodes on top of the amplifier array.

To prepare the monolithic CMOS device for electrochemical applications such as single-cell amperometry, a biocompatible epoxy-based photoresist, SU-8 3010, is used to provide isolation between the electrodes in the electrochemical detector array (Fig. 6b). After the lift-off process has been completed, the chips are again cleaned with acetone, isopropanol, and deionized water. The SU-8 photoresist is spin coated, exposed, and developed for patterning. The SU-8 patterns are an array of 15 μm × 15 μm wells atop the electrodes. The SU-8 layer that remains on the surface of the monolithic CMOS device is approximately 20 –30 μm thick.

B. Cyclic Voltammetry on Individual Electrode

Cyclic voltammetry is demonstrated by applying a sweeping electrode potential from 1.2 – 2.0 V in a 20-second period while simultaneously measuring the electrochemical current resulting from reactions occurring at the electrode's surface (Fig. 7). Phosphate-buffered saline (PBS) (2mL) is placed on the electrode array and an Ag|AgCl reference electrode, which is connected to 1.2 V, is placed in the electrolytic solution to form the CV setup. As the potential of the integrated

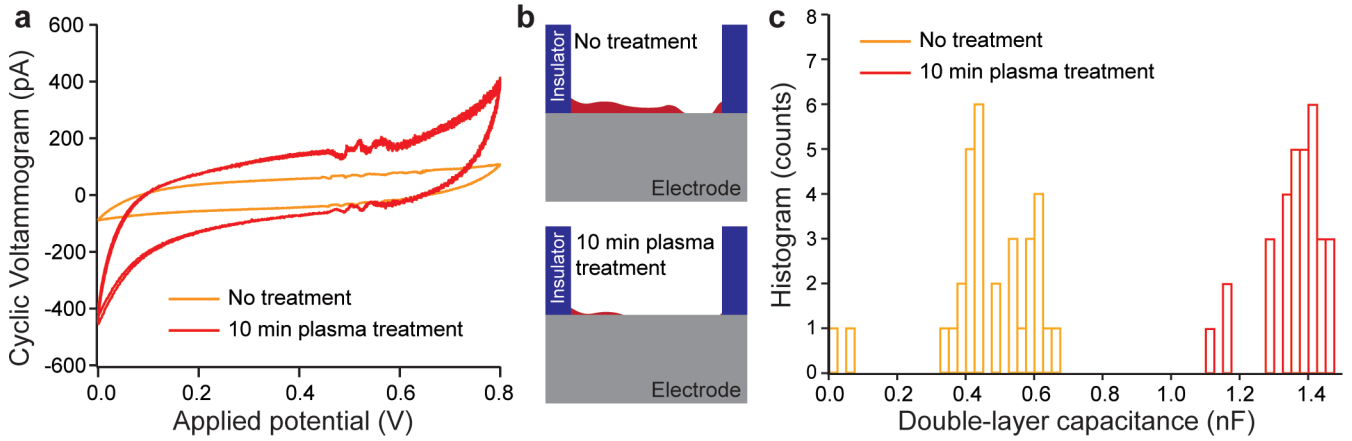

Fig. 8. CV recordings from an electrode array. (a) A representative CV of an electrode before and after 10-min plasma treatment. The electrodes are initially contaminated and exhibit reduced sensitivity as shown in the orange lines. (b) The electrode with contamination on the surface can have reduced surface area where the plasma treatment is anticipated to increase the surface area by etching the contaminant. (c) After plasma treatment, the capacitance of the electrode array is increased consistently throughout the array, reflecting the increased surface area.

electrodes sweep from 1.2 – 2.0 V against the reference of the Ag|AgCl electrode that is held at 1.2 V, the resulting differential voltage drop at the electrode-electrolytic interface is 0 – 0.8 V (Fig. 7a), resulting in a CV scan rate of 80 mV/s. To increase the dynamic range for the CV measurements, the array is run at a sampling rate of 20 kHz. The time domain current measurements from a representative electrochemical detector (Fig. 7b), comprised of a bipolar TIA and its platinum electrode, are done with and without PBS on the array. When there is no PBS on the array, the voltammogram in grey (Fig. 7c) shows a response that is predominantly resistive. After placing PBS on the array, the effects of the double-layer capacitance can be seen. This double-layer capacitance introduces a component to the measured current that reacts to change in the applied potential's slope (Fig. 7b). When dealing with a purely capacitive system, the capacitance can be found by measuring the current that results from the applied potential's slope through the relationship C = I/(dV/dt). However, the presented system has both resistive and capacitive impedance. To remove the influence of current due to resistive impedance, the change in current due to both the positive and negative cycles of the applied potential is examined. To maintain an objectiveness, 400 mV is chosen as a standard to review the change in current across the electrode array. For our CV setup, there is a change of 800 mV over a 10 s period for both the rising and falling cycles of our applied potential, resulting in a dV/dt of 80 mV/s. Examining this change in current at 400 mV and the symmetric slope of the applied potential (Fig 7a), we can estimate the capacitance using the following eq. (1):

$$C = \frac{\Delta I_{bipolar}}{2 \times \frac{dV}{dt}} \tag{1}$$

For this particular electrode (Fig. 7c), the bipolar change in current is 1.19 pA when the electrode array is dry and 104.8 pA when there is electrolytic solution on top of the electrodes. When the array is dry, the voltammogram exhibits 7 pF of capacitance. When electrolytic solution is placed over the array the calculated double-layer capacitance is 660 pF. This significant increase in capacitance demonstrates the dominant capacitance for our CV recordings is from the double-layer capacitance formed by the electrode-electrolyte interface.

IV. Parallel Electrode Array Characterization

To study the quality of the monolithically integrated electrodes, parallel CV is performed to characterize individual electrodes. For the designed electrochemical detector array the input V_{pos} is shared across the array, enabling simultaneous CV measurements. When measuring from the array of electrodes the setup is as previously described, the integrated electrode is swept from 1.2 – 2.0 V, the reference electrode is held at 1.2 V in 2 mL of PBS, and the sampling rate of each amplifier is 20 kHz.

A. Electrode Surface Cleaning

After post-CMOS fabrication, cleaning of the electrode surface is required to ensure that the surface is pristine for use in electrochemical detections because contamination of the electrode's surface reduces its effectiveness for electrochemical measurements. An electrode's surface can be contaminated during the photolithography processes as well as through repeated use of the electrode for electrochemical measurements. In post-CMOS processing, the last step to create an insulation layer using SU-8 has been reported to often leave a thin film on the electrodes after development [13], [14]. Also, molecules, such as dopamine, can also adsorb onto the surface of the electrode [15], [16] after an electrochemical measurement and reduce the sensitivity of the electrode [17]. In this study, we used a plasma cleaner (PDC-32G, Harrick Plasma, Ithaca, NY) to remove organic material from the surface of the electrodes using ionized gas.

B. Parallel Cyclic Voltammograms

The resulting voltammograms from one parallel CV recording are shown in Fig. 8. The levels of contamination of an electrode array can be monitored by measuring the double-layer capacitance across the array through parallel CV recordings. As the area of the electrode's surface is contaminated, the effective area that creates an interface between

the electrode and the electrolyte, the double-layer capacitance, is reduced. Modeling the double-layer capacitance as $C = \varepsilon$ A/d, the reduction of the electrode-electrolytic interface area (A) is directly related to the reduction of capacitance. The electrochemical electrode array, which was previously used for several experiments involving the oxidization of dopamine, is used for electrode array characterization using CV (Fig. 8, orange trace). The recorded set of voltammograms is used to calculate the double layer capacitance formed at each electrode-electrolytic interface. The average capacitance of the electrode array is 0.47 nF with a standard deviation of 0.14 nF. To remove the contaminants, the electrode array is given a 10-minute plasma treatment, and the response of the electrodes is re-characterized (Fig. 8, red trace). The mean capacitance of the array after plasma treatment is 1.36 nF with a standard deviation of 84.5 pF, nearly tripled compared to the initial characterization. The increased mean capacitance reveals that the electrodes could have been previously contaminated and plasma treatment improved the surface condition, increasing the area of the electrode-electrolyte interface and thus the double-layer capacitance.

V. Conclusion

In this paper, we study the quality of an electrode array through parallel CV measurements, as well as present the design and performance of a bipolar capacitive TIA used in a 1024-channel monolithic CMOS device for high-throughput electrochemical recordings. The presented capacitive TIA is capable of measuring bipolar current from oxidation and reduction reactions through the introduction of a DC offset, I_{offset}. The bipolar capabilities of the capacitive TIA are demonstrated by measuring alternating current that is injected into the electrode node. Integration of the bipolar capacitive TIA for large-scale parallel electrochemical recordings in a 1024-channel CMOS device is achieved through the use of the half-shared OPA structure. Through post-CMOS processing, the platinum electrode array and the SU-8 insulation is monolithically integrated on the CMOS device. To examine the quality of the electrode array after repeated use for electrochemical recordings, parallel CV is performed before and after plasma treatment. The contaminations on the electrode surface, such as adsorbed molecules or a thin film of photoresist, reduce the effective area for the electrode-electrolyte interface and thus the double-layer capacitance. After plasma treatment of the electrode array, the capacitance increased substantially, indicating that the surface of the electrodes could have been contaminated and plasma treatment improved the surface of the electrode, thus increasing the electrode-electrolyte interface and the double-layer capacitance. Using parallel CV, characterization of the 1024 electrode array can be accelerated and conducted within minutes before it is used for analytical purposes.

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