

Single-Cell Recording of Vesicle Release From Human Neuroblastoma Cells Using 1024-ch Monolithic CMOS Bioelectronics

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Abstract—Human neuroblastoma cells, SH-SY5Y, are often used as a neuronal model to study Parkinson’s disease and dopamine release in the substantia nigra, a midbrain region that plays an important role in motor control. Using amperometric single-cell recordings of single vesicle release events, we can study molecular manipulations of dopamine release and gain a better understanding of the mechanisms of neurological diseases. However, single-cell analysis of neurotransmitter release using traditional techniques yields results with very low throughput. In this paper, we will discuss a monolithically-integrated CMOS sensor array that has the low-noise performance, fine temporal resolution, and 1024 parallel channels to observe dopamine release from many single cells with single-vesicle resolution. The measured noise levels of our transimpedance amplifier are 415, 622, and 1083 fA_{RMS}, at sampling rates of 10, 20, and 30 kS/s, respectively, without additional filtering. Post-CMOS processing is used to monolithically integrate 1024 on-chip gold electrodes, with an individual electrode size of 15 μm × 15 μm, directly on 1024 transimpedance amplifiers in the CMOS device. SU-8 traps are fabricated on individual electrodes to allow single cells to be interrogated and to reject multicellular clumps. Dopamine secretions from 76 cells are simultaneously recorded by loading the CMOS device with SH-SY5Y cells. In the 42-s measurement, a total of 7147 single vesicle release events are monitored. The study shows the CMOS device’s capability of recording vesicle secretion at a single-cell level, with 1024 parallel channels, to provide detailed information on the dynamics of dopamine release at a single-vesicle resolution.

Index Terms—Amperometric sensors, Bioelectric phenomena, biological cells, biomedical transducers, biosensors, cell signaling, electrochemical devices.

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I. INTRODUCTION

NEUROTRANSMITTER release is modulated by molecular manipulations related to neurological diseases [1] and drug treatments [2]. For example, Parkinson’s disease can considerably reduce the quantity of dopamine release [3] while the drug L-Dopa can increase the amount of secretion [2]. The release of neurotransmitters occurs in quantal packets when vesicles fuse with the cell membrane. By studying the secretion from individual vesicles, we gain rich information regarding the dynamics of membrane fusion [4], obtain insight into the mechanisms of neurological diseases at the molecular level [5], and learn both the desirable and undesirable side effects of drug treatments [6], [7]. Neurosecretory vesicles are small, commonly less than 100 nm in diameter. Release from such a vesicle is a fast process which occurs on a time scale of milliseconds or less and is thus difficult to observe using microscopy. Thus, an electrochemical method (amperometry) is widely used to monitor neurotransmitter release with high temporal resolution by oxidizing neurotransmitters at an electrode [4]. Oxidation is the process of molecules, such as the neurotransmitters dopamine, epinephrine, norepinephrine, and serotonin, releasing electrons into the electrode, generating picoampere currents that can be measured with high-quality low-noise amplifiers. Cyclic voltammetry is also an electrochemical method which is capable of measuring neurotransmitter levels but suffers from a lower temporal resolution compared to amperometry and is adequate for detecting the neurotransmitter level in a slow dynamic system. However, amperometric measurements conducted at the single-cell level and single-vesicle level are traditionally a low-throughput method where each cell is measured individually with a microelectrode under microscopic observation, which makes the technology costly and time consuming to acquire sufficient data to derive statistically significant conclusions.

The limitations of the single-cell amperometry can be overcome by using a scalable CMOS device in which the electrodes are each directly integrated with a dedicated amplifier. Several CMOS-based monolithic biosensors have been proposed using this concept of monolithic integration [8]–[13] to perform various types of electrophysiology with enhanced spatiotemporal resolution. A device that was proposed for the application of DNA sequencing integrated a solid-state nanopore onto a

CMOS chip and achieved enhanced temporal resolution as well as low noise performance with a sampling rate of up to 20 MHz [9], [14]. For the purpose of measuring action potentials from a neuron with a high spatiotemporal resolution, a multifunctional CMOS chip with an array of 59,760 on-chip electrodes can provide a high channel count of up to 2048 electrodes for simultaneous recording [10], [15]. The multifunctional CMOS chip featured 28 amplifiers for neurotransmitter detection using cyclic voltammetry with the 100s of pA_{RMS} noise level. Using an array of 11,011 electrodes, action potentials from axons in a neuronal network were measured with high spatiotemporal resolution [11], [16]. Impedance spectroscopy with a high spatial resolution and low-noise was performed with an array of 59,760 electrodes integrated onto a multifunctional CMOS chip [17]. To study bursting events from neurons in a neuronal network, a device providing high spatial resolution with an array of 4096 electrodes was proposed [18]. Another proposed system contains 1024 pixels to provide a low-noise multifunctional CMOS device with enhanced spatiotemporal resolution for extracellular potential measurement, optical cell detection, current stimulation, and cellular impedance measuring [13]. A low-noise device with an integrated on-chip electrode array was developed for the purpose of parallel recording of neurotransmitter release with a channel count of 100, providing high-throughput amperometric measurements [8]. This monolithic integration of an on-chip electrode array onto a CMOS device has demonstrated the feasibility of recording neurotransmitter release with high-throughput and a fine spatiotemporal resolution [8]. However, the fabricated array did not provide any provision for isolating the electrodes, thus allowing multiple cells to sit atop an electrode, and secretions from adjacent cells can influence readings from the electrode of interest. To address this issue, microwells as described by [19] were incorporated into a 100-electrode amperometry chip [20]. In this paper, we will present a monolithically integrated CMOS-based electrochemical sensor array with 1024 electrode-amplifier pairs operating at a frame rate of 10,000 per second, one of the fastest reported to date. Through the use of SU-8 in post-CMOS processing, structures are created to permit only a single-cell to rest on an electrode. Thus, the monolithic device is able to record neurotransmitter release throughout the array at a single-cell level and permit the resolution of single vesicle release events. The ability to offer a high density of single-cell measurements in a matter of minutes with the presented device offers significant benefit in regards to the study of the dynamics of neurotransmitters and the underlying mechanisms of vesicle secretion. To demonstrate the capabilities of this device, we recorded vesicle secretion from SH-SY5Y cells, a type of neuroblastoma cell that is used as an *in vitro* model for dopaminergic neurons. SH-SY5Y cells are often chosen for Parkinson's disease studies because of their human origin and similar catecholaminergic neuronal properties to dopaminergic neurons of the midbrain [21], [22].

In Section II, we discuss the design and characterization of CMOS devices with 1024 transimpedance amplifiers (TIAs). In Section III, we describe post-CMOS processing for integrating an on-chip electrode array. In Section IV, we discuss

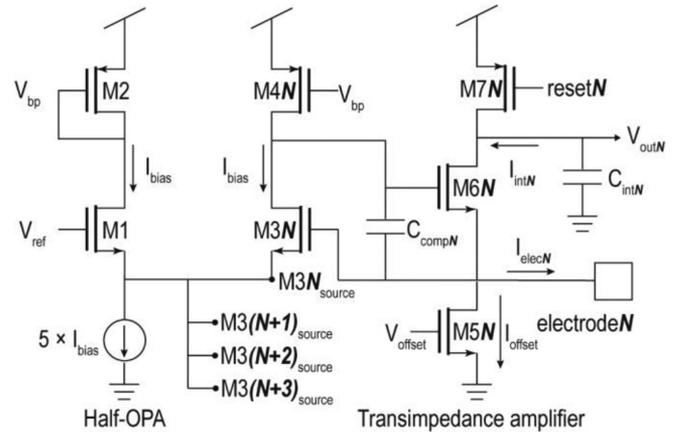


Fig. 1. Schematic view of the half-shared OPA and TIA designs. One half-OPA is shared among four TIAs. In a TIA, the current induced by the oxidation of neurotransmitters ($I_{\text{elec}N}$) is added to an offset current (I_{offset}). The currents are integrated on an integration capacitor ($C_{\text{int}N}$) and read out periodically ($V_{\text{out}N}$).

on-chip recordings of SH-SY5Y's dopamine releases using the monolithic CMOS device. In Section V, we analyze the measurements of neurotransmitter release.

II. DESIGN OF 1024-CH TRANSIMPEDANCE AMPLIFIER ARRAY

In this section, we describe the design of our CMOS device comprising a 1024-ch TIA array integrated with an on-chip array of 1024 electrodes. The resulting high-density electrode array is capable of measuring picoampere currents.

A. Half-Shared Operational Amplifier Design

Designing a small-sized TIA is a requirement to enable the integration of an array of 1024 amplifiers into a single silicon die. To use the silicon area most effectively, we adapted the half-shared operational amplifier (OPA) design of [23]. In this design, the non-inverting input is shared by several inverting inputs. The half-shared design achieves a significant reduction of cell area by almost a factor of two and reduces the power consumption by nearly half. The disadvantage of the half-shared design is the lack of individual control of the non-inverting input voltages. However, in many high-throughput applications including amperometry, individual control of the non-inverting inputs is not necessary [8], thus making the half-shared design advantageous. The half-shared design and TIA design is depicted in Fig. 1. The OPA uses a simple five-transistor design to minimize the area and power consumption. The current mirror, formed by M2 and M4N, closely matches the current level in all branches of sharing OPAs. The non-inverting input transistor, M1, is in the half-OPA and the inverting input transistor, M3N, is in the individual TIA. Negative feedback through M6N regulates the voltage at electrode N to be the same as the non-inverting input voltage (V_{ref}). The TIA uses a two-stage amplifier, thus the phase margin needs to be considered. The open-loop configuration without feedback is studied with M3N gate as the input and M6N source as the output. Two poles are from the M3N

TABLE I
DIMENSIONS OF TRANSISTORS IN THE TIA DESIGN

	M1	M2	M3 _N	M4 _N	M5 _N	M6 _N	M7 _N
Width	10 μm	10 μm	10 μm	10 μm	5 μm	1.2 μm	0.8 μm
Length	10 μm	10 μm	10 μm	10 μm	5 μm	1.2 μm	0.4 μm

drain and M6_N source. The dominant pole is introduced from the capacitance at the electrode and the 2nd pole can be close to the dominant pole because M3_N is operating in moderate to weak inversion. Thus, a compensation capacitor ($C_{\text{comp}N}$), a 20-fF polysilicon-insulator-polysilicon (PiP) capacitor, is used to increase the phase margin of the TIA by producing a zero ($g_{m3N}/C_{\text{comp}N}$) which closely matches the frequency of 2nd pole from M3_N. The current from the electrode ($I_{\text{elec}N}$) is integrated on the integration capacitor ($C_{\text{int}N}$), which causes the voltage of $C_{\text{int}N}$ to drop (ΔV). This voltage drop is readout periodically with a cycle interval (Δt) from each TIA. The cycle interval is determined by the desired sampling rate. For example, if a cycle interval of 100 μs is used, the resulting sampling rate of the TIA is 10 kS/s. During the readout, $C_{\text{int}N}$ is reset through M7_N transistor to re-initiate the next cycle of integration. The dimensions of each transistor in the TIA design are listed in Table I. $C_{\text{int}N}$ represents the total capacitance at the integrating node, including a passive PiP capacitor component and parasitic capacitors added by nearby transistors (M6_N and M7_N). The TIA includes two interchangeable $C_{\text{int}N}$ s, whose estimated capacitances are 116 fF and 13 fF. The transimpedance gain of the TIA is determined by Δt and $C_{\text{int}N}$. The measured transimpedance gain of every 1024 amplifiers is 0.86 ± 0.03 mV/pA (standard deviation, SD) and 7.72 ± 0.99 (SD) mV/pA, for 116 fF and 13 fF, respectively. A larger deviation in gain is observed when using the 13-fF $C_{\text{int}N}$ compared to using the 116-fF $C_{\text{int}N}$. This is because the small $C_{\text{int}N}$ is largely made of parasitic capacitance at the integration node which is inconsistent across the array. The integrating capacitor is incapable of integrating negative current, thus only offering unipolar measurements. To enable bipolar measurements, an offset current (I_{offset}) is applied in the TIA using M5_N. I_{offset} is superimposed on $I_{\text{elec}N}$ to generate $I_{\text{int}N}$, and when the electrode current drops below zero, $I_{\text{int}N}$ reduces below $I_{\text{offset}} \cdot I_{\text{elec}N}$ can drop as low as $-I_{\text{offset}}$ and still sustain positive current through M6_N. If $I_{\text{elec}N}$ falls below $-I_{\text{offset}}$, the negative feedback will be disabled, effectively turning off the TIA. Thus, the TIA is capable of bipolar measurement with a dynamic range of $-I_{\text{offset}}$ to $+(C_{\text{int}N} \times (V_{\text{DD}} - V_{\text{ref}})/\Delta t) - I_{\text{offset}}$. The TIA's dynamic range is -500 pA– 2516 pA with $C_{\text{int}N}$ s of 116 fF, Δt of 100 μs , I_{offset} of 500 pA, and V_{ref} of 0.7 V.

B. Bandwidth and Noise Characteristics

The TIA is characterized by injecting known AC and DC currents into the electrode node. The TIA's frequency response is measured by applying sinusoidal voltage (AC amplitude: 200 μV –2 mV) through a 1-M Ω resistor into the amplifier, for a range of frequencies extending beyond the Nyquist frequency. This input generates a sinusoidal current of 200 pA–2 nA that can be measured using the TIA. We chose a 1-M Ω resistor be-

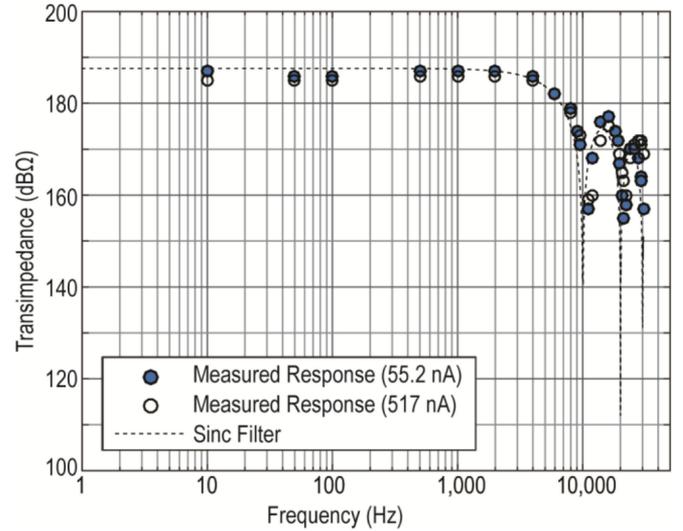


Fig. 2. The frequency response of the half-OPA-based TIA.

cause of a possible zero interfering with the frequency-response measurement. An introduction of the zero by the input resistor (and its parallel parasitic capacitor) in the low frequency range can cause a larger input current which results in a misinterpretation of the frequency response. With an approximate parasitic capacitance of 500-fF across the resistor, the zero of the input resistor and parasitic capacitor is expected to be at 318 kHz, which is beyond the frequencies of interest. As expected, the frequency response of the TIA, as a result of periodic sampling of the integration capacitor, has the characteristics of the sinc function (Fig. 2). When examining the characteristics of the TIA in the frequency domain, two bias conditions are tested: I_{bias} of 517 nA and 55.2 nA. The dominant pole of a sinc filter at a sampling rate of 10 kS/s is expected to be ~ 4.4 kHz, thus the influence of the biasing level is limited while the sinc's dominant pole is lower than the bandwidth of the OPA. The frequency response follows the characteristic of a Sinc filter with a -3 dB point of ~ 4.4 kHz. The frequency response beyond the -3 dB point still influences the sampling bandwidth, thus aliasing, however, the frequency response sharply drops with the sinc filter. Peaks of side lobes follow an approximately -20 dB/dec slope up until 5th sidelobe, which is equivalent to a single-pole anti-aliasing filter. Because the sinc filter has nulls at every integer of the sampling frequency (10 kS/s), the aliasing noise is smaller compared to a single-pole anti-aliasing filter. When the electrolytic solution is placed on the electrode, the double-layer capacitance, which can be in the order of tens of pF, is likely to influence the performance of the TIA. With an electrolytic solution covering the array, an average noise of 6.16 pA_{RMS} is measured with the corner frequency of the capacitive noise ranging from 60 to 200 Hz. The test conditions are a bias level of 55.2 nA and an I_{offset} of 100 pA. The presented bandwidth measurement (Fig. 2) is performed by using a bus that runs across the entire array, ExConE. When ExConE is connected to the TIA, 25.81 pF of input capacitance is measured at the electrode node. This capacitance is only present to the electrode

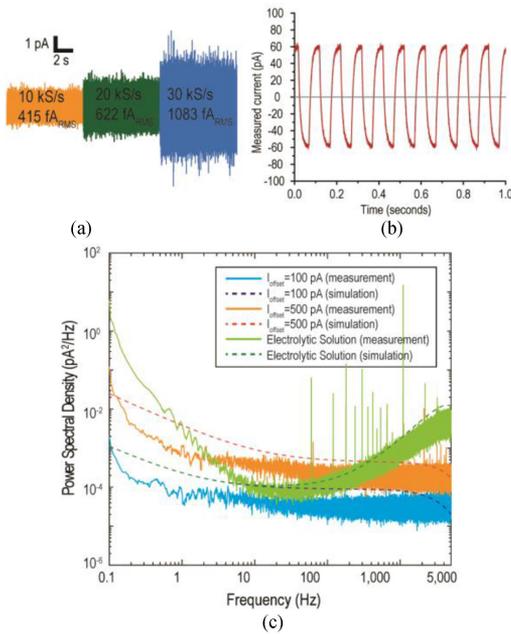


Fig. 3. Performance of the TIA array. (a) The noise levels of the amplifier at 3 different sample rates. (b) Bipolar current measurement using the TIA. (c) The noise spectral density of the amplifier when I_{offset} is set to 100pA, 500pA, and when an electrolytic solution covers the array.

node during the bandwidth measurement and is removed by an internal switch controlled by embedded SRAMs (explained in Section II-C.). Therefore, the bandwidth in the presence of the electrode-electrolyte interface is expected to be comparable to the measured bandwidth.

Because of the integrating capacitor's intrinsic characteristic, noise introduced from aliasing is minimal. This built-in low-pass filter eliminates the need for an anti-aliasing filter in the readout circuitry, resulting in a smaller design area. Under these test conditions, each TIA consumes 182 nW to maintain the full bandwidth and performance. Overall, the average noise level of all 1024 amplifiers is 421.4 ± 1.1 (SD) fA_{RMS} at 10 kS/s using the $13 - \text{fF } C_{\text{int}N}$. Because shot noise is expected to be $400 \text{ fA}_{\text{RMS}}$ with the 100-pA DC current, the contribution of the amplifier can be calculated to $132.6 \text{ fA}_{\text{RMS}}$. For I_{offset} levels of 500 pA and 1000 pA, the measured noise levels are 1.496 ± 0.012 (SD) pA_{RMS} and 1.769 ± 0.028 (SD) pA_{RMS} . The noise levels of the TIAs are measured at the 55.2-nA bias level. One selected TIA exhibits noise levels of $415 \text{ fA}_{\text{RMS}}$, $622 \text{ fA}_{\text{RMS}}$, and $1083 \text{ fA}_{\text{RMS}}$, at sampling rates of 10 kS/s, 20 kS/s, and 30 kS/s, respectively at the 55.2-nA bias level with I_{offset} set at 100 pA (Fig. 3a). Compared to a high-quality electrophysiology amplifier, the Axopatch 200B with a resistor-feedback headstage and 10 mV/pA gain with a 100-pA input current, the measured noise spectral density of the TIA demonstrates comparable noise performance ($\sim 4 \times 10^{-5} \text{ pA}^2/\text{Hz}$) (Fig. 3). The noise simulation based on the technology-specific parameters are also presented (Fig. 3c). Because the noise analysis on a non-stationary circuit is impractical, a load resistor is added into the integrating node $V_{\text{out}N}$ in Fig. 1 to produce a stationary circuit. The simulated noise is then multiplied to a Sinc function to emulate the fil-

tering effect from the integrating capacitor. For the electrolytic solution simulation, we added a 25-pF input capacitor to represent the electrode-electrolytic interface capacitance. The flicker noise matches closely between the measurement and the simulation result. Typically, the flicker noise corner can be below 10 Hz when the input current level is deep in weak inversion [24], which agrees with the measured noise spectral density. However, a mismatch in noise level is observed. This may be due to the poor matching of the design parameters in the deep weak-inversion. Designing the TIA with small-sized transistors can result in large mismatches between identical TIAs. This is due to the manufacturing imperfection that mainly influences effective width (W) and length (L) of fabricated transistors [25]. The OPA determines the bandwidth and $V_{\text{elec}N}$, and thus transistors in the OPA need large W and L to minimize mismatch. By adapting the half-shared OPA, investment in a large area for W and L is achievable as the inverting-half of an OPA requires only two transistors, $M3N$ and $M4N$. The size selected for $M3N$ and $M4N$ is $10 \mu\text{m} \times 10 \mu\text{m}$ (Table I). The input-referred output is measured throughout the array, resulting in a measured variation of $1.26 \text{ mV}_{\text{RMS}} \cdot I_{\text{offset}}$ is also subject to mismatch due to process variation. However, the mismatch in I_{offset} across the array only affects the dynamic range by several pA which has negligible effect during the electrochemical recordings.

The crosstalk between the sharing OPAs has been considered. As discussed by a previous publication [23], the response of each inverting-half of OPA is only a function of transconductance ($M3N$) and output impedance ($M4N$). Thus, as long as the sharing node ($M3N_{\text{source}}$) is kept constant with a constant non-inverting input, the crosstalk should be minimal. To confirm this, a 100 Hz current with 400-pA pk-to-pk is injected into a OPA while recordings are taken from three OPAs which share the inverting-half. The power loss between the original injected current and crosstalk measured from sharing OPAs is quantified. A heavy attenuation of $-38.7 \text{ dB} \pm 3.4 \text{ dB}$ (standard deviation) is observed. The small crosstalk may be due to the limitation of the recording setup rather than actual crosstalk through the sharing structure. The 100 Hz current is injected through a bus which runs across the entire array, which is only enabled during the electrical testing.

C. Integration of 1024-ch Amplifier Array

Fig. 4 shows a CMOS device containing an array of 32×32 amplifiers and electrodes fabricated in a standard $0.35\text{-}\mu\text{m}$ 4-metal 2-poly CMOS process. In the presented design, four TIAs share one non-inverting-half OPA. Each TIA occupies a $30 \times 30 \mu\text{m}^2$ area and includes a 1-bit SRAM. Thus, the array has a total of 1024 1-bit SRAMs. Using the column and row decoders, the embedded SRAM in each TIA is fully-addressable providing the capability to reconfigure the amplifier for unity gain, and/or enable testing circuitry. Also, global switches can be used to change the transimpedance gain, and enable/disable the phase compensation capacitor.

To operate the array, two clock signals are applied to the timing circuitry and clock signals are generated to achieve time-division multiplexing, correlated double sampling (CDS), and

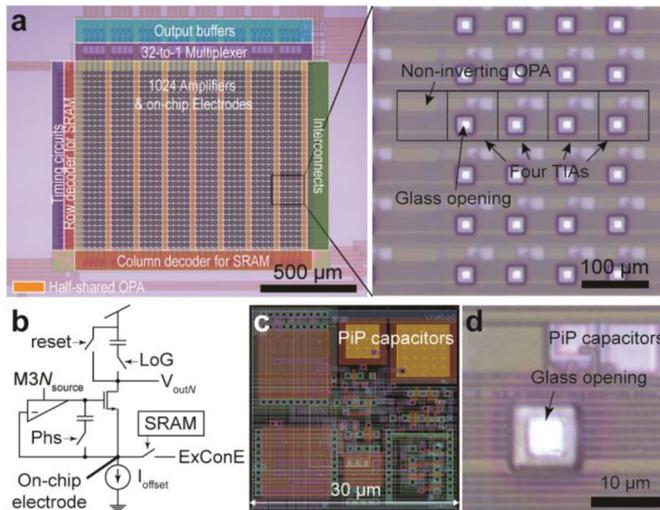


Fig. 4. Photographs and architecture of the CMOS die and amplifier array. (a) The array has 1024 amplifiers and 1024 on-chip electrodes. The 32-to-1 multiplexer combines outputs by time-division multiplexing to condense the data. Row and column decoders allow for fully-addressable writing of embedded SRAMs in the array. (b) Each TIA has low-gain (using LoG), phase margin (using Phs) options. Also, SRAM can be programmed to connect the ExConE node to the electrode node for testing. (c) The layout of one TIA is $30\ \mu\text{m} \times 30\ \mu\text{m}$. (d) The microphotograph of the TIA is showing PiP capacitors and glass opening.

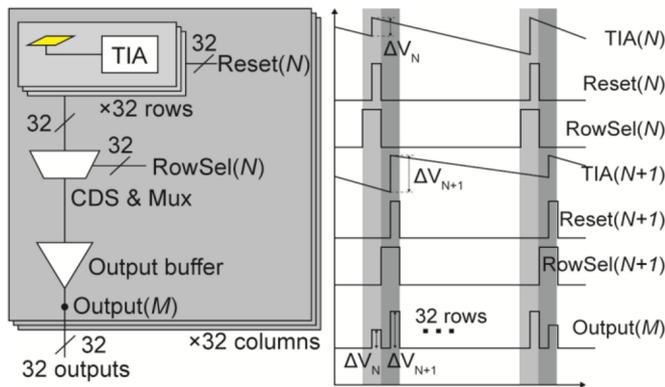


Fig. 5. The block diagram of time-division multiplexing and timing diagram. Each gold electrode (yellow box) is connected to its respective TIA which is physically embedded directly underneath. Each row of TIA has a dedicated reset, $\text{Reset}(N)$. The integrated voltage, ΔV_N , is generated from each TIA after each reset. Each $\text{Reset}(N)$ is synchronized with $\text{RowSel}(N)$ which samples the TIA output before and after each reset, thus enabling correlated double sampling. The integration periods of each TIA in every row are staggered in time to allow the time-division multiplexing without downtime in integration. After multiplexing, $\text{output}(M)$ includes ΔV_N of all the rows.

resetting of the integration capacitors (Fig. 5). The generated clocks provide the means of condensing the output of the array of 1024 sensors to 32 parallel outputs, one output per column, $\text{output}(M)$, through time-division multiplexing. Time-division multiplexing will sequentially stagger the integration period of each row, reading out the integrated current of one TIA, ΔV_N , while the other amplifiers in the column continue to integrate their respective inputs, as previously described [8]. The array with all the peripheral circuits is compacted and only occupied $\sim 1.5\ \text{mm} \times 1.5\ \text{mm}$. In this $5\ \text{mm} \times 5\ \text{mm}$ silicon chip, there are

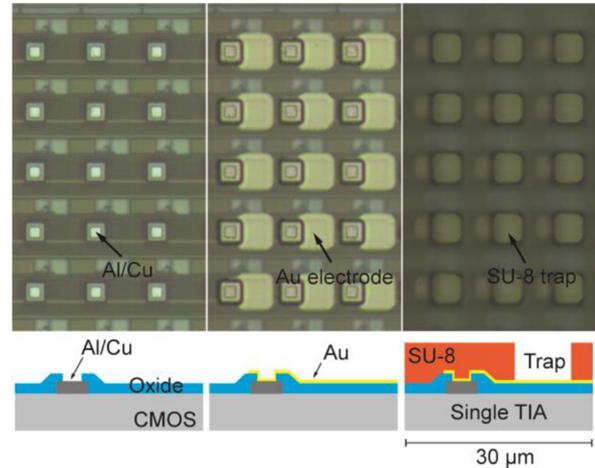


Fig. 6. Post-CMOS processing for on-chip integration of electrodes and SU-8 wells. Initially, the CMOS die has Al/Cu as the top metal. Gold layer is patterned using lift-off process which is followed by the fabrication of SU-8 wells. The SU-8 wells are used to trap single cells.

also electrostatic discharge (ESD) circuits and unused testing circuits which are not visualized in the microphotograph in Fig. 4.

Because the CMOS chip relies on external ADCs for digitization, source-follower-based output buffers are designed to drive the capacitive load from the output line, pad and ADC input capacitance. The overall power consumption of the chip is 12.5 mW.

III. POST-CMOS PROCESSING

CMOS chips fabricated from foundries commonly have aluminum-copper (Al/Cu) for the top metal layer. The aluminum is highly reactive with electrolytic solutions, making the unprocessed devices intrinsically inadequate for biosensing. This reactive material not only causes large offsets in electrochemical recordings, thus introducing a high level of shot noise, but the chip can also be damaged due to water leakage. To resolve this issue, post-CMOS processing can be used to integrate polarizable electrode materials, such as gold or platinum, on top of the topmost metal layer. These materials have low reactivity, making them suitable for biological recording.

A. On-Chip Gold Electrode Array

The CMOS dies are first processed using photolithography to integrate the gold electrode array onto the surface of the chip through a lift-off process. Each die ($5\ \text{mm} \times 5\ \text{mm}$) is initially attached to a coverslip ($25\ \text{mm} \times 25\ \text{mm}$) to reduce the complications of handling the small CMOS chips through the standard cleanroom process. Before the chips are spin coated with photoresist, they are cleaned using acetone, isopropanol, and deionized (DI) water. A negative photoresist, NR9-1500PY, is spin coated onto the surface of the chip, exposed, and developed to create the patterns for the electrodes, leaving a sacrificial layer of photoresist on the surface where metal deposition is undesirable. The electrodes are created by first depositing 15 nm

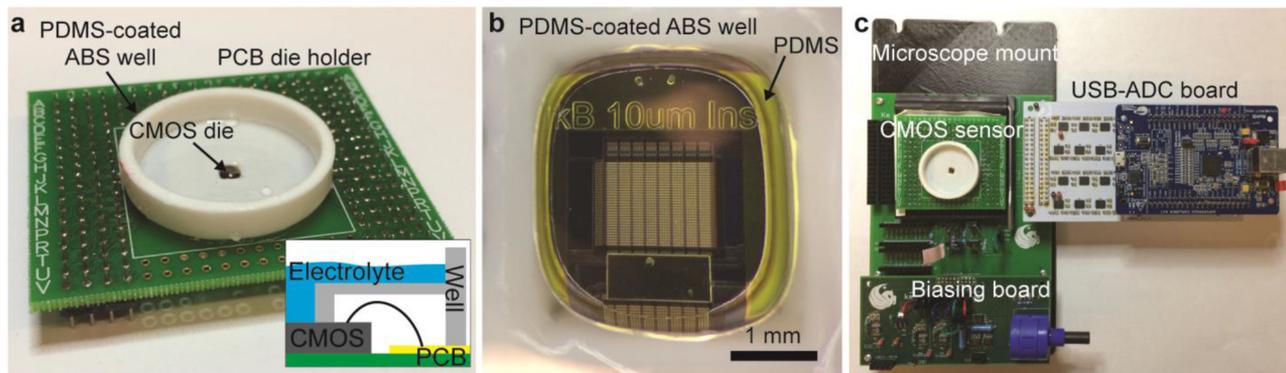


Fig. 7. The recording setup of the CMOS chip. (a) Biocompatible packaging of the CMOS chip by using PDMS-coated 3D-printed ABS well. (b) The photograph of the electrode array opening. (c) The custom-design PCBs for biasing and data acquisition using USB 3.0.

of titanium and then 150 nm of gold on the surface of the chips through sputtering (AJA Six-Gun Sputtering System, AJA International Inc., N Scituate, MA). The purpose of the deposited titanium is to provide adhesion between the Al/Cu layer on the surface of the chip and the deposited gold. To remove the sacrificial layer of photoresist, lift-off is performed by rinsing the chip with acetone. After removal of the sacrificial layer, the electrodes are patterned as intended (Fig. 6).

B. SU-8 Traps for Single-Cell Analysis

After lift-off has been completed, the chips are cleaned again using acetone, isopropanol, and DI water. With the array of gold electrodes integrated onto the surface of the chip, further photolithography processing is performed using SU-8 3010, a biocompatible epoxy-based photoresist. The SU-8 photoresist is used to provide isolation between each electrode in the array and to create well structures that can trap a single cell on top of an electrode [19], [20], as shown in Fig. 6. The estimated thickness of SU-8 traps is 20–30 μm . To achieve true single-cell measurements, the SU-8 is necessary to not only prevent multiple cells from populating a single electrode, but to also prevent the influence of adjacent cells and electrodes.

C. Packaging

After the array of electrodes and SU-8 traps are integrated onto the surface of a chip, it is bonded to a PCB die holder using a silver-filled epoxy (Fig. 7a). Once the epoxy has cured, the chip is wire-bonded to provide an interface to the inputs and outputs of the circuitry on the chip. To protect the easily broken wire bonds when handling the PCB and from liquids during experiments, a plastic well is manufactured to cover and protect the bonds and pads exposed on the chip. The well is designed to accommodate 2 mL of liquid, 3D-printed using ABS plastic, and coated with a layer of polydimethylsiloxane (PDMS) for waterproofing and biocompatibility. The coated well is bonded to the custom PCB and the surface of the CMOS chip using additional PDMS. As shown in Fig. 7b, the well conceals the wire bonds, provides an opening for access to the surface of the CMOS chip, and protects external electronics from liquids used during experiments. To prepare the CMOS chip for

SH-SY5Y cell measurements, the packaged devices is cleaned using a plasma cleaner (PDC-32G, Harrick Plasma, Ithaca, NY). This is necessary as there is a remaining thin film of SU-8 over some of the electrodes in the array after the resist is developed. After plasma cleaning, 1 mL of water is added to the surface of the chip and the device is placed into a vacuum chamber. By vacuuming the chip with liquid on the surface, bubbles that are captured in the SU-8 traps will be eliminated. After eliminating the bubbles in the SU-8 traps, the surface of the CMOS will continue to be covered with liquid to prevent air from being captured in the SU-8 single-cell traps.

IV. SH-SY5Y CELL MEASUREMENTS

A. Recording Setup

The setup for SH-SY5Y cell recordings is shown in Fig. 7c. It consists of custom PCBs that hold a socket for the packaged chip, supply power and biasing to the chip, and convert and transmit analog data collected from the chip to a computer through a USB interface. The PCB die holder has pin headers to allow access to the inputs and outputs of the chip for testing and operation, as well as setting the current biasing for the TIAs in the array and the output buffers using resistors. The smaller PCB that connects to the foot of the PCB holding the socket generates the voltages needed for the chip to operate and the baseline current used for the TIAs. When operating the chip, V_{ref} is set to 0.7 V and I_{offset} is set to 500 pA.

The USB data acquisition system consists of a custom designed PCB that has a microcontroller (Atmel SAM E70), 32 ADCs with 16-bit resolution (LTC2323-16), and a USB 3.0 controller (Cypress FX3). The Atmel chip functions as the control center for the acquisition system. All of the clocks required for the data acquisition system and the CMOS chip, are generated by this Atmel chip. The clocks generated for the CMOS chip are setup to achieve a sampling rate of 10 kHz for each amplifier and a multiplexed output rate of 320 kHz. The Atmel chip also provides the digital signals for the column and row decoders to program the SRAMs in the array as well as the reference voltage for the amplifiers through an embedded DAC. The 32 ADCs convert the 32 parallel, time-multiplexed, signals

from the CMOS chip into their binary representations at a rate of 1.3 MHz. The binary data from these ADCs are delivered directly to the USB 3.0 controller. The USB controller accumulates the data from the ADCs in its embedded memory and then transfers the data to a connected computer in packets at a rate of 106 MB/s.

B. Single-Cell Amperometry

SH-SY5Y neuroblastoma cells (ATCC# CRL-2266) are cultured in T-75 flask with 20 ml of growth media, which consists of a 1:1 ratio of MEM with L-Glutamate (Invitrogen) and F12 media (Invitrogen), 10% fetal bovine serum (FBS, Gibco) and 1% Antibiotic/antimycotic (Gibco). The cells are cultured in a 5% CO₂ incubator at 37 °C. The media is changed every 3 days. These cells mostly grow as adherent cells under these conditions. Cells are passaged when the culture becomes 80% confluent. To detach the cells, the growth media is removed, the cells washed with phosphate buffered saline (PBS, pH7.4), and incubated with Trypsin-EDTA (Gibco, 0.25%) at 37 °C for 5 minutes, until most of the cells are detached from the flask. Trypsin is deactivated by the addition of FBS. The cells are washed twice with PBS by centrifugation at 1500 rpm for 5 minutes. The cells are then immediately used for the experiments or plated in a new T-75 flask for further expansion in the culture.

For the recording of neurotransmitter releases from SH-SY5Y cells, the 1 mL of water that is on the chip (refer to Section III-C.) is replaced with 1 mL of suspended SH-SY5Y cells in culture media. With the cells floating on the surface of the packaged chip, it is placed into an incubator at a temperature of 37 °C and 5% CO₂ for one hour to provide time for the cells to be captured in the SU-8 traps and settle onto the bottom surface. Settled cells are randomly distributed on the CMOS chip. Some cells adhere to the SU-8 surface and some cells fall into the SU-8 traps. Once the cells are trapped and adhered in the SU-8, the 1 mL of culture media is exchanged with 1 mL of recording buffer. The recording buffer contains the following concentrations at a pH level of 7.3 and an osmolality of 300 mmol/kg: 140 mM NaCl, 5 mM KCl, 1 mM MgCl₂, 10 mM CaCl₂, and 10 mM HEPES/NaOH. At this point, the chip with cells is ready for recording and is placed into the socket (Fig. 7c). An Ag|AgCl reference electrode connected to ground is placed in the recording buffer and then the power and clock signals are applied to the chip. To stimulate the cells, 1 mL of a high KCl stimulation buffer is added to the recording buffer. The stimulation buffer has the same pH level and osmolality of 7.3 and 300 mmol/kg, respectively, with the following concentrations: 140 mM KCl, 5 mM NaCl, 1 mM MgCl₂, 10 mM CaCl₂, and 10 mM HEPES/NaOH. The anticipated KCl concentrations after adding the stimulation buffer is 72.5 mM, which is known to cause depolarization of the cell membrane and stimulate vesicle secretions [26].

C. 1024-ch Parallel Recordings of Vesicle Releases Using CMOS Chip

The diameter of a suspended SH-SY5Y cell is ~12 μm, which is marginally smaller than the 15 μm × 15 μm SU-8 single-cell

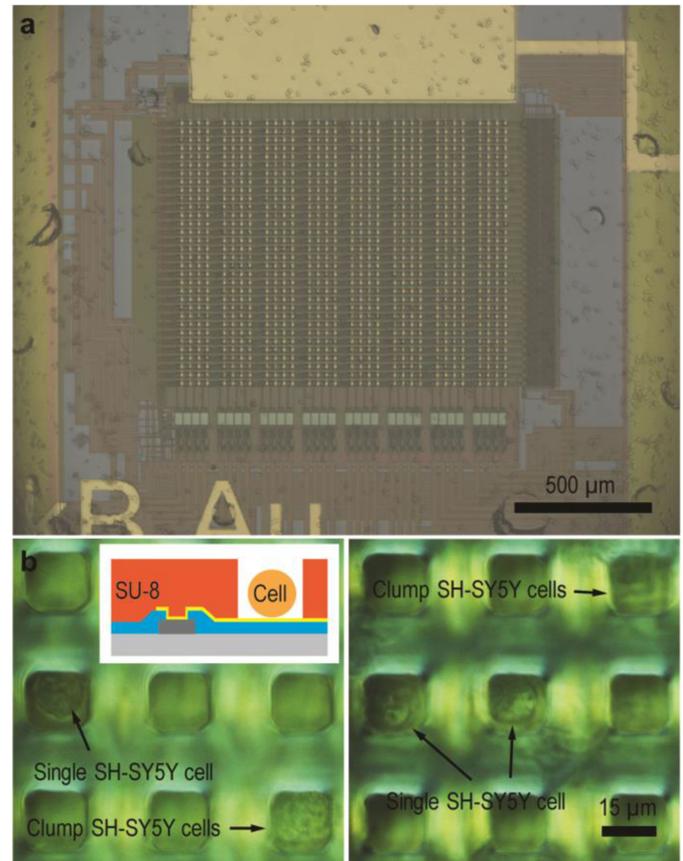


Fig. 8. (a) Microphotograph of SH-SY5Y cells on the CMOS device. (b) Differential interference contrast (DIC) image of SH-SY5Y cells on the CMOS device. Single SH-SY5Y cells are trapped in SU-8 traps. The traps allow only single cells to fall in to make contact with the electrode. The image has been processed by adjusting the contrast.

traps (Fig. 8). Many individual SH-SY5Y cells trapped in SU-8 wells are observed (Fig. 8b), allowing single-cell amperometry from the respective electrodes. Multicellular clumps that are also present failed to fit into the SU-8 traps because the SU-8 trap is only large enough for a single cell (Fig. 8b). For this experiment, of the 1024 SU-8 traps, roughly ~10% of the electrodes in the array are covered by a single cell. The CMOS device successfully measured amperometric spikes simultaneously from 76 electrodes out of 1024 electrodes in a single set of measurements (Fig. 9a). This is identified by manually monitoring the amperometric recordings from individual electrode-amplifier. Each spike corresponds to dopamine release from a single vesicle. The recorded data are read and demultiplexed using a custom-written MATLAB code. The amperometric data are then imported to Igor Pro 7 and analyzed using Quanta Analysis v8.20 [27]. In the representative measurements shown in Fig. 9b, vesicle secretions as small as 9.6 pA and as large as 1487 pA are observed, with an average amplitude of 132.4 pA. Within the 42 seconds of data, 333 quantal release events from this particular single cell are detected. The events from this cell exhibited an average half-width of 1.26 ms. To determine the number of released neurotransmitters, the quantal size can be

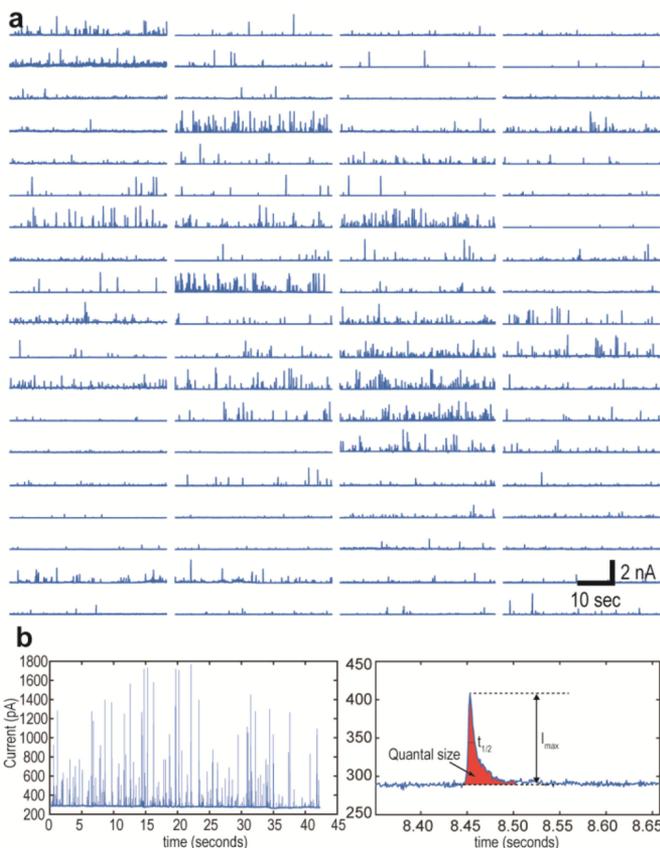


Fig. 9. (a) Parallel recordings of 76 single-cell vesicle secretions. (b) A representative recording shows individual spikes corresponding to single vesicle release of neurotransmitters.

found by integrating the current measured from each spike. For this cell the average quantal size is 0.288 pC, corresponding to the release of $\sim 900,000$ dopamine molecules per vesicle.

V. STATISTICAL ANALYSIS OF AMPEROMETRIC SPIKES

About 7147 vesicle secretions are detected from all 76 measurements. The characteristics of all measured spikes, including the half-width ($t_{1/2}$), maximum current (I_{max}), and amount of dopamine, are analyzed (Fig. 10). The average half-width is 1.63 ms with a standard deviation of 1.00 ms. With the 4.4-kHz bandwidth of the CMOS device, spikes with above 1-ms half-width can be measured reliably, however, faster spikes from rat ventral midbrain dopamine neurons, with 100–600 μs half-width, may be difficult to resolve using this CMOS device [28]. This observation is consistent with measurements from other neuroblastoma cell lines [5] and neurons [29], but the half-width from SH-SY5Y cells is significantly faster than that obtained for endocrine cells, such as PC-12 and bovine chromaffin cells [7], [30], [31]. The number of events varied from zero to 419 per cell, with 94 events per cell being the average. For the 76-cell measurements, the average amount of dopamine release from a single vesicle is 1.86 attomole, corresponding to $\sim 1.12 \times 10^6$ molecules per vesicle. The number of dopamine per vesicle in human blastoma SH-SY5Y cells is about 100 times larger than

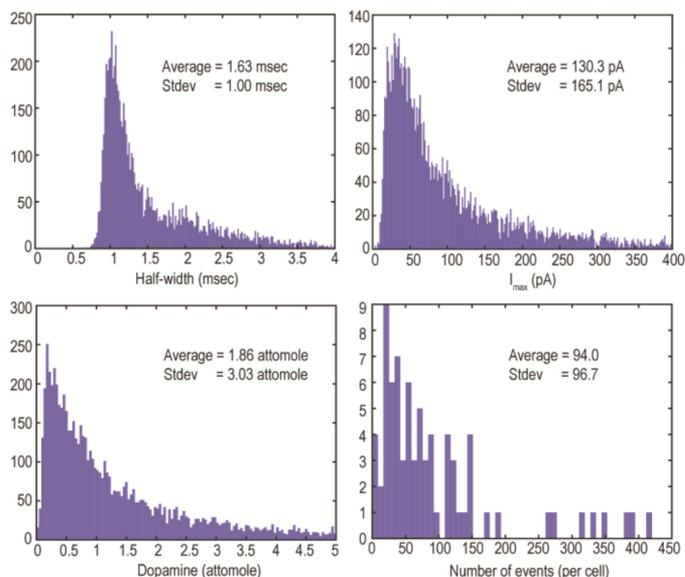


Fig. 10. The characteristics of vesicle secretions in human neuroblastoma cells, including half-width, maximum current, the amount of dopamine released, and number of vesicle release per cell.

that of rat ventral midbrain neurons [28], and is about 4 times less than that of bovine chromaffin cells [32].

VI. CONCLUSION

In this paper, we present a 1024-channel monolithic CMOS bioelectronics device, enabling high-throughput recordings of vesicle secretion from SH-SY5Y cells. Each electrode in the array, $15 \mu m \times 15 \mu m$ in size, has a dedicated TIA that has a small footprint of $30 \times 30 \mu m^2$ and fully addressable SRAMs to configure the sensors individually. The 1024-ch sensor array operates with a frame rate of 10,000 per second. We discussed in detail the device packaging, a completely in-house process that protects the wire bonds as well as pads, provides a reservoir to contain solutions, provides access to the electrode array on the surface of the device, and protects external electronics interfacing with the device. Monolithic integration of the gold electrodes and SU-8 single-cell traps to the surface of the CMOS bioelectronics is demonstrated to permit on-chip high-throughput single-cell amperometry. To demonstrate the feasibility of the device, SH-SY5Y cells are placed onto the sensor array to measure dopamine released from the cells after stimulation. Single-cell recordings of 76 cells and 7147 vesicle release events are captured in several minutes. This would have taken significantly longer, on the scale of months, to acquire using traditional instrumentations. The fine temporal resolution of the TIAs are able to capture the neurotransmitter secretions of the SH-SY5Y cells, which exhibited a fast half-width average of 1.63 ms. The presented system design enables high-throughput study of vesicle secretion at the single cell level through monolithic integration of an array of 1024 electrode-amplifier pairs with SU-8 single-cell traps, a biocompatible packaging process, and digital circuitry that enables 1024 parallel recordings

TABLE II
COMPARISON TO STATE-OF-THE-ART CMOS BIOELECTRONICS

Reference	[8]	[12]	[13]	[15]	This Work
Technology Node	0.5 μm	0.18 μm	0.13 μm	0.18 μm	0.35 μm
Die Size	3 mm \times 3 mm	5 mm \times 2.65 mm	3 mm \times 2 mm	12 mm \times 8.9 mm	5 mm \times 5 mm
Number of Electrodes	100	200	1024	59760	1024
Electrode Size	15 μm \times 15 μm	10 μm \times 10 μm	28 μm \times 28 μm	3 μm \times 7.5 μm	15 μm \times 15 μm
Electrode Material	Platinum	CNT Coated Gold (Current channels), Gold (Voltage Channels)	Gold	Platinum	Gold
Current Measurement Channels	100	200	4	28 ^a 32 ^b	1024
Noise performance (Current)	~ 100 fA _{RMS}	480 fA _{RMS} at 110 Hz filtered	56 pA _{RMS}	120 pA _{RMS} ^a 6.4 pA _{RMS} ^b	415 fA_{RMS}
Bandwidth (Current)	-	110 Hz - 10 kHz	700 Hz	16 kHz ^b	4.4 kHz
Accumulated Sample Rate (Current)	200 kS/s	200 kS/s	-	80 kS/s ^a	10 MS/s
Voltage Measurement Channels	-	200	4	2048	-
Noise performance (Voltage)	-	4.07 μV_{RMS} at 100 kHz	13 μV_{RMS}	4.4 μV_{RMS}	-
Bandwidth (Voltage)	-	1 Hz - 10 kHz	-	1 Hz - 10 kHz	-
Accumulated Sample Rate (Voltage)	-	200 kS/s	-	640 kS/s	-
ADC	16-bit off-chip	10-bit on-chip	16-bit off-chip	10-bit on-chip	16-bit off-chip
Total Power	-	3.21 mW	-	86 mW	12.5 mW

^a Neurotransmitter Detection

^b Impedance Measurement

at a rate of 10 kS/s/ch. The presented system design marks a significant advancement in regards to the field of single-cell electrophysiology, which is hindered by the low throughput of traditional methods. A comparison of the presented system design to recent state-of-the-art CMOS bioelectronics is presented in Table II. The device is demonstrated to provide improved benefit toward revealing the rich information regarding the dynamics of vesicle secretion and the underlying mechanisms of neurological diseases. For the study of neurological diseases and drug treatments that modulate neurotransmitter release, the presented device provides an excellent platform to obtain a significant amount of single-cell recordings to better arrive at statistically significant conclusions that must be established on the basis of a large number of measurements.

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