Harmonic Analysis for Quality of Service (HAQS)

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***Abstract* – The objective for this project is to develop a system capable of measuring the Total Harmonic Distortion of voltage and current waveforms provided by mains power outlets up to the fifty-first harmonic. The system will utilize a microcontroller to calculate the Total Harmonic Distortion and will be able to interface with single- and three-phase mains power outlets, both of which supply 120 VRMS at 60 Hz. This paper presents the design and verification methodology used to implement the sensor circuitry, analog-to-digital converter, microcontroller, and various peripherals, such as a liquid crystal display, a touch panel controller, and an SD card reader.**

***Index Terms* – Total Harmonic Distortion, Harmonic Analysis, Analog-Digital Conversion, Microcontroller, Voltage Measurement, Current Measurement**

I. Introduction

In an ideal scenario, a mains power outlet supplies a perfect 60 Hz sinusoidal power signal, free of harmonic content to distort it. However, these signals do not exist in realistic applications. As nonlinear components, such as diodes and transistors, were introduced into modern electronics, power signals became distorted with harmonic content. This occurs because the nonlinear elements draw currents that are not perfectly sinusoidal [1].

These distortions cause some of the transferred power to exist at harmonic frequencies of the fundamental, and the power transferred through these non-fundamental frequencies is unusable by the system. This power is, at best, useless and, at its worst, potentially destructive or damaging to the components within the device in question. Furthermore, harmonics can cause unreliable data transmission and interference with the operation of sensitive electronic equipment, such as medical devices [1] – [2].

The ability to measure the Total Harmonic Distortion (THD) of a mains power source will allow the user to evaluate an outlet's fitness for use. Mathematically, THD is calculated in the following manner:

$$THD = \sqrt{\sum_{n=2}^{\infty} \left(\frac{H_n}{H_1}\right)^2} * 100. \tag{1}$$

Practically, a high THD reading will indicate that an outlet is functioning in such a way that can be harmful to any device that interfaces with it. Furthermore, it allows a consumer, for instance, to evaluate how much of the power they are purchasing from utility companies is, in fact, usable at the fundamental frequency. Developing a system that is capable of measuring both single- and three-phase THD increases the utility of the product by expanding its ability to evaluate outlets more commonly used in large-scale and industrial applications.

With regards to the specific design requirements for HAQS as imposed by Texas Instruments (TI), the system must incorporate a microcontroller (MCU) to show the harmonic content of the input voltage and current waveforms up to the fifty-first harmonic. After digitizing and processing the inputs, the MCU will calculate the THD and display the harmonic content and THD for each input on a liquid crystal display (LCD). A touchscreen LCD was chosen for HAQS to save space by combining the display and User Interface (UI).

The system block diagram for HAQS illustrates how the individual elements discussed in this document are connected and is shown in Fig. 1.

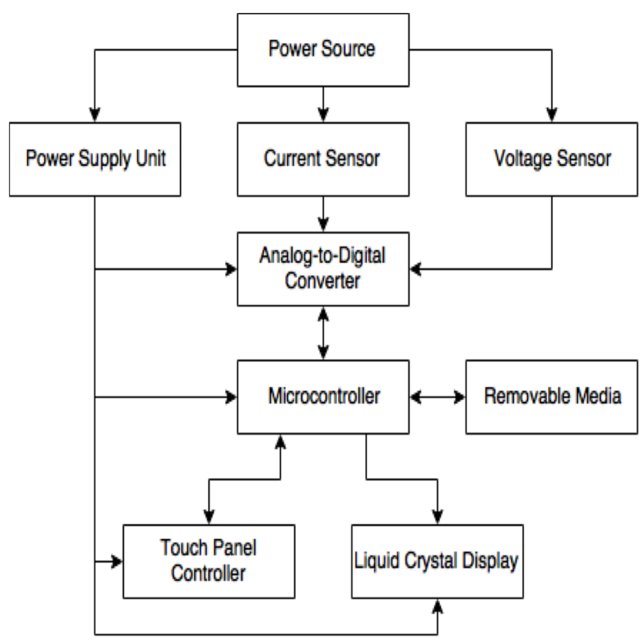


Fig. 1. HAQS System Block Diagram

II. Analog Design

A. Power Supply Unit

The design of the Power Supply Unit (PSU) will depend largely on the voltage and power requirements of the individual components in the system. Using a power flow diagram to map these requirements, we obtained the PSU design parameters listed in Table 1.

TABLE 1
POWER SUPPLY UNIT REQUIREMENTS

Parameter	Value
Input Voltage	120 VAC
Outputs Voltage(s)	3.3 VDC, ±2.5 VDC
Power Supplied	5 W
+3.3V Regulator Current	1.2 A
+2.5V Regulator Current	100 mA
-2.5V Regulator Current	100 mA

We derived the parameters in Table 1 using worst-case scenarios to ensure that even abnormal voltage spikes or inrush currents would not adversely affect the operation of the PSU.

The goal of the primary stage of the PSU is to reduce the incoming single-phase mains AC voltage and convert it to DC voltages. For the primary stage, we used Texas Instruments' PMP8477 design, which offers 10 W of power with a +5 VDC output. The PMP8477 features a flyback controller and Primary-Side Regulation (PSR), which is typically employed when size and efficiency are of special concern [3].

We selected a design with a flyback controller for its ability to handle high voltages efficiently for low-power applications. Though the secondary side of the flyback circuit required some filtering in order to reduce the ripple current associated with the use of the flyback controller, the design remained compact [4]. The flyback topology, combined with the use of PSR and relative simplicity of the circuit, make the PMP8477 design particularly useful for HAQS.

Following the primary stage, we connected the +5 VDC output of the PMP8477 to three different voltage regulators in parallel in order to achieve the voltages needed to power the system. Table 2 lists the regulators chosen to provide the necessary voltages for the system.

TABLE 2
VOLTAGE REGULATOR SELECTIONS

Regulated Voltage	Regulator Selected
+3.3 VDC	TPS2085SILR
+2.5 VDC	LM3671TLX-2.5/NOPB
-2.5 VDC	LM5088MH-2/NOPB

We selected the regulators in Table 2 for the secondary voltages based on the voltage and power needs of the components interfacing with each regulator as well as power supply simulations from Texas Instruments' WEBENCH tool.

Regarding the PSU printed circuit board (PCB), we implemented several design considerations to ensure reliable and safe operation. On the primary side of the PSU, we removed the ground pour to avoid the inductance of noise in the ground plane by the high-voltage input. We kept all ground traces and pours a minimum of 50 mil away from any trace carrying high voltage. Additionally, the maximum amount of current flowing through a trace in a worst-case scenario also affected the final design. On the primary side, the maximum current is 500 mA; anything more than that will burn the input fuse. Thus, we selected 16 mil traces, which can carry up to 1.2 A. On the secondary side, which includes the various voltage regulators, the maximum possible current is 2 A, according to the power flow diagram and the specifications of the PMP8477. We selected 32 mil traces on the secondary side in order to accommodate the higher current. The PSU is self-contained on one of the two PCBs included in the final design of HAQS.

B. Analog-to-Digital Converter

The requirement to analyze three-phases of current and voltage up to the fifty-first harmonic drove the analog-to-digital converter (ADC) selection process. The basic requirements for the ADC are included Table 3 [5].

TABLE 3
ANALOG-TO-DIGITAL CONVERTER REQUIREMENTS

Parameter	Value
Architecture	Sigma-Delta
Minimum Sampling Frequency	6120 Hz
Number of Input Channels	6
Input Type	Differential
Resolution	≥20 bits

We selected the TI ADS131E08 for this project due to its resolution, Sigma-Delta architecture, sampling rate flexibility, and sufficient number of differential inputs.

Based on how the ADC references analog input voltages to convert data, the 24-bit resolution of the ADS131E08 offers a quantization step of 286 nV. Such a level of accuracy is of utmost importance for this project, but it also places more emphasis on noise reduction and limitations, as even a small amount of noise can render the least significant bits of the digitized data as useless. In addition, being able to sample all six waveforms using differential inputs will improve the accuracy of the THD measurement by reducing noise [6].

The Sigma-Delta architecture is preferable for HAQS due to its typically high resolution and noise-reducing features. Sigma-Delta ADCs sample at rates significantly higher than the input signal. The Nyquist Sampling Theorem states that the sampling frequency must be twice the frequency of the input, but Sigma-Delta ADCs typically sample at, at least, twenty times the frequency of the input. The act of oversampling the input spreads the quantization noise across a broader range of frequencies. A digital filter then removes noise beyond the frequency of the input signal [6].

Oversampling works in tandem with a process known as noise shaping. Oversampling distributes the quantization noise, but noise shaping shifts the noise to higher frequencies by summing the error voltage with an integrator; this is what makes Sigma-Delta ADCs useful for low-frequency applications that require high accuracy—like HAQS. Using the digital filter mentioned before now has an increased effect, as the noise has been shifted deeper in the rejection region of the filter. Noise reduction measures such as these are valuable to HAQS in order to keep the final THD readings accurate.

As previously state, in order to fulfill the Nyquist Sampling Theorem, the ADC will need to sample at twice the bandwidth of the signal. The ADS131E08 outputs sampled data at several preprogrammed rates. The lowest rate that fulfills the Nyquist Sampling Theorem is the 8 ksps setting; thus, for a bandwidth of 3060 Hz, the ADC will output sampled data at 8 ksps.

It is important to note that the 8 ksps setting does not dictate the actual sampling rate; however, it defines the Over-Sampling Ratio (OSR). The 8 ksps setting sets the OSR to 128. This is important for controlling how the Fast Fourier Transform (FFT) bins the frequencies of the signal it is analyzing. Using a sampling frequency of 8 ksps with 256 samples creates a bin at 62.5 Hz, which will artificially inflate the final THD reading due to the bin not being at the fundamental frequency of 60 Hz. Using the OSR, we determined that we could change the system clock frequency to then change the sampling frequency and, ultimately, the frequencies at which bins are created. Using a 1.966080 MHz programmable oscillator as the system clock for the ADS131E08 changed the data rate to 7680 ksps, which allowed us to achieve a bin size of 30 Hz with 256 samples or 15 Hz with 512 samples. Sampling at 7680 ksps still adheres to the Nyquist Sampling theorem, but it also provides a bin at 60 Hz and its harmonic frequencies.

Adjusting the data rate also addressed the issue of coherent sampling. With the stock clock frequency, a windowing function would have been required to make up for the fact that the ADC was not sampling an integer number of periods. Using the new clock frequency, HAQS is coherently sampling the input, increasing the accuracy of the system and eliminating the need for a windowing function.

To address the noise issue previously mentioned, TI recommends the use of an array of filtering capacitors on the inputs and voltage supply lines. The use of 0.1 μF and 1.0 μF capacitors on the supply lines and reference voltages will help reduce noise. Noise reduction measures for the inputs are incorporated into the voltage sensing circuits.

Because the voltages interfacing with the ADC are bipolar, and due to how the input voltages are referenced against the supply voltages, we must include +2.5 VDC and -2.5 VDC rails in the final design for the AVDD and AVSS supplies, respectively. This will allow the system to sample the full range of the voltage and current waveforms without any clipping.

C. Voltage Sensing Circuit

We designed the voltage sensing circuit to measure the voltage of a Wye-connected three-phase power source, as well as a common single-phase power source. The circuit is based on the voltage divider topology and includes a varistor for protection purposes, two ferrite beads and a low-pass filter to fulfill the role of an anti-aliasing filter.

In designing the sensors, we must consider several parameters regarding the ADC, such as voltage and current input limitations, the bandwidth of the input signal, and the sampling rate. These parameters, which will guide the design of the voltage sensors, are included in Table 3 [5].

TABLE 3
VOLTAGE SENSOR DESIGN REQUIREMENTS

Parameter	Value
ADC Input Voltage	$\pm V_{ref}/gain = \pm 2.4V$
ADC Input Current	10mA
ADC Max Sampling Rate	64 ksps
Desired -3dB Bandwidth	3060 Hz
Mains Voltage	120VRMS (170V_{pk})

We selected the resistor values for the voltage divider first. The divider ratio provides an output swing of 1 V_{pk} to allow the meter to continue taking samples in the event of a voltage surge not exceeding the breakdown voltage of the varistor. Choosing a 1 MΩ resistor limits the current, as well as the power dissipation, through the divider. Furthermore, choosing to use three 332 kΩ resistors in series distributes the power dissipation evenly across the three resistors, instead of burdening a single resistor.

Ideally, a 5.9275 kΩ resistor is required to achieve an output of 1 V_{pk}. However, 5.9 kΩ resistors are readily available and provide an output of 0.944 V_{pk}. A voltage divider using these two resistor values will reduce the output voltage and current to levels that the ADC can safely handle.

The low-pass filter follows the voltage divider. The desired bandwidth is 3060 Hz in order to measure up to the fifty-first harmonic of the voltage and current waveforms; thus the low-pass filter is configured with a cutoff frequency of 4.3 kHz. Components with tight tolerances are preferred for both sensor circuits in order to maintain the integrity of the design.

The final step for the voltage sensor design is to ensure that the current into the ADC is within its tolerable range. Using a simulation, it was determined that a maximum voltage of 170 V will produce approximately 5 nA of current into the ADC, which is well within the 10 mA maximum input current specification of the ADS131E08, even in the event of a voltage spike.

D. Current Sensing Circuit

We designed the current sensing circuit for HAQS to measure the currents of each individual phase of the Wye connected three-phase power source that is available for testing purposes. The sensor employs the use of a current transformer to produce an AC current from the sensed current at the primary of the transformer. The current from the transformer induces a voltage across a burden resistor, which allows the system to measure the harmonic content of the current provided by the outlet to a load.

In addition to the current transformer and the burden resistor, the current sensor consists of a system of high-speed switching diode, a TVS diode for protection, a low-pass filter to fulfill the role of an anti-aliasing filter.

Given that the power outlets with which HAQS will be interfacing can deliver up to 60 A, the current transformer chosen for the final design must be able to accommodate such a load. We selected the Copal Electronics C-CT-10 for HAQS, as it can handle the maximum output current from the outlet and has a bandwidth that is sufficient for capturing the fifty-first harmonic of the signal.

Unlike the voltage sensor, the current sensor is electrically isolated from the power source and the power dissipation relative to the system's load is not a design concern. However, the current sensor must still adhere to the design constraints imposed by the ADS131E08, as listed in Table 3 [5].

With a maximum current of 60 A and the transformer's 3000:1 ratio in mind, we selected a burden resistor of 60 Ω so that a 1.697 V_{pk} waveform is delivered to the ADC.

As with the voltage sensor, the bandwidth of the low pass filter for the current sensor is 4.3 kHz, which will keep attenuation at the fifty-first harmonic to a minimum.

III. DIGITAL DESIGN

A. Microcontroller

When selecting a MCU, we prioritized finding a low-power option. TI offers a wide variety of MCUs, but the MSP line in particular specializes in low-power operation. Processor speed was a secondary concern. Due to the nature of the calculations that HAQS will perform, it was important to find a MCU that could perform the entire analysis operation in a reasonable amount of time. It is worth noting that the concern for a low power system did take precedence over having a fast system. Other considerations included the communication schemes, compatible programming languages, and number of GPIO pins.

With these criteria, and with a recommendation from TI, we selected the MSP432P401R for HAQS, as it is the most robust of the MSP43x options and best fits the requirements for the system. The specifications for the MSP432P401R are listed in Table 4 [7].

TABLE 4
MSP432P401R SPECIFICATIONS

Parameter	Value
Clock Speed	48 MHz
Volatile Memory	256 KB
RAM	64 KB
GPIO Pins	84
Maximum Power Consumption	330 mW
Architecture	32-bit

In addition to being a capable and power-efficient solution, the MSP432P401R is available in the form of a LaunchPad. The availability of a LaunchPad for prototyping and testing purposes adds to the value and incentive to use this particular MCU.

The MSP432P401R is outfitted with several different types of communication channels. The majority of the system's components are able to communicate with the MCU via SPI. However, the touch panel controller requires I^2C. The communication and procedural software is written in C programming language.

The MCU is incorporated into the Sensor Board, which includes the components not associated with the PSU. Typical design measures were taken in order to ensure that the Sensor Board operates as intended. Some of these measures include separating the analog and digital grounds, filter capacitors, making use of ground and voltage pours, and the reduction of unnecessary traces and trace lengths.

The MCU is powered by the +3.3 VDC rail from the PSU. Both the analog and digital supplies are tied to the same voltage, as specified by the datasheet [6].

We were able to program the MCU on the final Sensor Board by leveraging the ARM device debugger on an extra MSP432P401R LaunchPad. Jumping the debugging pins from the LaunchPad to the JTAG pins on the HAQS Sensor Board flashed the software to the MCU and allowed debugging without the aid of a dedicated ARM debugger.

B. Liquid Crystal Display

Because we purchased the LCD unit as a complete package, the only design associated with it is the physical and software interfaces and the construction of the Graphical User Interface (GUI).

In order for the MCU to be able to connect and communicate with the LCD, we included an eight-pin connector to host the SPI lines. Otherwise, the circuity for the LCD is self-contained on the unit, simplifying the PCB design process.

The GUI for HAQS is dynamic and flexible. After loading the firmware, the user has the option to operate in single- or three-phase modes, depending on the outlet under test. A mockup of the GUI is illustrated in Fig. 2.

Pressing the "Analyze" button on the home screen initializes the sampling and analysis process. After the analysis is complete, the harmonic content of the first voltage phase is displayed on the screen. Touching the arrows on either side of the graphing area allows the user to scroll through the sampled bandwidth and see harmonic content up to the sixty-fourth harmonic. Touching the graphing area zooms in on the graph and displays the frequencies on the x-axis and the exact magnitude of the harmonic content at a given frequency on the y-axis. The THD is calculated and displayed on the screen as well.

The user can switch between the three voltage and three current phases by pressing the "Source Type" and "Phase" buttons on the left side of the Results screen and can save the data displayed to an SD card by pressing the "Save" button. Pressing the "Save" button writes an ID, the THD, and the harmonic content of the analyzed signal to the SD card. Back on the home screen, the "Lock" button puts the LCD in an inactive state to save power.

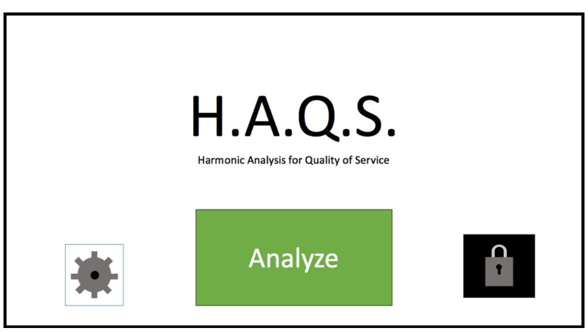


Fig. 2. HAQS Home Screen GUI, providing the user with the ability to change the analysis settings, put the display to sleep, or begin the sampling/analysis process

C. Touch Panel Controller

The touch panel is the means by which the user controls the system. We opted for a touchscreen LCD over physical UI (such as buttons) in order to save space on the enclosure and create a more intuitive control system.

Unlike the other components of HAQS, the touch controller uses I^2C communication, instead of SPI. The inclusion of a ZIF connector on the Sensor Board was required to physically connect the touch controller to the MCU.

III. Software Development

The system's execution with respect to the MCU begins with initialization of communication with all peripheral devices and creation of necessary storage arrays used for sampling. The main loop then runs, continually polling the touch controller until a touch is detected. The touch position is calculated and appropriate actions are performed if the position is within the bounds of a button. These actions could be anything from displaying the settings screen to scrolling through the results of an analysis. The intended process flow of the system is detailed below.

The user will begin by opening the settings screen and selecting the analysis mode they wish to use. The system is set to Single Phase Analysis by default. The user will return to the main menu and touch the "Analyze" button. Then, the system will sample the signals from the voltage and current sensors and perform an FFT on the recorded samples. The results are displayed graphically to the user on the Results screen. From this screen, the user can choose which spectrum they would like to view—voltage or current, and which phase.

We implemented our own FFT algorithm to save on code size and execution time. Our implementation was developed and tested prior to any physical components being available to us using the CodeBlocks development environment. The algorithm was later incorporated into the Code Composer Studio project used to program our MCU and tested by outputting results through our SD card reader. This test and future tests were performed using a function generator to create the signal to be sampled. It was then tested by outputting results to the LCD screen graphically as intended in the final design.

Implementing SPI and I^2C communication programmatically involved the use of TI's DriverLib library. For each peripheral device, we defined the functions device_SPI_receive() and device_SPI_send() which sent and received a byte of information using the transmit and receive buffers of the associated communication channel on the MCU. DriverLib functions for initializing the communication channel and setting its clock signal are called for each peripheral device. To communicate with our touch controller through I^2C, a similar process was used but with several transmission functions having more overhead than others. Both SPI and I^2C communication implementations were tested and debugged using a logic analyzer.

The SD card within the system contains one file which is maintained in a certain way to ease the usage of the file. The first sector of the file is kept as a header that stores the number of sectors into the file the system has written to last as well the number of bytes into that sector. This allows the system to make effective use of a Petit FatFs library to seek to the last byte written to and further record results. The file is saved as a .CSV extension so it can be viewed in Excel or a Notepad program for later inspection.

IV. Testing and Results

We prototyped HAQS using the various evaluation modules, LaunchPads, and BoosterPacks offered for the components we selected. This simplified and quickened the prototyping process by allowing us to explore each component without the need to design our own evaluation modules. Working with these pieces of equipment, we were able to arrive at a working prototype, which accomplished all functions of HAQS as intended. Following the prototype, we started the design of our own boards and interfaces. After receiving the components and other hardware, we assembled the final system.

The first step to testing HAQS is to verify that the PSU provides the proper voltages at its outputs. We populated the primary side of the PSU first to confirm that the 120 VAC from the outlet is safely reduced to a clean +5 VDC. We then populated the three voltage regulator circuits and used a DMM to read the +3.3 VDC, +2.5 VDC, and -2.5 VDC outputs.

With the PSU board completed, we started the verification process for the Sensor Board. After population, each individual subsystem was tested to verify the design and implementation. These tests are detailed in the following sections.

A. Voltage Sensors Testing and Verification

The process below details the testing and verification process for the voltage sensors.

1. Using a function generator, apply a 60 Hz, 20 V_{pp} input to the three voltage sensors to confirm that the voltage dividers are operational. The output should be 117 mV_{pk}.
2. Apply a 4.3 kHz, 20 V_{pp} input to the three voltage sensors to confirm that the anti-aliasing filters are operational. The output at this frequency should be 82 mV_{pk}.
3. Connect a mains power outlet to the voltage sensors to confirm that the board can handle and reduce the high voltages without any issues. The output should be 1 V_{pk}.

B. Current Sensors Testing and Verification

For the sake of testing and verification, we constructed an external current sensor to examine how the response to a voltage input from a function generator. First, we applied the current transformer setup to the external sensor to confirm that the circuit is able to generate a current and a voltage using the current transformer; then we tested the sensor with voltage inputs from a function generator. After establishing a baseline for comparison, we applied the same inputs to the onboard current sensors. The process used to verify the current sensors is included below.

1. Using a function generator, apply a 60 Hz, 4 V_{pp} input to the three current sensors to confirm that the voltage dividers are operational. The output should be 4 V_{pp}.
2. Apply a 4.3 kHz, 4 V_{pp} input to the three voltage sensors to confirm that the anti-aliasing filters are operational. The output at this frequency should be 2.82 V_{pp}.

C. Liquid Crystal Display Testing and Verification

Due to the fact that testing and verifying the MCU as its own subsystem is difficult and tedious, we verified the MCU in conjunction with the peripherals with which it interfaces. We chose to test the LCD first. After flashing the code to the onboard MCU, we connected the LCD to the Sensor Board. The LCD immediately turned on and displayed the loading screen associated with the initialization sequence of the system, thus confirming that the MCU was flashed correctly and that the MCU and LCD were communicating as intended.

D. Touch Panel Controller Testing and Verification

We verified the touch panel controller in a similar way. After connecting the MCU to the controller, we confirmed that the entire system could be controlled with the GUI on the LCD and that all regions of the panel responded appropriately to the user's touch.

E. Removable Media Testing and Verification

TABLE 5
HAQS PROTOTYPE TEST RESULTS

Input Type	Theoretical THD	Measured THD	Percent Error
60 Hz, 20 V_{pp}, Sinusoidal	0%	0.01%	1.25%
60 Hz, 20 V_{pp}, Square	48.3%	45.73%	3.98%
60 Hz, 20 V_{pp}, Sawtooth	80.3%	77.16%	2.52%

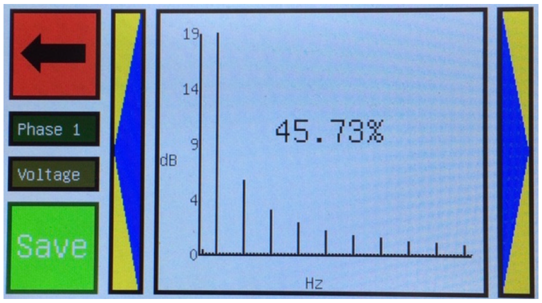


Fig. 4. HAQS voltage THD analysis result with a 60 Hz, 20 V_{pp} square wave input provided by a function generator

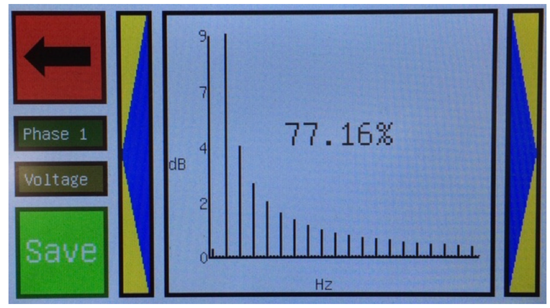


Fig. 3. HAQS voltage THD analysis result with a 60 Hz, 20 V_{pp} sawtooth input provided by a function generator

We tested the SD card by using the MCU to write a line of data to the file on the card, then moving the card to a reader on a personal computer to verify that the information was written correctly. We ran consecutive tests to ensure that new data could be written without affecting or overwriting old data.

Later tests confirmed that the MCU could correctly write data associated with the analyses to the SD card. These tests confirmed that the MCU and SD card were communicating properly and ensured that the data saved by the user would remain on the card, even after multiple analyses.

F. System Testing and Verification

After testing and verifying the individual subsystems of HAQS, we assembled the complete system and exposed it to a number of test signals, both ideal and non-ideal, in order to verify that the input waveforms were being digitized and processed correctly and that the THD measurements were accurate. The final test is to confirm that the ADC and MCU are operating and communicating correctly.

The test procedure for the system was consistent for all of the tests listed in Table 5 and is as follows:

1. Assemble the system and connect the appropriate peripherals, including function generators and oscilloscope.
2. Use HAQS to measure the harmonic content of the input signal.
3. Compare the measurement provided by HAQS to the ideal case (if applicable) and to the THD provided by data read from an oscilloscope to verify results. In addition, compare these values to those provided by TI's ADS131E08EVM-PDK software package, which can also measure THD.

The third step in the process above provides two reliable points of comparison for the THD measurement provided by HAQS. Using the ADS131E08EVM-PDK software and an oscilloscope with an FFT function, we were able to determine how the data provided by HAQS compares with other THD-measuring systems and the overall accuracy of our product.

It is important to note that the Theoretical THD referenced in Table 5 is calculated using an infinite number of harmonics. HAQS only uses the first sixty-four harmonics in its calculations; thus, it is expected that the value HAQS provides is less than the Theoretical THD value.

To remedy the discrepancy, an oscilloscope with a FFT function was used to verify the results. The first nine harmonics were used to calculate THD values by hand using (1) to compare the results provided by HAQS and the data provided by the oscilloscope. These values were used to calculate the Percent Error

Over the course of many tests to prove reliability, the system behaved as expected and repeatedly produced accurate results. Samples of the outputs provided by HAQS are shown in Fig. 4 and Fig. 3

V. Conclusion

In conclusion, the design process described in this document resulted in a successful product that meets or surpasses all requirements set at the beginning of the project. The original plan was to implement a system that could read the first fifty-one harmonics and report the Total Harmonic Distortion of the signal on a seven-segment LCD. Instead, the team delivered a low-power meter that can read harmonic content up to the sixty-fourth harmonic, display the harmonic content of the signal in graphical form, and interface with both single- and three-phase power outlets, all while allowing the user to utilize and navigate the system using a touchscreen LCD. After thoroughly testing the accuracy and reliability of the final product, the process is complete.

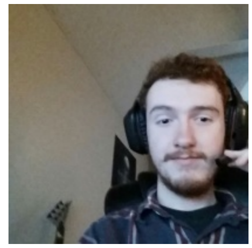
Acknowledgement

The idea for this project originated from Texas Instruments. The team wishes to acknowledge Texas Instruments for proposing the base idea for this project and to thank them for their sponsorship. We would also like to thank Dr. Chung Yong Chan for his assistance and support throughout the course of this project and Mr. Don Harper for his assistance during the construction of the final product.

Biography

Brian Angiel is a senior electrical engineering student at the University of Central Florida and will graduate in the spring semester of 2016. His interests involve audio equipment, consumer electronics, and building guitar equipment as a hobbyist in his free time. Brian worked at Lockheed Martin as a College Work Experience Student for two years during his undergrad education in both systems and electrical engineering. Following graduation, he will begin his career as an electrical engineer at Texas Instruments.

Nick Hellenbrand is a senior electrical engineering student at the University of Central Florida and will graduate in the spring semester of 2016. His interests involve consumer electronics and working with digital/analog circuits.



Louis Hofer is a senior computer engineering student at the University of Central Florida who will graduate in the spring semester of 2016. His interests involve the application of artificial intelligence techniques and SOLID object oriented development. Following graduation, he will begin graduate studies at the Florida Interactive Entertainment Academy with a focus in artificial intelligence for game design.

Kevin White is a senior electrical engineering student at the University of Central Florida and will graduate in the spring semester of 2016. His interests involve analog/digital signal processing and signal processing applications. Following graduation, he will begin graduate studies at the University of Central Florida with a focus in circuit design for bioelectronics.

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