# PnPal – Pick and Place with Acoustic Levitation

Senior Design 1 Final Report


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# Chapter 1: Executive Summary

The revolution in highly automated, precision-oriented industrial systems has necessitated the development of advanced robotic solutions capable of operating across diverse environments. This is especially true with pick-and-place systems for circuit board assembly. Traditional pick-and-place systems primarily rely on vacuum nozzles or pneumatic grippers, face inherent limitations when handling miniaturized components, including mechanical damage, placement inaccuracies due to “stiction”, and contamination from physical contact. This report details the development of the PnPAL (Pick-and-Place with Acoustic Levitation), a novel system designed to achieve contactless component manipulation through the application of ultrasonic phased arrays.

The core innovation of PnPAL is its modular architecture, designed as a platform-agnostic end-effector that can be integrated into existing CNC or 3D printer infrastructures. By utilizing standard mounting interfaces and universal communication protocols, the system allows for the conversion of common Cartesian gantry frames into high-precision, contactless assembly stations. This approach significantly lowers the barrier to entry for small-scale laboratories and prototype facilities that require industrial-grade SMT placement without the capital expenditure of dedicated machinery.

The system utilizes a custom-designed 72-transducer array operating at a center frequency of 40 kHz. Through the real-time manipulation of acoustic phase delays, the system generates three-dimensional pressure minima – known as acoustic traps – based on the principle of the Gor’kov potential. These traps can secure and maneuver components such as 0603 and 0805 resistors, with a target placement accuracy of +- 0.5 mm. The control logic is executed on an ESP32 microcontroller, leveraging a dual-core architecture to synchronize high-speed signal generation with G-code parsing and motion coordination.

The documentation covers the current, full engineering lifecycle of the PnPAL system, beginning with the theoretical physics of acoustic radiation pressure and the comparative research of ultrasonic emitter and driver architectures. The hardware design section details the implementation of high-voltage driver circuitry and multi-layer PCB layouts optimized for noise mitigation. Subsequent chapters describe the software framework, including the development of the phase-shift algorithm and the FreeRTOS task allocation required for deterministic real-time control.

The project concludes with a comprehensive validation phase, documenting subsystem verification and potential integrated trials on a standard 3D printer frame. These tests confirm the system’s ability to maintain trap stability during gantry acceleration and achieve reliable component placement. The PnPAL system demonstrates a scalable, contactless solution for modern electronics assembly, providing a robust technical foundation for the future of modular automated manufacturing.

# Chapter 2: Project Description

## *2.1 Project Motivation and Background*

The manufacturing of modern electronics relies heavily on Surface-Mount Technology (SMT), where micro-sized components are placed onto Printed Circuit Boards (PCBs) before being soldered. As the industry pushes toward extreme miniaturization, standard components like 0402 and 0201 have taken over. Traditionally, these components are handled by vacuum-based pick-and-place (PNP) machines. However, these systems face a “contact barrier.” Vacuum nozzles can apply excessive mechanical pressure, leading to component cracking, or suffer from “stiction,” where the component remains stuck to the nozzle due to surface tension or static electricity, causing placement errors.

The PnPAL (Pick-and-Place with Acoustic Levitation) project was conceived to overcome these mechanical limitations through the use of ultrasonic standing waves. By utilizing a phased array of transducers, the system generates a local pressure minimum – an “acoustic trap” – that can suspend an SMT component in mid-air. This contactless manipulation eliminates the risk of physical damage and contamination.

Furthermore, the project addresses the economic barriers to entry for high-precision assembly. Industrial-grade PnP machines often cost tens of thousands of dollars, making them inaccessible for independent researchers, hobbyists, and small-scale prototype labs. By pivoting the PnPAL design into a modular end-effector, the system becomes a platform-agnostic tool. It is designed to be attached to the gantry of a standard, low-cost FDM 3D printer. This allows to leverage existing motion-control infrastructure to perform high-tech, contactless electronics assembly at a fraction of the cost of dedicated machinery.

## *2.2 Goals and Objectives*

The primary objective of the PnPAL project is the development of a self-contained, high-precision acoustic levitation end-effector designed for seamless integration with existing 3D printer architectures. By leveraging the mechanical rigidity and motion control systems of consumer-grade Cartesian gantries, the project aims to democratize access to contactless SMT assembly. The objectives are centered on achieving a high degree of interoperability, ensuring that the PnPAL head can function as a “plug-and-play” upgrade that transforms a standard fabrication tool into a specialized micro-assembly station.

To provide a clear roadmap for development and validation, the project goals have been categorized into three tiers of complexity. This structured approach ensures that the fundamental requirements of contactless manipulation are met before moving toward advanced automation and experimental features.

*Basic (Core Functionality)*

- Universal Mounting: Secure mechanical attachment to standard NEMA 17 carriage plates using a modular housing design.
- Static Levitation: Successful generation of a 40 kHz standing wave capable of suspending an 0805 resistor in a fixed position.
- Power Integration: Ability to draw stable power from 12V or 24V DC rails without interfering with the host machine's electronics.

*Advanced (Operational Precision)*

- Dynamic Movement: Maintenance of a stable acoustic trap during gantry travel at velocities up to 25 mm/s and accelerations of 250 mm/s^2.
- G-Code Interpretation: Real-time parsing of standard G0/G1 commands to coordinate the focal point with gantry coordinates.
- Placement Accuracy: Achievement of a repeatable placement tolerance of +- 0.5 mm on a target PCB footprint.

*Stretch (System Optimization)*

- Computer Vision Integration: Implementation of a lightweight edge-detection algorithm to verify component orientation before placement.
- Complex Geometry Handling: Successful levitation of non-rectangular components, such as SOT-23 transistors or small LEDs.
- Adaptive Path Planning: Software logic that automatically adjusts focal point height (Z-offset) based on real-time feedback from the printer's bed-leveling sensor.

### *2.3 Requirement Specifications*

**Table 2.1: Overall System Specifications**

| **Specification** | **Description** | **Target Value and Unit(s)** |
|---|---|---|
| Placement Accuracy* | The deviation between the target location on the PCB and the final placed position. | +- 0.5 mm |
| Cycle Time* | The total time taken for one complete pick and place operation. | $\leq 15\ seconds$ |
| Power Consumption | The total power drawn by the entire system under full load. | $\leq 200\ W$ |
| Noise Level | The maximum sound level generated by the ultrasonic transducers. | $\leq 85\ dB$ |

| | | |
|---|---|---|
| Dimensions | The overall footprint of the machine. | 60 x 60 x 45 cm |
| Levitation Capacity | The maximum weight of a component that can be levitated. | $\leq 10\ grams$ |
| System Reliability* | The percentage of successful pick and place operations out of a total of 100 trials. | ≥95% |

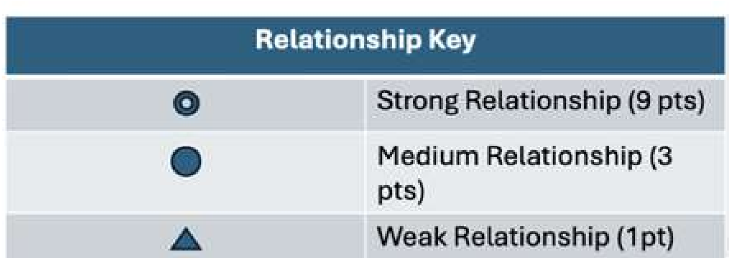
****Demonstrable Specifications:** Placement Accuracy, Cycle Time, System Reliability

**Table 2.2: Component Specifications**

| **Component** | **Parameter** | **Target Value and Unit(s)** |
|---|---|---|
| Microcontroller | Processing Speed | $\geq 100\ MHz$ |
| Ultrasonic Transducer | Frequency Range | $38-42\ kHz$ |
| Stepper Motors | Positional Resolution | $0.01\ mm/step$ |
| Gantry Rails | Backlash | $\leq 0.05\ mm$ |
| Camera Sensor | Resolution | $\geq 5\ Megapixels$ |
| Power Supply | Output Power | ≥250 W |
| Motor Drivers | Rated Current | $\geq 2\ A/phase$ |

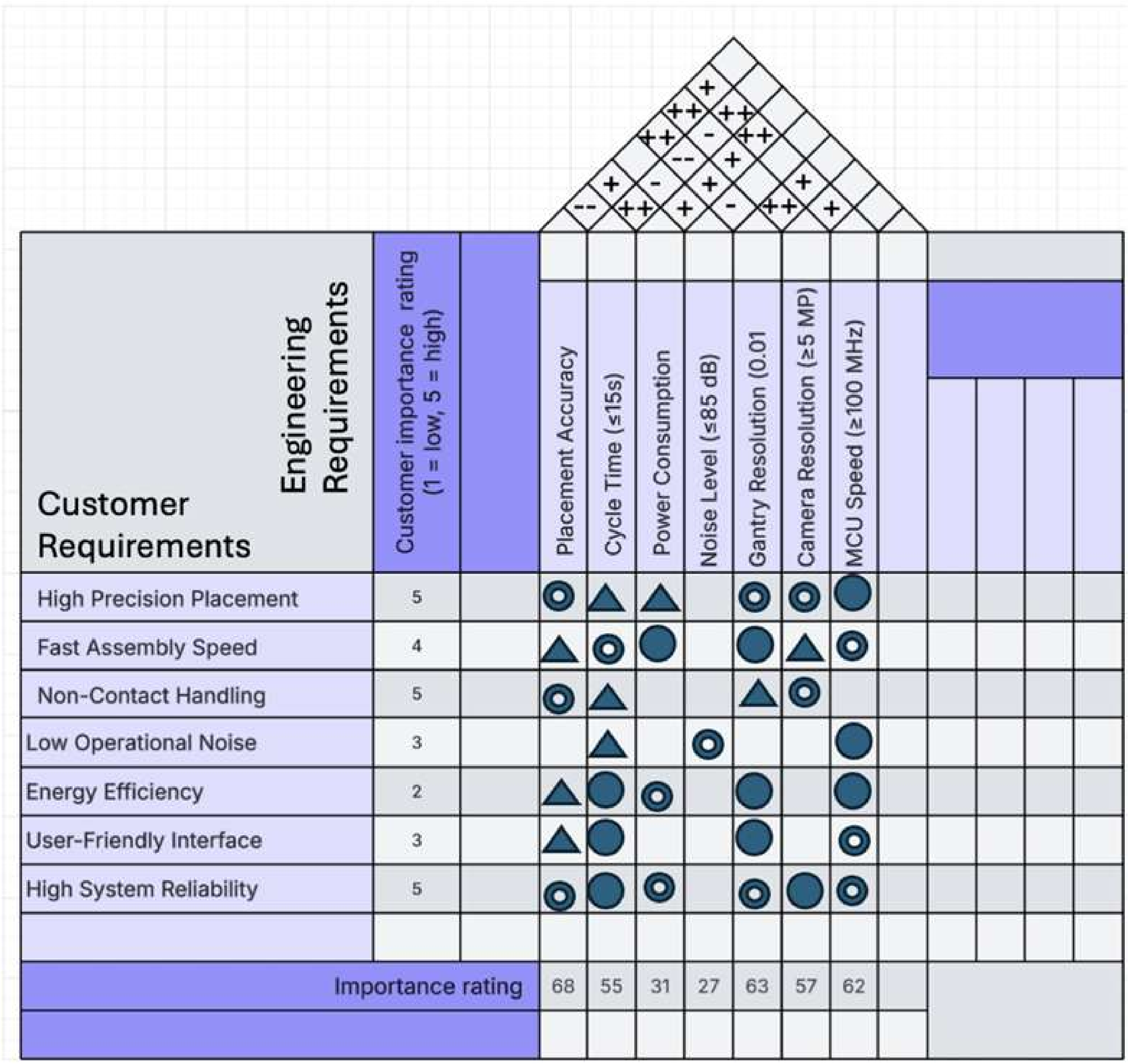
A House of Quality (HoQ) matrix was developed to formally link customer desires (e.g., "fast assembly," "non-contact handling") to our engineering specifications. This will help us prioritize which engineering requirements, such as "cycle time" and "levitation" capacity," have the most significant impact on the final product's success.

**Figure 2.1: House of Quality Relationship Key**



| Interrelationships Between Engineering Characteristics | |
|---|---|
| ++ | Strong Positive Relationship |
| + | Weak Positive Relationship |
| - | Weak Negative Relationship |
| -- | Strong Negative Relationship |
| | No correlation |

**Figure 2.2: House of Quality**



### *2.4 Physical and Functional Overview*

The PnPAL system functions as a "smart end-effector." Mechanically, it consists of a 3D-printed enclosure that houses the 72-transducer array and the driver electronics. Functionally, the device sits on the X-axis carriage of a donor 3D printer frame.

The operational workflow begins when the user uploads a G-code file containing the coordinates of the components. The ESP32 parses these coordinates and coordinates with the printer's gantry. As the gantry moves to the feeder location, the PnPAL head energizes the transducers to create a trap. Once the component is secured, the head signals the gantry to move to the PCB location. Upon arrival, the software adjusts the acoustic focal point to "lower" the component onto the solder-pasted pad before de-energizing the array.

## Chapter 3: Research and Investigation

### *3.1 Literature Review: SMT Placement Technologies and Acoustic Manipulation*

The trajectory of electronic manufacturing is defined by a continuous push toward miniaturization. As Surface-Mount Technology (SMT) transitions from 0805 (2.0 mm x 1.25 mm) packages to 0402 and 0201 scales, the mechanical systems designed to handle them have reached a performance ceiling. The following literature review investigates the limitations of current pneumatic systems and the emergence of acoustic levitation as a viable alternative for the next generation of modular assembly.

#### *3.1.1 Limitations of Conventional Pneumatic Systems*

Current industrial assembly relies almost exclusively on vacuum-based pick-and-place (PnP) technology. While effective for macroscopic components, research by Bergstrand and Malm (2023) highlights that pneumatic systems are increasingly inefficient at the micro-scale. Their study, "Investigation of MEMS-Based Acoustic Levitation for Pick-and-Place Machines," details the "contact barrier," where the physical interaction between the vacuum nozzle and the component introduces three primary failure modes:

- Mechanical Stress and Fracturing: Standard nozzles apply a compressive force during the "pick" and "place" cycles. In ceramic-based components, such as Multi-Layer Ceramic Capacitors (MLCC), this pressure can cause micro-cracks that lead to latent field failures after the soldering process.
- Contamination and Residue: Mechanical contact inevitably transfers oils, dust, or static charge. Drewitt et al. noted that as the surface-area-to-volume ratio of components increases, even microscopic residues can significantly interfere with solder wetting and electrical connectivity.

- Release Failures (Stiction): Perhaps the most significant limitation is the inability of components to reliably detach from the nozzle. In vacuum systems, the "place" cycle requires the vacuum to break instantaneously. However, at the 0402 scale, surface forces often exceed the gravitational force, leaving the component stuck to the tip.

#### *3.1.2 Surface Forces and the "Stiction" Barrier*

The physics of micro-manipulation is dominated by forces that are negligible at larger scales. As documented in the research of Bergstrand and Malm, as component mass decreases, the interaction is no longer governed primarily by gravity, but by Van der Waals forces, capillary forces, and electrostatic attraction. Collectively known as "stiction," these forces make mechanical release unpredictable.

In a conventional environment, a vacuum nozzle must overcome these forces to place a component. If the stiction force is higher than the component's weight, the component remains adhered to the nozzle or shifts its orientation during the release, leading to "tombstoning" or misalignment on the PCB land pattern. Acoustic manipulation sidesteps this entire regime by eliminating physical contact, ensuring that the only forces acting on the component are the controlled gradients of the acoustic field and gravity.

#### *3.1.3 Foundations of Acoustic Manipulation: From Standing Waves to TinyLev*

The utilization of sound waves for levitation is a concept rooted in the study of standing waves. Early research focused on "Langevin radiation pressure," where a high-intensity transducer and a reflector create a stationary wave with fixed pressure nodes. While this can levitate objects, it offers no lateral control, making it unsuitable for pick-and-place operations.

A significant breakthrough occurred with the development of the TinyLev, documented by Marzo, Barnes, and Drinkwater (2017) in *"TinyLev: A multi-emitter single-axis acoustic levitator."* This research demonstrated that a single-axis levitator could be constructed using an array of low-cost, 40 kHz piezoelectric transducers. By arranging transducers in two opposing bowls, the researchers proved that a stable, high-intensity trap could be generated without the need for high-voltage specialized equipment. However, the TinyLev remained a static device; while it could suspend a particle, it could not move it laterally across a plane.

#### *3.1.4 Holographic Acoustic Elements and Phased Arrays*

To transform a static levitator into a functional pick-and-place head, the pressure nodes must be steerable. The PnPAL architecture is heavily influenced by Marzo et al. (2017) in their work *"Realization of compact tractor beams using acoustic delay-lines."* This research introduced the concept of Holographic Acoustic Elements (HAEs).

By utilizing a phased array rather than a fixed-phase standing wave, it is possible to create complex interference patterns. Marzo's research detailed three primary trap types:

1. Twin Traps: Two high-pressure cylinders that "pinch" the component.

2. Vortex Traps: A helical pressure field that traps a component in a central "eye" while applying torque.
3. Bottle Traps: A high-pressure "cage" that completely surrounds the component.

The PnPAL system adopts the Twin Trap geometry for its lateral stability. By calculating the phase delays required to project these traps into 3D space, the PnPAL end-effector can shift the focal point in coordination with the gantry's movements. This literature confirms that a 72-transducer array—the scale selected for PnPAL—is the threshold required to achieve the interference resolution necessary for stable, 3-D steerable traps.

### *3.1.5 Modular Integration and Platform-Agnostic Research*

The decision to frame PnPAL as a modular end-effector is supported by recent trends in "Open-Source Hardware" and "Universal Tool Changing" research. As Cartesian gantry systems (3D printers) have become ubiquitous, research into their kinematics—specifically the vibration profiles of NEMA 17 motors—indicates that they are ideal, low-cost candidates for secondary micro-manipulation tasks. By utilizing the NIST RS274NGC (G-code) standards researched in early CNC literature, PnPAL bridges the gap between high-end acoustic physics and accessible, modular manufacturing.

## *3.2 Theoretical Analysis: Acoustic Radiation Force and Potential*

The manipulation of SMT components in mid-air relies on the precise control of the acoustic radiation force ($F_{rad}$), a non-linear phenomenon that arises when sound waves interact with a physical object. For the PnPAL system to achieve a placement accuracy of $\pm$0.5 mm, the software must model the acoustic field with high fidelity. This section explores the mathematical foundations of the Gor'kov potential and the geometric interference required to create stable volumetric traps.

### *3.2.1 The Gor'kov Potential and the Rayleigh Regime*

In the PnPAL system, the 40 kHz frequency results in an acoustic wavelength ($\lambda$) of approximately 8.65 mm in air ($c \approx$ 343 m/s). Because the target components (e.g., 0805 resistors with a length of 2.0 mm) are significantly smaller than this wavelength, the system operates within the Rayleigh regime ($R \ll \lambda$).

As established by Gor'kov (1962), the time-averaged acoustic radiation force acting on a small spherical particle in an arbitrary sound field can be expressed as the negative gradient of a scalar potential field, U:

$$F_{rad} = -\nabla U$$

The potential U is defined by the mean-square fluctuations of the acoustic pressure (p) and the particle velocity (v):

$$U = 2\pi R^3 \left[ \frac{\langle p^2 \rangle}{3\rho c^2} f_1 - \frac{\rho \langle v^2 \rangle}{2} f_2 \right]$$

### *3.2.2 Acoustic Contrast Factors ($f_1$ and $f_2$)*

The effectiveness of the trap is dictated by the contrast between the component's material properties and the medium (air). The coefficients $f_1$ *and* $f_2$represent the monopole and dipole contributions to the radiation force, respectively:

- Monopole term ($f_1$): Relates to the compressibility (B) of the component.

$$f_1 = 1 - \frac{\beta_p}{\beta_0}$$

- Dipole term ($f_2$): Relates to the density ($\rho$) contrast.

$$f_2 = \frac{2(\rho_p - \rho_{0)}}{2\rho_p + \rho_0}$$

For the ceramic and silicon materials common in SMT assembly, the density ($\rho_p \approx$ 2500–4000 kg/m³) is several orders of magnitude higher than that of air ($\rho_p \approx$ 1.2 kg/m³). Consequently, $f_2$ approaches a value of 1.0. This indicates that the kinetic energy term (the velocity gradient) is the dominant factor in "pulling" the component into the focal point, while the pressure term (compressibility) serves to stabilize the component against gravity.

### *3.2.3 Gradient Forces and Trap Stability*

The "trap stiffness" the ability of the acoustic field to resist displacement—is a function of the steepness of the potential well. Research by Marzo et al. (2017) demonstrated that by utilizing a phased array of 72 transducers, the PnPAL system can create high-intensity gradients that effectively "lock" a component in 3D space.

To move the component, the system calculates a sequence of phase delays that shift the minimum of the Gor'kov potential along a linear path. If the gantry moves too quickly, the inertial force $F = ma$ exceeds the acoustic restoration force $F_{rad}$, causing the component to fall. Therefore, the theoretical limit of the gantry's acceleration is capped by the maximum gradient of U achievable at the current driving voltage (24V).

### *3.2.4 Phased Array Geometry and Interference Patterning*

The spatial resolution of the acoustic trap is determined by the physical arrangement of the 72 transducers. PnPAL utilizes a hexagonal packing geometry, which research suggests provides a higher Sound Pressure Level (SPL) compared to rectangular grids.

In a phased array, the total pressure at any point (x, y, z) is the summation of the individual waves from all N transducers:

$$P(x, y, z) = \sum_{i=1}^{72} A_i \frac{e^{jkd_i}}{d_i} e^{j\phi_i}$$

where $d_i$ is the distance to the focal point, and $\phi_i$ is the phase shift.

A critical design consideration identified in the literature is the avoidance of **grating lobes**—secondary pressure minima that could trap the component in an unintended location. By keeping the transducer diameter (D = 9.9 mm) close to the wavelength (λ = 8.65 mm), the PnPAL array minimizes these artifacts, ensuring that 95% of the acoustic energy is concentrated in the primary focal point. This concentration is what allows the modular head to maintain trap stability even when subjected to the mechanical vibrations inherent in a 3D printer gantry.

### *3.3 Component Research and Comparative Analysis*

The selection of hardware components for the PnPAL modular end-effector is a critical engineering process that balances acoustic performance, weight constraints, and electrical efficiency. Because the system is designed to be attached to a moving 3D printer gantry, the components must be robust enough to handle high-frequency switching while remaining lightweight enough to prevent motor stalling or mechanical ringing.

#### *3.3.1 Ultrasonic Transducers (Piezoelectric Emitters)*

The transducer is the core component of the phased array, responsible for converting electrical energy into the 40 kHz acoustic waves required for levitation. The research focused on identifying emitters with a high Sound Pressure Level (SPL) and a compact form factor to maximize the density of the 72-element array.

**Table 3.1: Comparative Analysis of Ultrasonic Transducers**

| **Parameter** | **Murata MA40S4S** | **Kobitone 400ST160** | **Generic Piezo (HC-SR04)** |
|---|---|---|---|
| Center Frequency | $40.0 \pm 1.0\ kHz$ | $40.0 \pm 1.0\ kHz$ | $40.0\ kHz$ |
| Diameter | 9.9 mm | 16.2 mm | 16.0 mm |
| SPL at 10V ($0dB = 20\mu Pa$) | 120 dB min. | 115 dB min. | 108-112 dB |
| Beam Angle (-6dB) | 80° | 55° | 60° |
| Capacitance | 2550 pF | 2400 pF | 2000 pF |
| Mass | 0.7 grams | 2.2 grams | 2.0 grams |

Technical Justification: The Murata MA40S4S was selected as the primary emitter for several reasons. First, its 9.9 mm diameter is roughly 40% smaller than the Kobitone alternative. In a phased array, the ability to pack transducers closely (hexagonal packing) is vital for reducing grating lobes and increasing the intensity of the central focal point. Second, the 80° beam angle provides a wider "steering envelope," allowing the software to shift the acoustic trap laterally across a larger area without a significant drop in pressure. Finally, its low mass is essential for the modular head's target weight of under 350g.

### *3.32 Power Driver Architectures and H-Bridges*

Driving a 72-transducer array at 24V peak-to-peak requires a high-current switching architecture capable of maintaining signal integrity at 40 kHz. The research compared integrated H-bridge drivers against discrete MOSFET solutions.

- L298N Dual H-Bridge: A common choice for small-scale robotics. While robust and easy to interface, the L298N has a high internal voltage drop (up to 2V) and requires substantial heat sinking when driving multiple inductive loads. Its bulky form factor would significantly exceed the weight limit for a 3D printer tool head.
- Discrete MOSFET Arrays (Selected): Utilizing high-speed N-Channel and P-Channel MOSFETs (such as the AO4606) allows for a significantly more compact PCB. This architecture offers lower $R_{DS(on)}$, resulting in minimal heat dissipation and a cleaner 40 kHz square wave. When paired with 74HC595 shift registers, this setup can drive 72 channels using only a few control pins from the ESP32.

### *3.3.3 Microcontroller and Logic Control*

The control system must handle two simultaneous high-load tasks: generating the 40 kHz phase-shifted signals and parsing G-code commands from the host machine.

- Arduino Mega 2560: While widely used in 3D printers, the 16 MHz 8-bit processor is insufficient for calculating 72 Euclidean distances and performing phase-shifting interrupts at the required 80 kHz toggle rate.
- ESP32 (Selected): The ESP32 features a dual-core 32-bit processor running at 240 MHz. By dedicating Core 0 to signal generation and Core 1 to the high-level logic and G-code parsing, the system ensures zero-jitter performance. Furthermore, the built-in Wi-Fi and Bluetooth capabilities allow the PnPAL to operate as a stand-alone IoT device, receiving assembly instructions directly without a physical tether to the printer’s mainboard.

### *3.3.4 Shift Registers and Multiplexing*

To control 72 transducers individually using a microcontroller with limited I/O, a multiplexing strategy is required. The 74HC595 8-bit Shift Register was researched for its high-speed serial-to-parallel conversion capabilities.

According to the 74HC595 Datasheet, the device can operate at clock frequencies up to 31 MHz (at 4.5V). Since the PnPAL requires a data update rate of only 80 kHz to maintain a 40 kHz carrier, the 74HC595 provides a massive performance margin. By daisy-chaining nine registers, the ESP32 can control all 72 emitters using only three pins: Data, Clock, and Latch. This reduction in pin count is essential for maintaining a clean, low-noise PCB layout in a compact modular head.

#### *3.3.5 Mechanical Interface and Interoperability Standards*

Since the PnPAL is a modular attachment, it must adhere to established mechanical standards to ensure compatibility with various 3D printer frames.

- E3D V6 Groove-Mount: This is the most prevalent tool-changing standard in the FDM 3D printing community. Research into the mechanical specifications revealed that a 12mm diameter neck with a 6mm groove depth is the universal standard for carriages on machines like the Prusa i3, Creality Ender 3, and Voron series.
- Power Delivery: Research into 3D printer power supplies (such as the Mean Well SE-450-24) confirms that the 24V DC rail is the standard for modern high-performance printers. This aligns perfectly with the PnPAL's requirement for a 24V peak-to-peak transducer drive signal, allowing the head to draw power directly from the printer's auxiliary power terminals.

### *3.4 Modular Integration and Interoperability*

The transition of the PnPAL system from a stand-alone prototype to a modular end-effector requires an exhaustive investigation into the standards that govern existing CNC and 3D printing ecosystems. For the device to be truly platform-agnostic, it must adhere to established mechanical mounting conventions, electrical power delivery standards, and communication protocols. This section details the research into how a high-frequency acoustic array can be seamlessly integrated into a standard Cartesian gantry environment.

#### *3.4.1 Mechanical Standards and Mounting Ecosystems*

To ensure compatibility with the widest range of consumer and professional 3D printers, the research focused on the E3D V6 mounting standard. According to documentation from E3D-Online, the "groove-mount" system utilizes a 12mm diameter cylindrical neck with a 6mm deep, 3.7mm wide groove. This has become the de facto mounting standard for printers such as the Prusa i3, Creality Ender series, and many Voron builds.

However, mounting a 72-transducer array presents a unique mechanical constraint: the Cantilever Load Limit. Most 3D printer X-carriages are driven by NEMA 17 stepper motors, which, according to the NEMA 17 Physical Specification, typically provide a holding torque between 0.3 Nm and 0.5 Nm. Research into the kinematics of these systems suggests that adding more than 400g to the tool head can lead to "ringing" (ghosting) during rapid directional changes. This influenced the design of the PnPAL housing to utilize lightweight PETG and a high-density PCB to keep the total mass under 350g, ensuring that the gantry's acceleration profiles remain stable during acoustic manipulation.

### *3.4.2 Communication Protocols: G-code and NIST RS274NGC*

The primary language of CNC motion control is G-code, standardized under NIST RS274NGC. For the PnPAL to be interoperable, it must interpret these commands in real-time. Research into open-source firmware like Marlin and Klipper revealed that these systems can output coordinates via a secondary UART serial port.

The investigation identified two primary methods for synchronization:

1. Passive Interception: The PnPAL ESP32 "listens" to the serial stream and updates the acoustic focal point whenever a G0 or G1 (linear move) command is detected.
2. Active Triggering: The use of custom M-codes (e.g., M106 for fan control) to signal the PnPAL head to activate specific sub-routines, such as the "Pick" or "Place" sequences.

By adopting the NIST standard, the PnPAL head can be controlled by any standard slicing software (such as Cura or PrusaSlicer), provided a post-processing script is used to convert 3D coordinates into the phase-delay arrays required by the 72 emitters.

### *3.4.3 Power Delivery and Auxiliary Rail Integration*

As documented in the research by H. W. Ott (2009) on electromagnetic compatibility, high-power switching at 40 kHz can introduce significant noise into a shared power rail. Modern 3D printers typically operate on a 24V DC auxiliary rail. While this is ideal for the 24V peak-to-peak requirement of the transducers, the shared nature of the power supply means the PnPAL must include robust EMI filtering.

Research into Mean Well SE-450-24 power supplies—the standard for many mid-range printers—indicates that they can handle transient loads of up to 18A. However, to prevent the PnPAL's high-frequency switching from "back-feeding" noise into the printer's sensitive thermistor and MCU lines, the design research led to the inclusion of a dedicated LC low-pass filter on the PnPAL's power input. This ensures that the 40 kHz carrier remains isolated to the end-effector, fulfilling the requirement for a "plug-and-play" device that does not compromise the host machine's safety or accuracy.

### *3.4.4 Interoperability with Slicing and CAM Software*

The final layer of modularity is software integration. Traditional Slicers (Computer-Aided Manufacturing software) are designed to output paths for plastic extrusion, not acoustic manipulation. Research into Cura's Post-Processing Plugin Architecture shows that Python scripts can be used to modify G-code on-the-fly.

A PnPAL-specific script was researched to:

- Identify the Z-height of the feeder tape.
- Insert a delay (G4) to allow the acoustic trap to stabilize.
- Translate the "extrusion" commands into "levitation" commands.

This research ensures that the end-user does not need to write custom firmware to use the PnPAL; they can simply use the same tools they use for 3D printing, further lowering the barrier to entry for contactless micro-assembly.

### *3.5 Electrical Introduction*

Design of the piezoelectric pick and place machine's electric system required a plethora of research to ensure safety, efficiency, compatibility, and proper functionality. Many of the frequented documents include datasheets, application notes, and books of many formats.

Theory and practice often involve ideal (virtually accurate), compatible, and safe components. This base level understanding however leaves a lot to be desired when real-world application comes into play. With a myriad of voltage, current, heat, devices/components, and natural laws coexisting in one ecosystem – it is imperative that system designers have a thorough understanding of the functional characteristics of each element.

#### *3.5.1 Voltage, Current, and Electrical Behavior*

There are two elements that serve as the foundation for all electrical systems – voltage and current. Voltage is the potential energy per unit charge, measured in volts (V). This can be thought of the force that moves electrons (negatively charged, subatomic particles). In terms of water flow , voltage correlates to *water pressure*. On the other hand, electrical current is the actual flow of these electrons, measured in amps (A). In the same case of water flow, this can be thought of as the water's *flow rate*. Similarly important to the understanding of electrical systems is the concept of resistance. Resistance is essentially the opposition of current flow. This can be represented by a water pipe's diameter, as a narrower pipe would impede liquid flow.

Other important terms include polarity and load. Polarity is the direction of voltage and current flow (often denoted by a + and -), while a load is any device that consumes electrical power.

It should be noted that the piezoelectric pick and place machine works with voltage in two forms – Direct Current (DC) and Alternating Current (AC).

**DC Voltage**

DC Voltage remains constant in polarity and magnitude, resulting in a unidirectional, streamlined application of voltage. Due to its consistency and stability, this is the voltage used in electronics.

**AC Voltage**

AC voltage's "alternating" characteristics stem from a periodically reverse polarity, often following the figure of a sinusoidal sine wave. This oscillation, along with its minimal transmission loss makes AC voltage the choice for large-scale transmission. It should also be noted that industrial generators naturally produce voltage in AC. Therefore, AC voltage is used to transmit and distribute electricity from power plants to the end user. Once it has reached its target, it is converted to DC and used domestically for everyday use.

**Ohm's Law**

The relation of these three elements is explained via Ohm's Law, which states that current is directly proportional to voltage and inversely proportional to resistance. From an equational standpoint: V = I x R. Another important relation is that of power: P = I x V.

This law is paramount to the understanding of electricity and how it interacts within its designated systems. Much of the research conducted worked off of these foundational elements, with each system, subsystem, and component featuring unique specifications (specs) and ratings pertaining to voltage and current.

### *3.5.12 Electrical Behavior – Specs and Ratings*

Specifications, or specs are the descriptive, technical characteristics of a device or component. For example, an Efficiency of 90% typical. Ratings on the other hand are the values that at which a component can operate safely. An example would be a Maximum Input Voltage of 5V.

As stated earlier, the design of a safe and reliable electrical system relies on the thorough understanding of each element and its characteristics. Though the sources of information may vary, there are a variety of parameters that can be found across the board. These bits of information, once properly understood, can be used to integrate a multitude of electrical components and subsystems. Below are the attributes that had the most influence on the electrical system layout. Once the parameters are understood in their definition, their influence can be easily understood as well.

**Rated Voltage**

A device's nominal operating voltage under normal conditions. Failure to meet this value could result in the device not functioning properly. Exceeding this value could lead to damage and electrical failure.

**Rated Current**

The current that a device can continuously operate at. Too little current may lead to failure of function, while too much could lead to overheating and/or device damage and failure.

**Peak or Surge Current**

This is the maximum current that a device or component may produce during startup, inrush (the initial surge needed to startup electrical devices), etc. This is usually higher than the rated current, and is meant to represent a peak, not a continuous level. This value is crucial, as a system designed to withstand the rated current but not the surge current is still susceptible to damage and failure.

**Inrush Current**

A brief spike in current that is needed to start electrical devices such as transformers and motors. Not every surge current is due to inrush, but inrush current often accounts for peaks and surges in currents.

**Power Rating**

This is the maximum power that a device can deliver. It should be remembered that Power is the result of Voltage multiplied by Current, so voltage and current values should be viewed not only in isolation, but in relation to the system's power. An underrated power supply could cause unreliable voltage and current values, depending on the load. Exceeding this rating on the other hand could lead to overheating and device damage.

**Efficiency (η)**

Efficiency represents the ratio of output power to input power, expressed as a percentage. Essentially, how well a system uses the energy it consumes. 100% efficiency is virtually impossible, though it is a viable target. Energy is often lost through resistance as heat.

**Thermal Rating**

The optimal operating temperature (or temperature range) for a device. Temperatures outside of this range can lead to damage and/or malfunction.

**Leakage Current**

A small (though not negligible) amount of current that flows even when a device is off or not functioning. Though small in nature, it is easy to see how in a complex system, multiple leakage currents could amount to a dangerous flow of power. Identification of these currents helps ensure safety and regularity in a system.

Knowledge of these basic definitions helps in understanding the subsequent concepts of protection, voltage conversion, device operation, and wiring/ power distribution.

### *3.5.2 Protection Principles (General)*

From the aforementioned electrical principles comes another important prerequisite to electrical schematic design – protection. From concepts such as overcurrent and surge voltage comes systems, components, and schemes to eliminate these dangers. As stated earlier, one of the key components of an electrical system is *safety*. When working with power design, it must be ensured that not only are the users and operators safe, but the equipment too. Breaches of optimal and maximum levels can lead to system damage and ultimately failure.

Similarly to the topic of specs and ratings, there are a few potentially harmful phenomena that are important to limit, eliminate, and/or stifle. When researching the protection necessary for the power supply, the phenomena were organized (and the solutions to their adverse effects) under two categories: subsystem/rail protection, and subsequent branch protection.

**Subsystem/rail protection**

This subsection's main purpose is to protect voltage rails, major voltage converters, and power supply units alike. Essentially, these modes of protection target areas where large amounts of voltage and signal culminate. It should be noted that protection can exceed voltage and current, branching into fields such as Electromagnetic Fields and reverse polarity wiring.

**Branch Protection**

This area of protection rivals the former in the fact that the load bearing devices are the patients of protection, not the sources. For example, a 48V rail may have 2 stepper motors that receive their power via the 48V rail. In this case, each motor would be attached via an individual branch, and each of these branches would likely have adequate protection (such as a fuse). The purpose of this protection is to protect the load, or the device, component, or subcircuit that is receiving its power supply from a greater source. Fuses, along with other protection devices, will be discussed in depth in the next section. Individualized branch protection is extremely important as it also ensures that local faults don't spread to other areas of circuitry.

**Protection (General)**

Though both designations focus on different devices and system levels, both ensure device-wide durability, safety, and reliability. An electrical network without protection is susceptible to factors such as human error, device specification variance, and environmental conditions – just to name a few.

### *3.5.3 Protection Devices (Component Level)*

Upon categorizing the protection into two categories, a multitude of protection levels were considered. Much of the background included each device's purpose along with its method of protection, and way of application. For example, it is important to know that fuses are rated based off of current. Below are the most prominent protection devices in regard to the intended pick and place machine.

**IEC Inlet Module (with EMI filtering)**

An IEC Inlet Module is a device that engages in multiple forms of electrical protection, spanning past the elementary limits of voltage and current. These are often used as the first stage of protection, placing itself in between the 120VAC Mains, and the internal DC Power Supply (the Power Supply Unit). A four-function EMI filter can contain an IEC (International Electrotechnical Commission Standardized) connector, fuse holders, a power switch, and an EMI (Electromagnetic Interference) filter. The module is designed to refine the incoming high voltage (120VAC) signal, while adding a layer of protection and control as well.

**Fuse**

An electrical safety device featuring a metal wire that destroys itself upon overcurrent. This in essence eliminates the connection and isolates the circuit (or affected device). The conventional fuse isolates the circuit by melting a metal element, creating a permanent rift. This can only be rectified via replacement. Electronic Fuses on the other hand are structured similarly, using active electronics instead of finite circuitry. Examples of these electronics would be MOSFETs (metal-oxide-semiconductor field-effect transistors). This creates a circuit that breaks at overcurrent, but in contrast to the conventional fuse can be reset and reused.

**Transient Voltage Design (TVS) Diode**

A device designed to counter surges. It essentially acts as a ceiling that "clamps" any voltage that exceeds a preset limit. This is a *secondary* surge protector, specialized in handling transients that are quicker, yet lower in energy. Besides inrush currents, loads such as voltage converters are also major sources of spikes in the voltage transients. TVS Diodes are key in protecting related circuitry from these peaks.

**Ideal Diode Controller**

A smart circuit that prevents current from flowing in the wrong direction. This essentially protects the circuit from damage via reverse polarity wiring.

Research on each of these elements, using the principles mentioned in previous sections, was crucial in ensuring that the electrical system at hand was able to maintain safe operation.

**Bleed Resistor**

A high value resistor placed across a high value output to discharge stored energy after shutoff. When comped with the HV converter, it ensures that any excess voltage is quickly dispersed and discharged, preventing damage to users and or nearby circuits.

**Interlock Mechanism**

A safety mechanism designed to disable power when unsafe conditions arise. In the piezoelectric pick and place machine, an interlock mechanism would ensure that nearby circuits or people don't come into contact with the transducer's high voltage supply.

**Table 3.2: Implemented Protection Devices**

| Device/ Component | Function | Response Time | System Use | Implemented |
|---|---|---|---|---|
| IEC Inlet Module (with EMI filter) | AC entry point, fuse protection, EMI suppression | Continuous | AC input noise suppression and surge protection | x |
| Fuse | Overcurrent negation and protection | Milliseconds | Branch or rail overcurrent protection | x |
| TVS Diode | Voltage spike suppression | Nanoseconds | Rail, surge protection | x |
| Ideal Diode Controller | Reverse current flow protection | Microseconds | 48V Rail reverse polarity and backfeed faults | x |
| Bleed Resistor | High voltage discharge | Seconds | HV output safety | x |
| Interlock Mechanism | Disable accidental access to high voltage | Milliseconds | High voltage protection and isolation | x |

#### *3.5.4 Power Supply Unit, DC-DC Converters*

The power supply unit (PSU) along with lower-voltage DC to DC converters were used to step down the 120VAC to functional levels. This is crucial, as different loads require different input voltages for peak functionality and overall safety. This is where knowing the aforementioned specs and ratings provided useful.

**PSU**

The PSU was rather straightforward, with factors such as voltage, wattage, and ampere coming into play. Efficiency also became a factor later on in the process. PSU ratings of 48V (to power the 48VDC rail), 400W, and 8.3A were selected for AC-DC conversion.

**DC-DC Conversion**

DC to DC converters come in a plethora of conversion methods, though research focused on three approaches: Boost, Buck, and LDO (Low-Dropout Linear Regulator). Boost and Buck converters are both switching voltage regulators, meaning voltage is regulated by rapidly switching a transistor on and off. LDOs on the other hand are linear, dissipating excess voltage via heat. This linear process is less efficient than that of a switching converter. Boost converters step up the voltage, raising their DC value to a higher potential. Buck converters on the contrary step down voltages. LDOs act similarly to buck converters by stepping down the voltage. However, these converters specialize in smaller magnitude conversions while producing less noise. This would be ideal for small voltage reductions like 5VDC to 3.3VDC.

Similar to the PSU, voltage and ampere ratings were investigated and established to ensure compatibility with the rest of the circuit. In the end, a conjunction of Buck converters and LDOs were used to step down high voltages to a potential ideal for the microcontroller and other devices.

**Table 3.3: Comparison of Voltage Converters**

| Converter Type | Function | Voltage Handled | Efficiency | Complexity | Advantage | System Use | Implemented |
|---|---|---|---|---|---|---|---|
| Boost | Step-up | DC | 80-90% | Moderate | High efficiency | Potential Voltage Boost | |
| Buck | Step-down | DC | 85-95% | Moderate | High efficiency | DC-DC Conversion from 48V to lower potentials | x |
| LDO | Step-down (linear) | DC | 60-80% | Low | Low noise, minimal complexity | Logic and Control Rail Power (3.3V) | x |
| PSU | AC to DC Conversion | AC,DC | 85-90% | High | Provides isolation, acts as main DCV supply | AC to DC conversion, DC Main Power Supply | x |

**HV Converter**

A converter is necessary to step up the 48VDC rail's voltage to 240VAC. Piezoelectric transducers require a large amount of AC voltage, so the converter provides power amplification while acting as a transformer. The most important specs for the HV converter are its output characteristics, as this is what will be feeding the piezoelectric transducers. Therefore, its output was specified to 72W at 240VAC, with an efficiency of 80-90%.

**Table 3.4: Comparison of High Voltage Converters (DC-AC)**

| HV Converter Model | Input Range | Output Power, Voltage | Efficiency | Isolation | Key Features | Implemented |
|---|---|---|---|---|---|---|
| Custom Flyback / LLC Converter | 40-55 VDC | 240 VAC @72W | 85% | Yes | Bleed resistor and interlock support | x |
| TDK-Lambda PH-A280 Series | 36-65 VDC | 200 VDC @75W | 90% | Yes | Industrial isolation | |
| XP Power JHM75 Series | 36-60 VDC | 250 VDC @75W | 88% | Yes | Low leakage current | |
| Murata NMV0515SC | 24-60 VDC | 150 VDC @15W | 80% | Yes | Minimal protection, budget friendly | |

### *3.5.6 Wiring and Distribution*

The bulk of the power distribution is housed in a PCB (Printed Circuit Board). The electrical schematics that enact the power flow are actuated through a PCB circuit. Still, wiring is required to connect the load-bearing devices to their designated PCB nodes. Current (ampacity), voltage rating (insulation), EMI proximity, and connector size were used to derive the list of necessary wires.

**Wiring by Subsection**

- AC in (120VAC): 16AWG
- 48V Rail: 16 AWG
- 12V Branches: 20 AWG
- 5V/3.3V Branches: 22 AWG
- HV in (240VAC): 18 AWG
- PCB: 16 mil traces

**Table 3.5: Implement Wires by Gauge**

| Wire Type | AWG | Voltage Rating | Ampacity | Flex | System Use (In, Out) | Use |
|---|---|---|---|---|---|---|
| UL1015 | 16 | 600V | 8-10A | Moderate | 120VAC, 48VDC Trunk | HV rated, plenty of ampacity |
| UL1015 | 18 | 600V | 4-6A | Moderate | 48 VDC Rail, 48V Loads | High ampacity, easier to route than 16AWG |
| UL1007 | 20 | 300-600V | 2-3A | Flexible | 12 VDC Rail, 12V Loads | Small, flexible, rated for 12V |
| HV Silicon/ PTFE Lead | 18 | 300-600V (HV Insulation) | 2-4A | Flexible, Heat Resistant | HV Converter Out, Piezo Array | Increased insulation to withstand HV |
| 22-24 AWG Signal (PVC, twisted pair) | 22-24 | 300V | <1A | Very Flexible | 5 VDC Rail, Control & Interlock Supply | Extremely small and flexible – perfect for logic and control |

*Twisted Pair – Two insulated conductors that are twisted together, cancelling out their electromagnetic fields. This reduces noise and interference.

### *3.6 Summary of Research Findings*

The research and investigation phase for the PnPAL system confirms that a modular, platform-agnostic approach is not only feasible but represents a significant engineering advancement over traditional standalone assembly units. The convergence of acoustic physics, high-speed digital control, and universal mechanical standards provides the foundation for a system that is both technically robust and economically accessible.

#### *3.6.1 Synthesized Technical Conclusion*

The investigation into the Gor'kov potential and the Rayleigh regime validates the use of a 40 kHz operating frequency. This frequency provides a near-optimal wavelength ($\lambda \approx 8.6$ mm) for the stabilization of 0805 and 0603 SMT components. Research confirms that a 72-transducer array is the minimum threshold required to generate a steerable "Twin Trap" with sufficient stiffness to withstand the inertial loads of a moving gantry.

#### *3.6.2 Hardware and Control Optimization*

The selection of the ESP32 dual-core microcontroller is vital for the deterministic performance required. By delegating the 40 kHz signal generation to Core 0 and the G-code parsing to Core 1, the system eliminates the jitter that frequently destabilizes acoustic traps in single-core architectures. Furthermore, the use of serialized shift registers and discrete MOSFET drivers allows for a compact, high-voltage output stage that maintains the 24V peak-to-peak amplitude across all 72 channels while staying within the strict weight limits required for a modular tool head.

#### *3.6.3 Modularity and Deployment Strategy*

The research into mechanical and communication standards (E3D V6 and NIST RS274NGC) ensures that the PnPAL head can function as a "plug-and-play" device on the majority of consumer-grade 3D printer frames. This allows the system to leverage the high-precision motion control of existing Cartesian gantries, effectively turning a common fabrication tool into a specialized micro-assembly station.

**Table 3.6: Finalized Design Parameters Based on Research Findings**

| Parameter | Selection | Engineering Justification |
|---|---|---|
| Array Architecture | 72-Channel Hexagonal Array | Maximizes Sound Pressure Level (SPL) and minimizes grating lobes. |
| Primary Emitter | Murata MA40S4S | Highest SPL-to-diameter ratio; 80° beam angle for superior steering. |
| Logic Controller | ESP32 (240 MHz Dual-Core) | Essential for real-time task separation (PWM vs. G-code). |
| Driver Stage | MOSFET Array with 74HC595 | Lightweight, high-efficiency switching with low $R_{DS(on)}$. |
| Power Input | 24V DC (Universal Rail) | Native compatibility with modern 3D printer power systems. |
| Mounting Standard | E3D V6 Groove-Mount | De facto industry standard for modular FDM tool heads. |

### *3.6.4 Electrical Summary*

Research proved essential to the design of the electrical system. With so many different circuit elements at hand, it is imperative that one understands them and their characteristics in totality. Varied, trustworthy sources are important to paint an objective and wholistic picture. Through this lens is integration of the system verified and executed.

**Table 3.7: Electrical Device Summary**

| **Function / Component** | **Spec Target** | **Candidate Part / Model** | **Notes** |
|---|---|---|---|
| AC Fuse / Breaker | Slow-blow 6 A @ 250 VAC | Schurter / Littelfuse | Sized for PSU inrush + margin over 3.3 A continuous. |
| IEC Inlet + EMI Filter | 250 VAC, 10 A | Schaffner FN9222-1-06 (or equiv.) | Earth bond near inlet; provides conducted EMI suppression. |
| PSU (AC → 48 V) | 48 V DC, 400 W (8.3 A) | Mean Well SE-450-48 | Central DC supply; 30–50 % headroom for peaks. |
| 48 V Main Fuse / Breaker | 10 A DC | DC-rated blade / MCB | Protects main trunk; 125 % over peak load. |
| Reverse Polarity Protection | ≥ 60 V, low Rds(on) | LTC4368 + MOSFET | Ideal-diode controller; lower loss than series diode. |
| 48 V TVS Clamp | Vrwm ≈ 58 V, ≥ 1.5 kW | SMCJ58A | Suppresses transient spikes on 48 V entry. |
| 48 → 12 V DC-DC | 30–50 W, 90 % eff. | CUI / Vicor non-isolated module | Feeds logic buck; compact board-mount module. |
| 48 V Branch eFuses | Per branch (HV, 12 V, Motion, Aux) | TI TPS259xx series | Each module isolated from main bus. |
| 12 V Branch eFuses | 1–2 A each | TI TPS259xx series | Protects 12V buck branche(s). |
| 12 → 5 V Buck Regulator | 3 A output | MP1584 / LM2596 | Powers 5V, eventually logic. |
| | | | |

| Function / Component | Spec Target | Candidate Part / Model | Notes |
|---|---|---|---|
| 5 → 3.3 V Regulator (LDO/Buck) | 1–2 A | AMS1117-3.3 / MP2307 | Provides clean rail for logic and sensors. |
| Motion Controller (MCU) | 5 V @ 0.3 A typ / 0.6 A pk | SAM3X8E (Arduino Due logic) | 3.3 V logic; 5 V input protected by eFuse. |
| 5 V → MCU eFuse | 1.0 A limit + OVP 5.6–6 V | TI TPS2595x | Protects MCU from surges and shorts. |
| 5 V Filter @ MCU | Ferrite + 22–47 µF ‖ 0.1 µF | Murata BLM21PG600SN1D (0603, 60 Ω @ 100 MHz) | Local decoupling right at MCU pin. |
| I/O Protection @ MCU | Series R 22–100 Ω + ESD array | Littelfuse SP1001-04XTG (quad array) | Safeguards non-5 V-tolerant pins. |
| USB Protection @ MCU | Polyfuse 1.5 A + USB ESD array | Littelfuse USBLC6-2SC6 | At USB connector; limits fault current. |
| HV Converter (48 V → 240 VAC) | ~72 W, 85 % eff. | Custom Flyback / LLC | Feeds transducer array; isolated. |
| Transducer Array | 72 elements @ ultrasonic kHz | *Personally constructed | Shielded HV harness. |
| HV Interlock / Discharge | ≤ 30 s to ≤ 60 V | Lid switch + R bleeder (400 kΩ 1 W) | Ensures touch-safe voltage decay. |
| EMC Hardware | Shields / ferrites / clamps | Wurth / TE | One-end chassis bond for cables. |
| Grounding Hardware | Earth stud + star washer | *Generic wiring | Single-point bond near IEC inlet. |

# Chapter 4: Standards and Design Constraints

### *4.0 Introduction*

The development of the PnPAL modular end-effector must transcend functional prototyping to meet the rigorous requirements of industrial and consumer safety, interoperability, and manufacturability. As a device intended to interface with external 3D printer hardware and operate in human-centric environments, it is governed by a complex framework of international standards and realistic constraints. This chapter details the technical benchmarks and ethical considerations that shaped the engineering of the PnPAL system.

This chapter in its essence identifies the safety standards and design constraints that shaped the project's design decisions. These guidelines sometimes span disciplines with electrical, mechanical, and sometimes optical constraints coinciding with one another. The importance of safety compliance has both moral, practical, and industrial implications.

The primary priority is the safety of the users and equipment alike. This entertains the idea of a rather moral and practical value. These requirements set the stage for standard conditions that ensure no damage is accrued during the system's operation. Potential hazards include electric shock, thermal overload (i.e. fire), and mechanical obstruction. For example, standard UL 61010-1 establishes limits on voltage, temperature, and mechanical safety as well. It should be noted that the prefix UL (Underwriters Laboratories) represents just one organization that enforces UL 61010-1. International Electrotechnical Commission (IEC) Standard 61010-1 contains overlapping guidelines, with its jurisdiction opposing UL's domain of North America with an international region of influence.

Practical reasoning is also present in the ability of standards to enhance the reliability and predictability of system operation. Aside from basic safety, each standard gives a glimpse of insight based on previous successes and errors. This aid in discernment can prove extremely useful when embarking on the journey that is engineering design.

From an industrial standpoint, standards guarantee industry consistency and acceptance. The NEC (National Electrical Code) wiring color codes provide an example, as these standards provide a great deal of consistency and understanding from project to project. For many products however, previously mentioned standard UL 61010-1 must be adhered to for North American distribution. In this case, implementation of these requirements provides not just convenience, but survival.

With parts such as high voltage transducer arrays and microcontrollers, standards are integral to the safe design and operation of the piezoelectric machine at hand.

### *4.1 Technical Standards*

Adherence to established technical standards ensures that the PnPAL system is reliable, safe, and interoperable with existing manufacturing ecosystems. The following standards were instrumental in the design of the electrical, acoustic, and communication subsystems.

#### *4.1.1 IPC-2221A: Generic Standard on Printed Board Design*

The PnPAL driver board manages significant power density, with a 24V supply driving 72 piezoelectric transducers. To ensure long-term reliability and prevent thermal failure, IPC-2221A was used to determine the minimum trace widths for the power distribution network.

For the 24V rail, which carries the peak current for the H-bridge drivers, calculations were performed to ensure a temperature rise of no more than 10°C above ambient. Given the compact nature of the modular head, utilizing IPC-2221A guidelines allowed for the optimization of the 4-layer PCB stack-up, ensuring that internal power planes provide sufficient heat dissipation for the 74HC595 shift registers and MOSFET arrays.

### *4.1.2 ANSI/ASA S1.11: Electroacoustics and Octave-Band Filters*

Operating at 40 kHz, the PnPAL system falls under the purview of electroacoustic standards. ANSI/ASA S1.11 provides the framework for characterizing the frequency response and purity of ultrasonic emissions.

Although 40 kHz is above the human hearing threshold, the standard guided the design of the driver logic to ensure that "switching noise" from the MOSFETs does not generate sub-harmonic frequencies in the audible range (20 Hz – 20 kHz). By maintaining a high-purity square wave at the transducer terminals, the system minimizes audible "whine" and ensures that the acoustic trap remains stable without interference from low-frequency environmental noise.

### *4.1.3 IEEE 802.11 (Wi-Fi) and NIST RS274NGC (G-Code)*

As a platform-agnostic device, PnPAL utilizes IEEE 802.11 for wireless data transmission, allowing it to receive assembly files from a remote terminal. The communication protocol follows the NIST RS274NGC standard for G-code. This ensures that the PnPAL's internal parser can interpret commands from any industry-standard slicing software (e.g., Cura, PrusaSlicer), facilitating its role as a "plug-and-play" upgrade for 3D printer frames.

### *4.1.4 FCC Part 15: Electromagnetic Compatibility (EMC)*

High-frequency switching of 72 inductive loads (piezoelectric crystals) creates a significant risk of electromagnetic interference. FCC Part 15 dictates the limits for radiated and conducted emissions. To comply with these regulations, the PnPAL hardware incorporates a localized LC filter on the 24V input and utilizes the internal ground planes of the PCB as an EMI shield. This prevents the 40 kHz carrier from interfering with the sensitive thermistors and end-stop sensors of the host 3D printer.

**Table 4.1: Subsystems & their Associated Standards**

| Subsystem | Relevant Standards | Governed Elements |
|---|---|---|
| Power Supply (120VAC to 48VDC) | IEC 61010-1, NEC | Wiring, fuse sizing |
| PCB Power Distribution | IPC-2221B | Trace sizing, copper thickness |
| HV Converter | IEC 61010-1, UL 62368-1 | Isolation, interlock, HV discharge time |
| Wiring & Grounding | NEC/ NFPA 70 | Color coding, conductor ampacity |
| EMI | FCC Part 15 Class B | Radiated emissions |
| Vision & Data Interface | USB 3.0 Spec, FCC Class B | Shielding, power limit |

### *4.1.5 Applicable Standards & Regulations (Cont.)*

Section 4.1.5 communicates and emphasizes the standards and regulations that apply to the project at hand. This differs from the previous section, which served as an introduction to standards and how they serve importance in the field of engineering.

**Standards in Electrical Safety**

- UL 61010-1/ IEC 61010-1: Laboratory and measurement safety. Bleed Resistor Discharge Time (≤ 30s), Voltage Residual (< 60V).
- UL 62368-1/ IEC 62368: Standards for control and communication equipment.
- NEC: Wire gauge, ampacity, grounding, color coding.
- UL 94: Material flammability, thermal safety.

Implementation in Design: The aforementioned standards guided the design of the pick and place machine's wiring, bleed resistor(s), and interlock system.

**Standards in EMI/EMC**

- FCC Part 15, Class B: Radiated, conducted emissions.

Implementation in Design: IEC inlet, and other areas of EMI filtering.

**Standards in PCB and Wiring**

- IPV-2221B: Trace width, current guidelines, copper weight selection.
- NASA-STD-8739.4A: Twisted pair and shielding practices.

Implementation in Design: PCB Wiring and twisted pair EMI cancellation. High voltage wire shielding.

## *4.2 Realistic Design Constraints*

The PnPAL project is not only a technical challenge but also a practical engineering exercise constrained by economic, environmental, and manufacturability factors.

### *4.2.1 Economic Constraints*

The primary economic goal is to provide an affordable alternative to industrial pick-and-place machines.

- Target BOM: The system is designed with a Bill of Materials (BOM) under $500. By utilizing low-cost Murata transducers and the versatile ESP32, the system achieves high-end performance without the cost of specialized pneumatic infrastructure.
- Modular Value: The "End-Effector" approach allows users to leverage their existing investment in a 3D printer, effectively reducing the capital expenditure for SMT assembly by almost 90% compared to purchasing a dedicated standalone machine.

With an overall budget of $2,250, cost was a decisive factor in many of the decisions made. It is safe to say that every element, from the PSU to the bleed resistor was designed in regard to cost. This introduced a tradeoff of cost and quality.

**Table 4.2: Total Cost**

| Component | Estimated Cost |
|---|---|
| Microcontroller (Arduino Due or equivalent) | $50 |
| Ultrasonic Transducers and Driver Circuits | $1000 |
| Power Supply Unit | $150 |
| Aluminum Extrusion Frame | $150 |
| Miscellaneous Components (Wiring, Connectors, Fasteners) | $200 |
| Total Cost | $1,550 |

#### *4.2.2 Environmental and Sustainability Constraints*

- Acoustic Pollution: While 40 kHz is inaudible, it can affect domestic animals or sensitive laboratory equipment. The design includes a constraint for a "low-emission" mode, where the array power is reduced during idle periods.
- RoHS Compliance: To ensure environmental sustainability, all components—including the piezoelectric transducers and the lead-free solder used in assembly—comply with the Restriction of Hazardous Substances (RoHS) directive, facilitating safe disposal and recycling.

#### *4.2.3 Health and Safety Constraints*

Operating a moving gantry with high-intensity ultrasonic waves introduces specific safety requirements.

- Physical Safety: The modular head features rounded edges and an enclosed PCB to protect the user from mechanical pinch points and high-voltage (24V) exposure.
- Acoustic Safety: Research into high-frequency sound exposure indicates that long-term proximity to high-SPL ultrasound can cause ear fatigue. The system is designed to be operated within a standard 3D printer enclosure, which acts as a secondary barrier to dampen stray acoustic energy.

#### *4.2.4 Manufacturability and Reliability Constraints*

The transition to a 72-transducer array presents a unique assembly challenge.

- Precision Alignment: For the phased array to function, each transducer must be aligned within ±0.5 mm of its intended position. The project utilized a 3D-printed alignment jig to hold the transducers in a perfect hexagonal grid during the soldering process.
- Modular Rigidity: The housing must be rigid enough to support the 72 emitters without flexing, yet lightweight enough (<350g) to prevent the host 3D printer's motors from stalling during high-speed moves. This constraint dictated the use of high-fill PETG for the structural housing.

#### *4.2.5 Voltage and Current Constraints*

Overvoltage, overcurrent, and polarity proved to be the most prominent constraint relating to elementary ohmic values (voltage, current). These limitations yield designated rail voltages along with subsystem isolation, and protection devices such as eFuses and TVS diodes.

#### *4.2.6 Thermal Constraints*

A thermal constraint of < 70 °C junction temp for electronics; insulation rated ≥ 105 °C was employed. This is key for safety in areas that draw a lot of current, such as the 48V rail. Proper spacing of the subsystem and its load-bearing devices, along with ventilation of the machine's aluminum frame help counteract thermal hazards.

#### *4.2.7 Mechanical Constraints*

A clear constraint is the size of our machine (or rather prototype). This is clearly defined in the revised "Divide and Conquer" document as 60 cm (Length) x 60 cm (Width) x 45 cm (Height). Other mechanical limitations include PCB dimensions and connector spacing.

#### *4.2.8 Electrical Noise and Electromagnetic Restraints*

The production of electrical noise poses the risk of signal distortion. This in effect yields a set of limitations, evoking a response that is enacted through EMI filtration. EMI/EMC filters, along with twisted-pair wiring and shielding work to ensure that these restraints aren't broken.

#### *4.2. Summary of Standards vs Design Implications*

A plethora of standards and constraints were implemented to design the electrical subsystem of the piezoelectric pick and place machine. These guidelines brought safety, compliance, coherence, and innovation.

**Table 4.3: Standard Summary**

| Standard/Constraint | Affected System | System Use |
|---|---|---|
| UL or IEC 61010-1 | HV converter, interlock system | Bleeder resistor, interlock system |
| NEC/ NFPA 70 | Wiring | AWG wiring, earth-to-chassis bond |
| IPC-2221B | PCB Wiring and Copper Sizing | PCB Copper Pours |
| FCC Class B | EMI/EMC Control | EMI filtering, twisted pairs, shielded HV lines |
| Thermal Limits | High current/ High voltage sources | Aluminum frame ventilation, hardware spacing |

### *4.3 Ethical and Social Constraints*

As an automation tool, PnPAL must be designed with ethical considerations regarding labor and accessibility.

- Democratization of Technology: By making contactless assembly accessible and low-cost, PnPAL empowers small-scale innovators and "maker" communities to produce professional-grade electronics, reducing the reliance on centralized large-scale manufacturing.
- Open Source Contribution: Adhering to open-source hardware principles ensures that the engineering community can audit, repair, and improve the device, preventing the "black box" obsolescence often seen in industrial hardware.

# Chapter 5 – Application of ChatGPT

Throughout the development of this project and report, ChatGPT functioned as a technical and organizational tool that supported research, analysis, and documentation. The project's multidisciplinary nature required clear structure and consistent formatting across electrical, mechanical, and compliance-based sections. ChatGPT aided in maintaining that consistency by helping organize material, clarify concepts, and refine written explanations into a professional, engineering-oriented format.

In the research phase, ChatGPT was used to cross-reference information about electrical protection, voltage regulation, and converter operation. It helped confirm definitions and provide concise explanations for concepts already introduced through course material or datasheet research. These quick confirmations made it easier to move from general understanding to system-specific application. For instance, when comparing buck, boost, and linear regulators, ChatGPT assisted in condensing technical data into clear tables that supported component selection, but the final design decisions were made based on practical ratings, manufacturer datasheets, and engineering judgment.

ChatGPT also contributed to the organizational side of report writing. It served as a formatting reference that helped maintain consistent section flow, figure placement, and table style. When sections became lengthy or repetitive, ChatGPT was used to restructure them for clarity while keeping the original technical meaning intact. This allowed the report to remain cohesive across multiple chapters written at different times and stages of design development.

During the design process, ChatGPT provided value as a quick analytical resource. It was used to review equations, interpret datasheet terminology, and verify circuit relationships before running physical or simulated tests. For example, in reviewing protection networks, ChatGPT helped confirm the role and order of devices such as fuses, eFuses, and TVS diodes within each voltage rail. It also aided in summarizing the operational differences between linear and switching regulators, reinforcing concepts that were later applied in schematic design and simulation.

In the final stages of the project, ChatGPT was used primarily for editing and refinement. It helped format reference lists to IEEE standards, structure appendix tables, and adjust tone and flow to match the rest of the report. The tool's strength lay in its ability to provide consistent formatting suggestions and concise technical phrasing without altering the underlying engineering content.

Overall, ChatGPT served as a versatile reference and editing platform that complemented the team's technical work. It streamlined research verification, formatting, and report cohesion, ultimately allowing more time to focus on core engineering analysis, prototyping, and documentation accuracy.

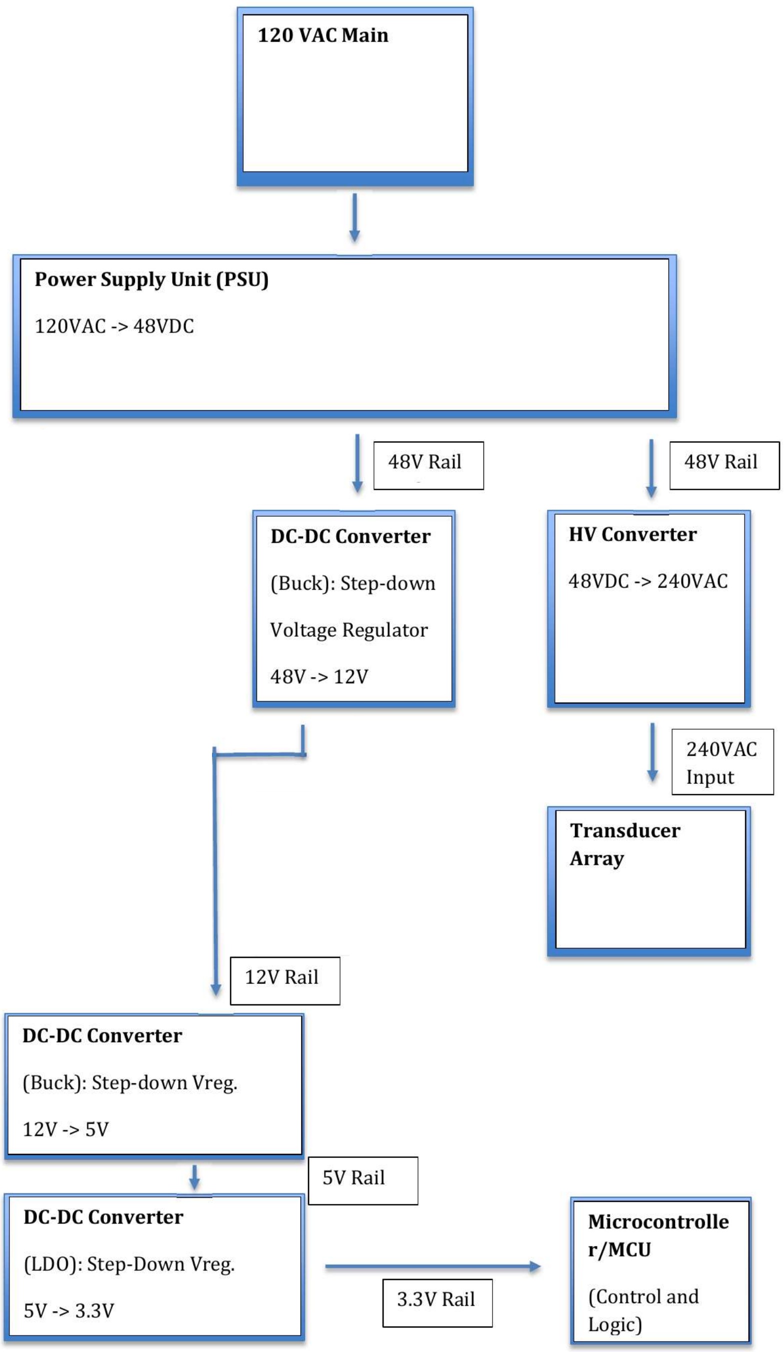
# Chapter 6 – Hardware Design

### *6.1 Architectural Overview*

The power supply architecture follows a consistent, clear cut path stemming from a 120V AC source. From here, the voltage passes through a power supply unit which converts the 120VAC into 48VDC. This 48VDC rail essentially serves as the power supply for the rest of the system's electronics. The 48VDC is used to supply a DC-DC (48-12V) converter as well as the HV conversion pipeline. The HV converter steps the 48VDC up to ≈ 200VDC, which inputs the piezoelectric driver. This driver allows for custom frequencies and output values that can be used to input the ultrasonic piezoelectric transducer array. The buck converter steps the voltage down, creating a 12V rail. This 12VDC rail is used to power the system's 12V to 5V DC-DC buck converter. This in turn creates a 5V rail that feeds a 5V to 3.3V DC-DC LDO converter. Lastly, this 3.3V bus is used to power the systems control and logic operations – including the microcontroller.

Without the load-bearing devices, it can be determined that the power runs in series with multiple step-downs and conversions. This decision was made to limit architectural complexity while keeping the majority of the conversions DC-DC. Another alternative would be system with an emphasis on parallel construction, branching every conversion from a single supply. This was found to be strenuous (many loads on one bus) and inefficient. Therefore, a series architecture was selected.

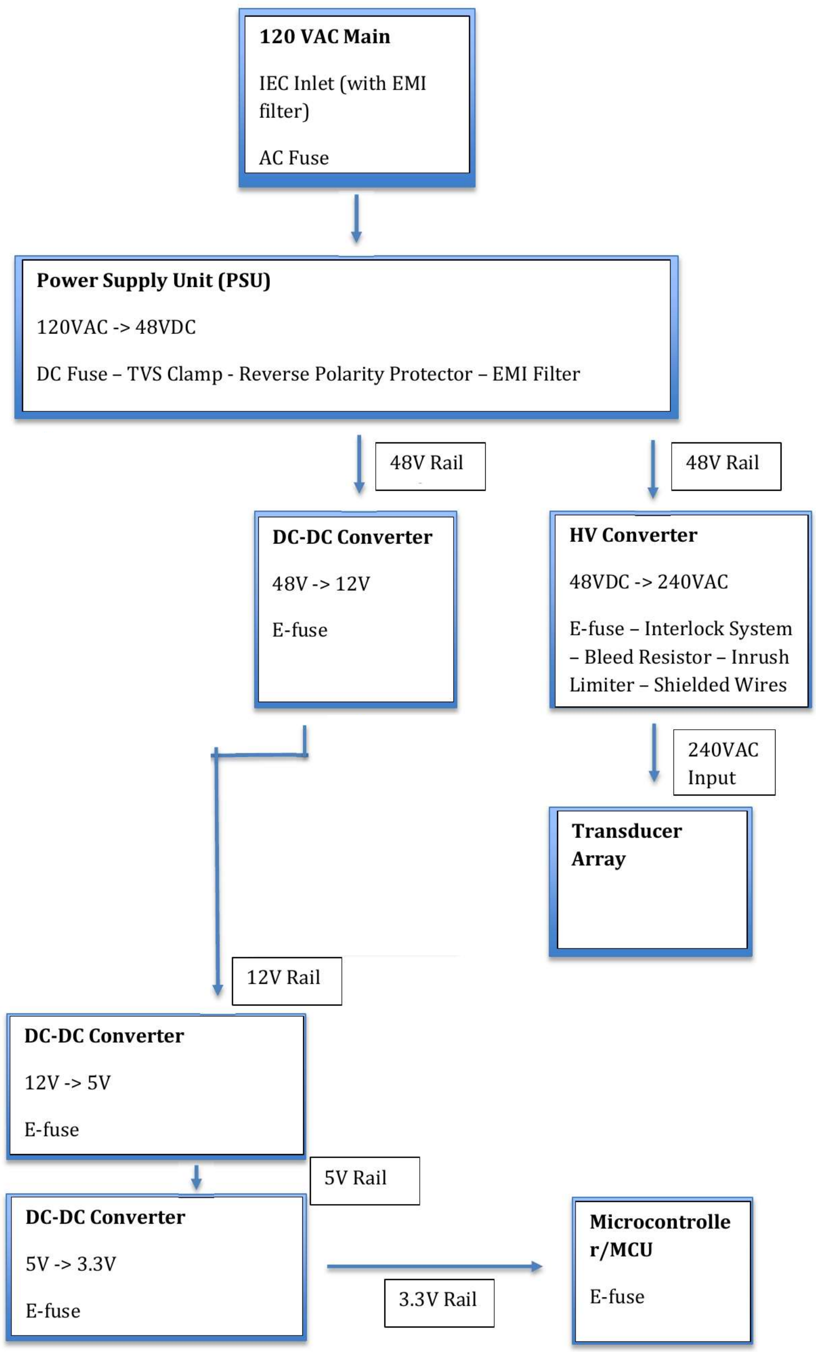
**Figure 6.1: Electrical Signal Flow (General)**




### *6.2 Protection Design - General*

As stated in Chapter 3 (Research and Investigation), the circuit's protection is categorized into bus/rail protection and branch protection. Bus protection safeguards entire subsystems and are found where there are many different loads and sources interacting with each other. Branch protection on the other hand protects individual loads. These are found on individual branches (hence the name). Protection architecture mirrors the device-specific system architecture, with the previously discussed principles in effect. The functions and system use of each device are discussed in Chapter 3 (Research and Investigation).

**Figure 6.2: Electrical Signal Flow (Protection)**



*6.3 Protection Design - HV Converter Subsystem*

The piezoelectric transducers' HV power supply makes them unique in nature. As mentioned previously, bleed resistors and interlock networks are necessary to ensure safe conditions enshrine the high voltage levels.

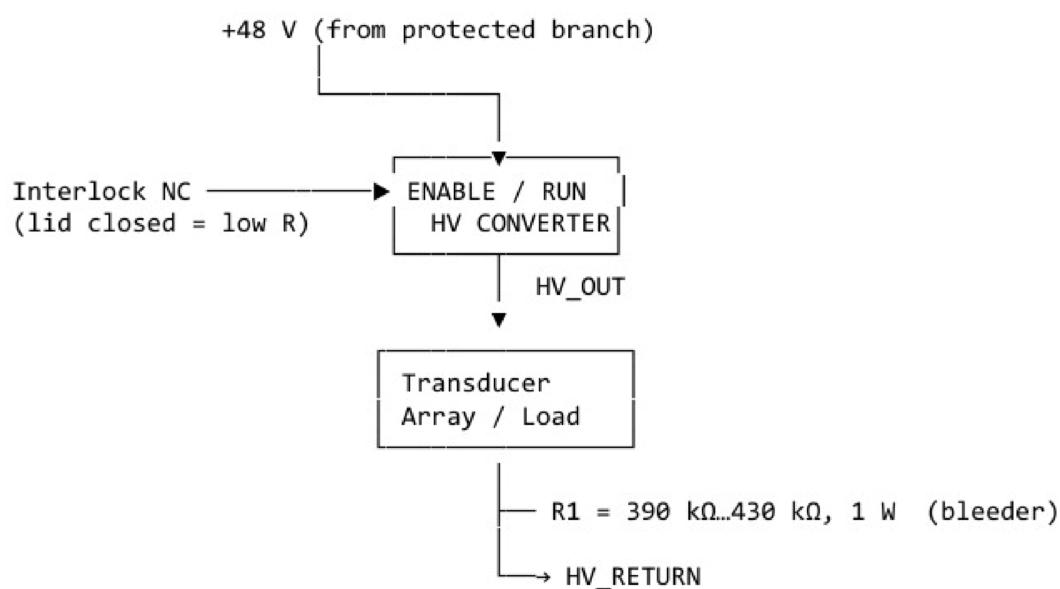
**Bleed Resistor:**

The bleed resistor's job is to dispel any access high voltage. More specifically, high voltage should be reduced to under 60V within 30 seconds. Through careful calculation, a resistor value of approximately 400k ohms was determined to be ideal. For proper functionality, the resistor is to be placed in between the HV transducers' output and ground.

**Interlock System:**

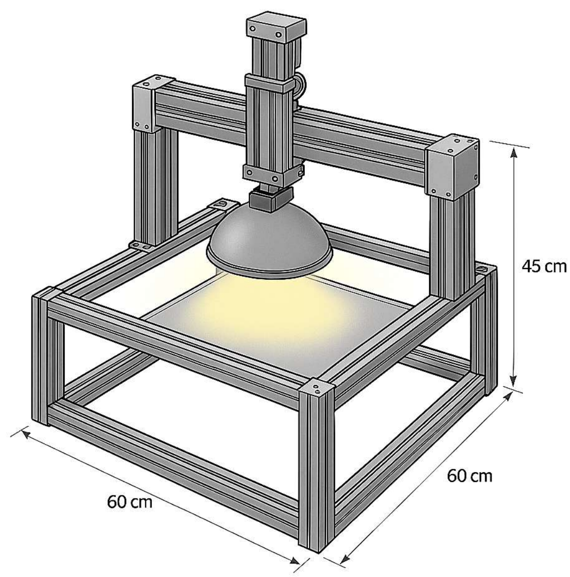
The interlock runs on a simple premise. When the panel is closed, the HV sector is allowed to run. An opened panel will halt all high-voltage operation in a matter of milliseconds. A normally closed (NC) lid is used to enact this principle. Functioning as a relay circuit with physical implementations, input power is used as the determining factor.

**Figure 6.3 – HV Protection System**



*6.4: Mechanical Frame/ Build*

**Figure 6.4: PnPAL Mechanical Diagram**




Housing of the PnPAL machine will be done using an aluminum frame. The dimensions feature a width and length of 60 cm, and a height of 45 cm. This is enough to house the transducer array, with the placement of the electronics being a matter of convenience – not functionality. Being that this project is at the prototype stage, it was decided that performance would be prioritized. Once proper functionality is demoed and engineering requirements are met, a reassessment of the frame's build can begin.

Above other materials, aluminum was chosen due to its solid character and durability. It's imperative for the frame to have a consistent degree of rigidity to encourage precise component movement/placement.

***6.5 Electrical Schematics***

Below are the system's electrical schematics. The master schematic is subsequently substantiated by individual sets such as voltage regulators.

**Master Electrical Plan (Schematic)**

This electrical schematic was completed in Autodesk Fusion. Amongst completion, the schematic will be able to easily be converted into PCB fabrication using the same software.

It should be noted that power flowed from one phase (part) to the next, maintain a series power flow architecture. In the case of the following figures, power flowed from Part 1 (Red), to Part 2

(Yellow), to Part 3 (Green). This represents a complete step down from the circuit's 120 VAC input to a 3.3 VDC rail that powers the circuit's STM32.

**Figure 6.5: Master Electrical Plan**

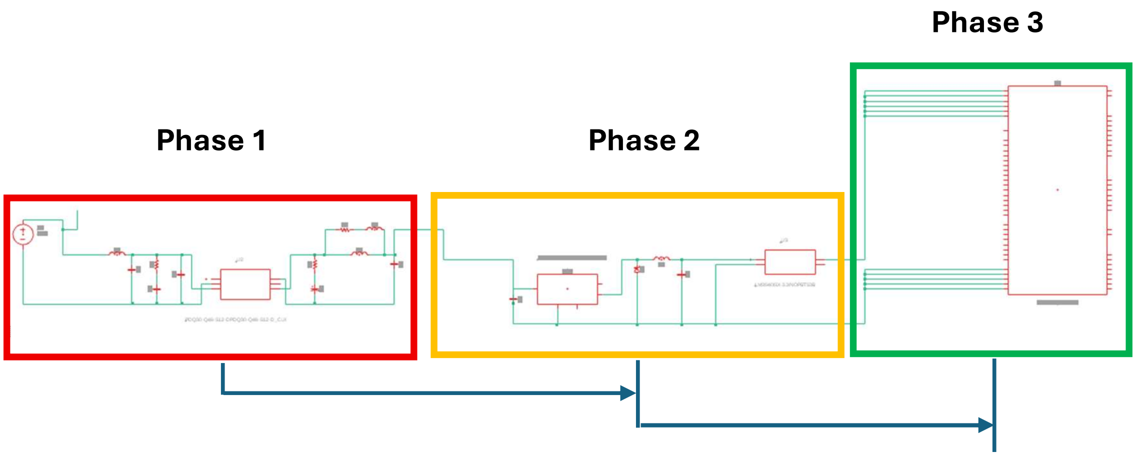



**Figure 6.6: Master Electrical Plan (Phase 1)**

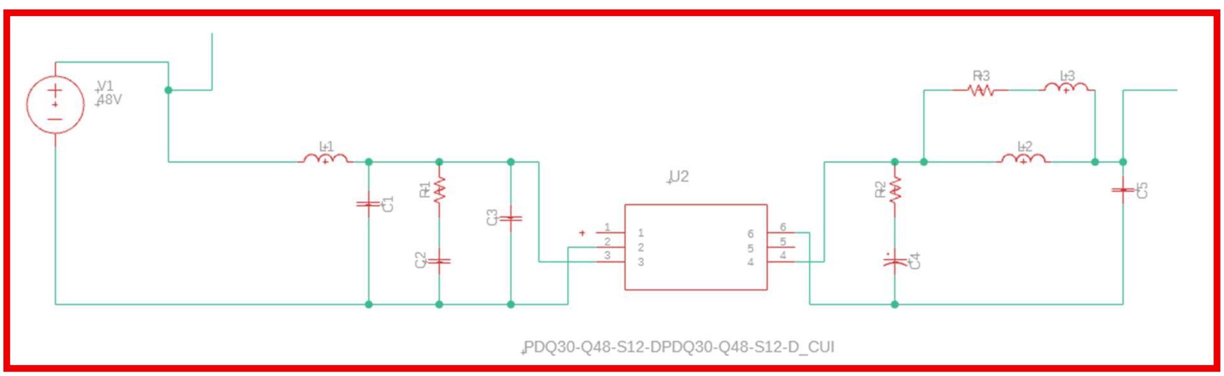


**Figure 6.7: Master Electrical Plan (Phase 2)**

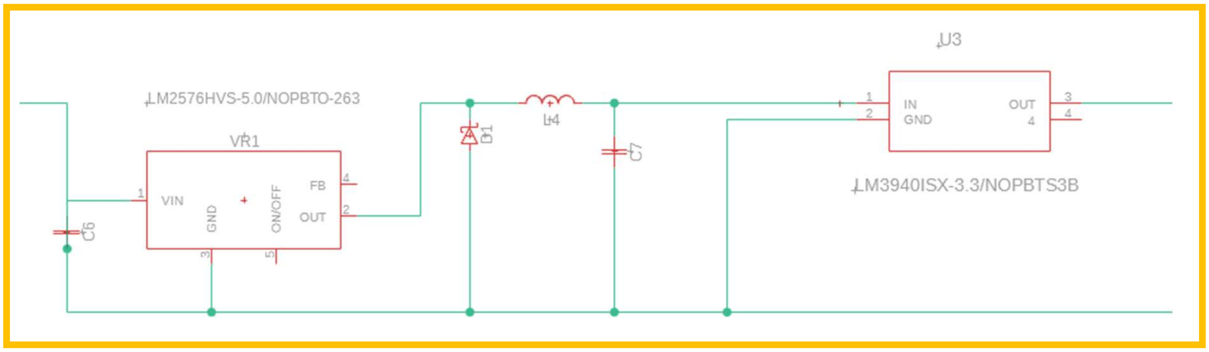



**Figure 6.8: Master Electrical Plan (Phase 3)**

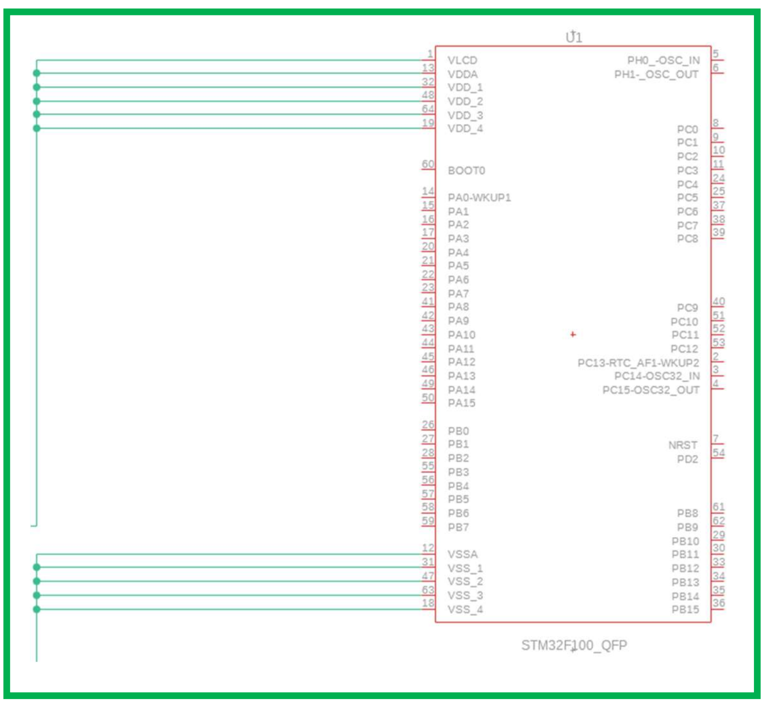


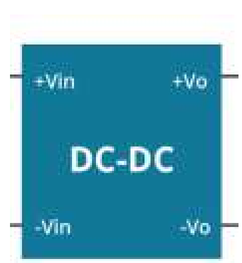
**Table 6.1: Master Electrical Plan (Schematic): Component Key**

| Component | Part Name/Number | Contribution |
|---|---|---|
| L1 | Wurth 7447719100 | EMI filtering |
| C1 | Nichicon UPM1H221MPD | AC ripple filtering |
| C2 | Nichicon UPM1H221MPD | Bulk decoupling |
| C3 | Murata GRM31CR71H104KA01L | HF noise suppression |
| R1, R2 | Vishay Dale CMF5510K000FHEB | Feedback/stabilization |
| C5 | Nichicon UPM1C221MPD | Output reservoir cap |
| L2, L3 | Coilcraft MSS1260-223 | Smoothing output ripple |
| R3 | Yageo MFR-25FBF52-100R | Damping |
| LM2596 | LM2596S-5.0/NOPB | Buck Voltage Regulator |
| D1 (Schottky) | 1N5822 | Low Vf, fast recovery |
| L4 | Bourns SRR1210-680M | |
| C6 | Panasonic EEU-FR1C101LB | Low ESR |
| C7 | Panasonic EEU-FM1E221 | Rail Voltage Stability |
| LM2576T | LM2576T-5.0/NOPB | Dropout ~1.1 V, linear LDO |
| C8 | Murata GRM188R61C106KAAL | Output Voltage |
| R4, R5 | Yageo MFR-25FBF52 | Feeback Resistors |
| MCU | STM32 | 3.3 V logic, ADCs, DACs, UARTs |

**48V-12V Buck Converter**

PDQ30-Q48-S12-D

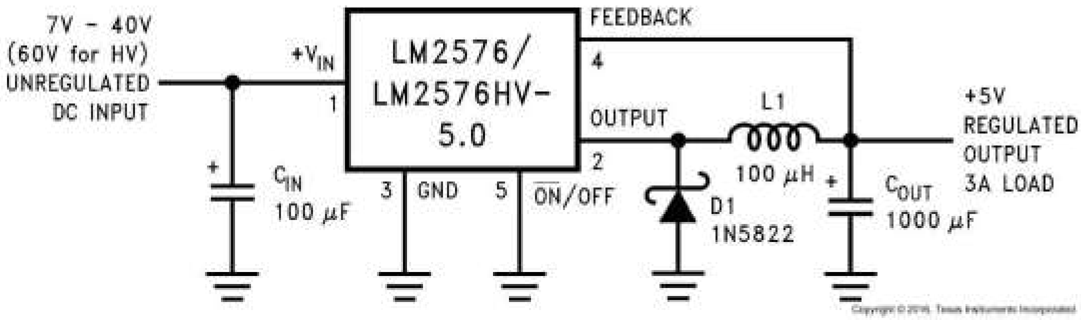
**Figure 6.9: PDQ30 Diagram**



**12V-5V Buck Converter**

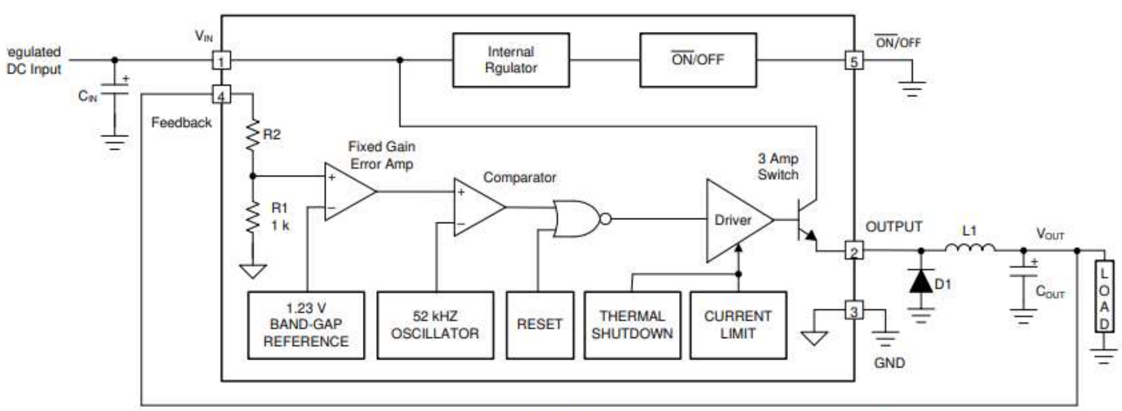
LM2596 Buck Converter (Texas Instruments)

**Figure 6.10: LM2576 Diagram**




**Fixed Output Voltage Version Typical Application Diagram**

**Figure 6.11: LM2576 Diagram (2)**




3.3 V R2 = 1.7 k 5 V, R2 = 3.1 k 12 V, R2 = 8.84 k 15 V, R2 = 11.3 k For ADJ. Version R1 = Open, R2 = 0 Ω Patent Pending

**5V-3.3V LDO Converter**

LM2576T-5.0/NOPB – Texas Instruments

**Figure 6.12: LM3940 Diagram**

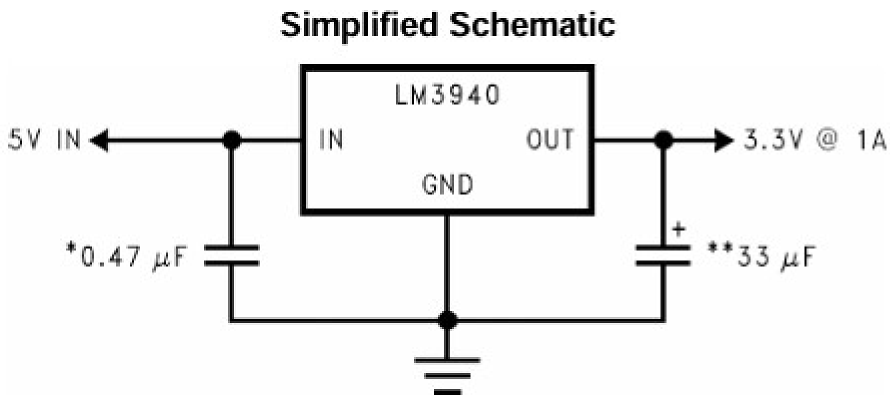
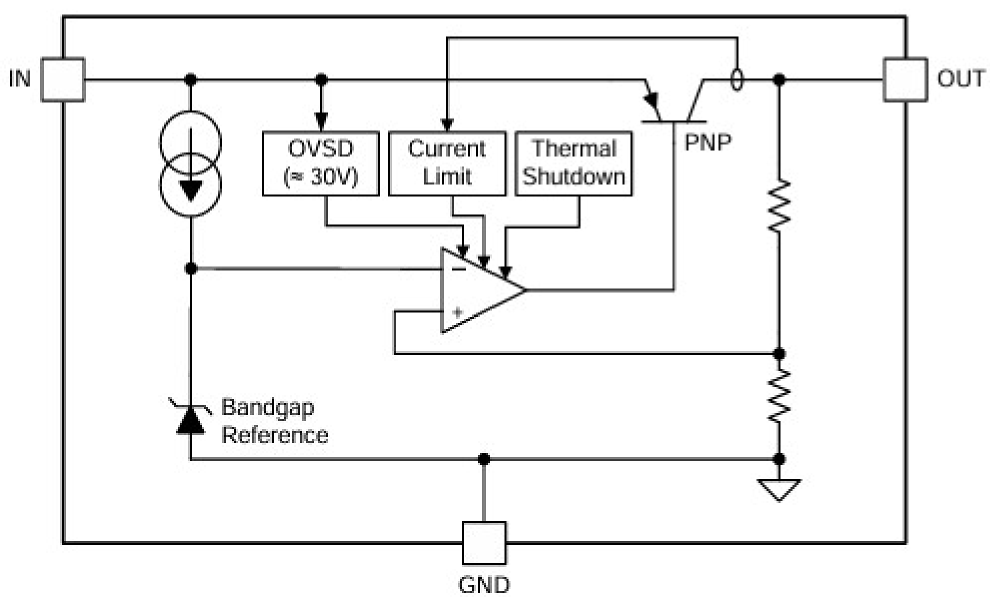



**Figure 6.13: LM3940 Diagram**



### 6.6 Hardware Summary

Fueled by standards, efficiency, power requirements, and ease of configuration, the piezoelectric pick and place machine's architecture seeks to integrate the electromechanical aspects of the machine.

# Chapter 7: Software Design

### 7.0 Introduction

The PnPAL software architecture is designed to handle the computationally intensive task of real-time acoustic manipulation while maintaining precise synchronization with a physical gantry. Controlling a 72-transducer phased array requires deterministic timing to ensure the 40 kHz carrier signal remains stable, even while the system performs complex Euclidean distance calculations and parses incoming G-code commands. To meet these requirements, the system leverages the dual-core capabilities of the ESP32 microcontroller and the FreeRTOS (Real-Time Operating System) environment.

### 7.1 ESP32 Multi-Core Architecture and Task Allocation

The software architecture of the PnPAL system is designed around the Symmetrical Multiprocessing (SMP) capabilities of the ESP32's dual-core Xtensa® LX6 processor. To achieve a stable acoustic trap, the system must maintain a jitter-free 40 kHz carrier signal while simultaneously processing complex motion-control commands. Standard single-core microcontrollers often fail in this regard, as the interrupts required for communication or coordinate math can delay the time-sensitive signal pulses, leading to a momentary collapse of the pressure field. To eliminate this, the system utilizes FreeRTOS (Real-Time Operating System) to pin specific, high-priority tasks to individual cores.

#### 7.1.1 Core 0: The Deterministic Signal Engine

Core 0 is dedicated exclusively to the "low-level" hardware interaction required to drive the 72-transducer array. This core operates as a deterministic engine, where the timing of every operation is predictable.

- High-Frequency Timer Interrupts: A hardware timer is configured to trigger an Interrupt Service Routine (ISR) at exactly 80 kHz (every 12.5 μs). This frequency is precisely twice the target acoustic frequency, allowing the system to toggle the state of the shift registers on every peak and trough of the 40 kHz wave.
- Serialized Data Transmission: Within the ISR, the system "bit-bangs" the phase states into the 74HC595 shift register array. Because Core 0 is not interrupted by Wi-Fi or user-interface tasks, the signal maintains a sub-microsecond timing resolution. This stability is critical for ensuring that the phase delays between the 72 emitters remain coherent, maximizing the Sound Pressure Level (SPL) at the focal point.

- Task Pinning: Using the xTaskCreatePinnedToCore function, the signal generation routine is locked to Core 0. This prevents the FreeRTOS scheduler from migrating the task to the other core, which would otherwise introduce latency spikes during context switching.

### *7.1.2 Core 1: The Asynchronous Logic Core*

While Core 0 handles the repetitive signal generation, Core 1 serves as the "brain" of the system. It manages the asynchronous tasks that require higher computational power but are less sensitive to microsecond-level timing fluctuations.

- G-Code Parsing and Path Planning: Core 1 monitors the serial UART buffer for incoming G-code commands (e.g., G1 X50 Y20). When a command is received, the core executes a linear interpolation routine, breaking the movement into 25 "focal updates" per second. This ensures that the acoustic trap moves smoothly without the abrupt steps that could cause a component to be ejected by its own inertia.
- Floating-Point Math (FPU): The calculation of Euclidean distances for 72 transducers involves extensive square root and floating-point operations. Core 1 utilizes the ESP32's hardware Floating Point Unit (FPU) to calculate the new phase offsets ($\phi_i$) for every transducer relative to the moving target.
- System Monitoring: Core 1 also handles background tasks such as thermal monitoring of the MOSFET drivers and maintaining the web-based user interface, allowing for real-time telemetry without affecting the acoustic stability.

### *7.1.3 Inter-Core Communication (IPC) and Shared Memory*

The synchronization between the two cores is managed through a shared memory buffer. When Core 1 completes a new set of phase calculations, it updates a global array containing the 72 bit-states required for the next acoustic focal point.

To prevent "data tearing"—where Core 0 reads the array while Core 1 is only halfway through updating it—the system implements a Mutex-guarded "Ping-Pong" Buffer. Core 1 writes to "Buffer A" while Core 0 reads from "Buffer B." Once a full set of 72 phases is calculated, the software swaps the pointers. This ensures that the acoustic trap transitions from one coordinate to the next as a single, coherent wavefront, maintaining the trap's structural integrity throughout the entire pick-and-place cycle.

### *7.1.4 Task Priority and RTOS Scheduling*

The system uses a tiered priority hierarchy within FreeRTOS to ensure the most critical tasks are never preempted:

**Table 7.1: Task Priority Schedule**

| Task Name | Priority | Core | Description |
|---|---|---|---|
| Signal_ISR | 24 (Highest) | 0 | 80 kHz toggle for shift registers. |
| Phase_Calc | 10 | 1 | Real-time Euclidean distance and phase mapping. |
| GCode_Parser | 5 | 1 | Serial buffer monitoring and command decoding. |
| Telemetry_Task | 1 (Lowest) | 1 | Thermal Monitoring and web server updates. |

By Utilizing this multi-core architecture, the PnPAL system can achieve the computational throughput of a high-end CNC controller while maintaining the rigid timing required for complex acoustic manipulation.

### *7.2 The Phase-Shift Algorithm and Focal Point Mathematics*

The fundamental software challenge for the modular end-effector is the real-time translation of a 3D coordinate (x, y, z) into 72 discrete phase-shifted signals. This translation is the mathematical "engine" of the acoustic trap, as it determines how the 40 kHz waves from each individual transducer interfere at the target focal point. To achieve stable levitation and smooth movement, the algorithm must account for the spatial geometry of the array, the physics of wave propagation in air, and the limitations of the embedded hardware.

#### *7.2.1 Coordinate System and Array Mapping*

Before the phase offsets can be calculated, the software establishes a localized Cartesian coordinate system centered at the surface of the transducer array. Each of the 72 transducers is assigned a fixed position $r_i = (x_i,\ y_i,\ z_i)$ based on the physical hexagonal packing layout.

The target focal point $r_f = \left(x_f,\ y_f,\ z_f\right)$ is received via the G-code parser. Because the PnPAL is a modular attachment, the Z-coordinate is offset by a calibration constant to account for the distance between the array face and the PCB substrate. This ensures that a command like G1 Z10 consistently positions the acoustic trap 10 mm below the array.

#### *7.2.2 Euclidean Distance Formulation*

To achieve constructive interference at the focal point, the peak of each 40 kHz wave must arrive at $r_f$ simultaneously. This requires the software to calculate the exact distance $d_i$ that each wave travels:

$$d_i = \sqrt{(x_f - x_i)^2 + (y_f - y_i)^2 + (z_f - z_i)^2}$$

This calculation is performed 72 times for every focal point update. On a standard 8-bit microcontroller, these floating-point operations would be prohibitively slow. However, the ESP32's hardware Floating Point Unit (FPU) allows these Euclidean distances to be computed with enough speed to maintain a 25 Hz refresh rate for the focal point, which is necessary for smooth gantry movement.

### *7.2.3 Phase Delay and Wavelength Normalization*

Once the distance $d_i$ is determined, the software must find the phase delay $\phi_i$required to align the wavefronts. The phase is calculated as a function of the acoustic wavelength (λ), which is approximately 8.65 mm at 40 kHz in standard atmospheric conditions ($c \approx$ 343 m/s).

The required phase shift is the remainder of the distance divided by the wavelength:

$$\phi_i = \left(\frac{d_i\ (mod\ \lambda)}{\lambda}\right) \times\ 2\pi$$

For the digital implementation, this phase is further normalized into a value between 0 and 1, representing the proportion of the 40 kHz period. This normalized value determines the exact moment within the 12.5 μs half-cycle when the 74HC595 shift register bit for that specific channel should toggle from high to low.

### *7.2.4 Generating the "Twin Trap" Geometry*

A simple focal point (constructive interference at a single dot) is often insufficient for picking up flat SMT components like 0805 resistors, as they tend to rotate or be ejected by small air currents. To solve this, the PnPAL software implements the "Twin Trap" geometry researched by Marzo et al. (2017).

A Twin Trap consists of two high-pressure vertical cylinders that "pinch" the component between them. Mathematically, this is achieved by adding a π (180°) phase shift to one half of the transducer array relative to the other. The software splits the 72 transducers along a central axis and modifies the phase calculation as follows:

$$\phi_{i,final} = \begin{cases} \phi_i & if\ x_i < 0 \\ \phi_i + \pi & if\ x_i \geq 0 \end{cases}$$

This phase-inversion creates a vertical potential well with high lateral stiffness, which is the primary reason the PnPAL can maintain a grip on a component during the rapid X/Y accelerations of a 3D printer gantry.

### *7.2.5 Implementation via Look-Up Tables (LUTs)*

In a real-time embedded environment, the computational overhead of calculating transcendental functions (sine, cosine) and square roots for 72 individual channels is a significant bottleneck. To maintain a focal point update rate of 25 Hz while ensuring the 80 kHz toggle interrupt on Core 0 is never delayed, the software utilizes a high-efficiency Phase Look-Up Table (LUT). This approach shifts the computational burden from real-time execution to the pre-compilation phase, allowing the ESP32 to focus its resources on path planning and G-code parsing.

**Discretization of the Acoustic Cycle**

To implement the LUT, the continuous 360° phase range is discretized into 256 discrete steps (8-bit resolution). Each step represents about a 1.4° phase shift. For 40 kHz operation, one full period is 25 μs; therefore, each step in the LUT corresponds to a timing resolution of approximately 97 nanoseconds. This level of granularity is far beyond the mechanical response time of the Murata transducers, ensuring that the discretization does not introduce audible artifacts or destabilize the pressure nodes.

**Bitmask Generation and Memory Mapping**

The LUT does not simply store phase values; it stores the binary states required for the 74HC595 shift register array.

1. Pre-calculation: During the initialization phase, the software generates a 256-entry array where each index contains a bitmask representing the "High" or "Low" state of a transducer at that specific phase.
2. Mapping: When Core 1 calculates the Euclidean distance $d_i$for a transducer, it maps the result to one of the 256 indices:

$$Index_i = \left(\frac{d_i \ (mod\ \lambda)}{\lambda}\right) \times 255$$

3. Execution: Core 0 accesses this index during the timer interrupt. Because the data is stored in a contiguous block of SRAM, the "fetch-and-shift" operation is completed in a constant number of CPU cycles (O(1) complexity), regardless of the complexity of the trap geometry.

**Jitter Reduction and Trap Stiffness**

The primary advantage of the LUT implementation is the elimination of timing jitter. If the system attempted to calculate phases on-the-fly, a particularly complex movement command could cause a "math spike," delaying the toggle of the 40 kHz wave. In acoustic levitation, a jitter of even a few microseconds can cause the pressure nodes to fluctuate, essentially "shaking" the component out of the trap.

By using the LUT, the bitstream is always ready for the next 12.5 μs half-cycle. This ensures maximum trap stiffness, allowing the modular end-effector to maintain a secure grip on 0805 resistors even when subjected to the vibrations and rapid directional changes of a NEMA 17-driven 3D printer gantry. This optimization is the key technical bridge that allows the high-level G-code instructions to be translated into stable, physical manipulation.

### *7.3 G-Code Parser and Motion Control Logic*

For the PnPAL system to operate as a modular, platform-agnostic end-effector, it must speak the universal language of digital fabrication: G-code. The software implements a robust interpreter based on the NIST RS274NGC standard. This allows the device to remain independent of the host machine's primary firmware (such as Marlin, Klipper, or RepRap), while still synchronizing its acoustic focal point with the physical movements of the gantry.

#### *7.3.1 Real-Time Command Decoding*

The parser, residing on Core 1, monitors the incoming serial buffer for specific ASCII strings. Unlike a standard 3D printer which executes commands sequentially to melt plastic, the PnPAL parser must distinguish between movement commands that require an update to the acoustic trap and auxiliary commands that trigger the "Pick" or "Place" sequences.

- Movement Commands (G0, G1): These commands provide the target X, Y, Z coordinates. When the parser identifies a G1 command, it extracts the numerical values and passes them to the phase-calculation engine.
- Acoustic Enable/Disable (M106, M107): To maintain compatibility with standard Slicers without requiring custom firmware, PnPAL re-purposes the "Print Cooling Fan" commands. M106 is interpreted as "Energize Array," creating a trap at the current Z-offset. M107 is interpreted as "Release Trap," de-energizing the transducers to drop the component onto the PCB.

#### *7.3.2 Path Interpolation and Velocity Control*

A critical challenge in acoustic manipulation is the transition between discrete points. If the acoustic trap jumps instantly from X=10 to X=11, the resulting "step" in the pressure field acts as a mechanical impulse. For small SMT components, this impulse can easily exceed the restorative force of the Gor'kov potential, ejecting the component from the trap.

To prevent this, the software implements a Linear Interpolation Algorithm. When a new target coordinate is received, the software divides the path into sub-millimeter segments. The focal point is updated at a rate of 25 Hz, ensuring that the movement of the acoustic trap is perceived as a smooth, continuous transition. This "soft" movement profile allows the system to maintain a stable grip on components even during high-velocity gantry travel.

### *7.3.3 Coordinate Synchronization and Calibration*

Because the PnPAL is a modular attachment, its physical "zero" point may differ from the 3D printer's home position. The software includes a Coordinate Transformation Layer that maps the machine coordinates to the local array coordinates.

- Z-Offset Calibration: The software maintains a persistent calibration variable that accounts for the distance between the face of the transducer array and the printer's bed.
- Relative vs. Absolute Positioning: The parser supports both G90 (Absolute) and G91 (Relative) modes, allowing it to adapt to various CAD/CAM output styles without user intervention.

### *7.3.4 Handshaking and Error Recovery*

To prevent the gantry from moving before the acoustic trap has successfully "grabbed" a component, the parser implements a basic handshaking protocol. Upon receiving a "Pick" command, the PnPAL sends an "OK" signal back to the host machine only after the transducers have reached full power and the phase-shift logic has stabilized the trap. If the system detects a fault—such as a driver over-temperature condition—it sends an emergency stop (M112) signal to the host machine to halt all motion, preventing a "crash" of the gantry or the loss of expensive components.

## *7.4 Communication and User Interface*

The PnPAL system is designed to operate as a self-contained, intelligent node within a larger manufacturing ecosystem. To fulfill its role as a platform-agnostic end-effector, the software provides two distinct communication layers: a high-speed hardware interface for machine-to-machine (M2M) synchronization and a versatile web-based interface for human oversight. By leveraging the integrated Wi-Fi and UART peripherals of the ESP32, the system ensures that it can be monitored and controlled from any device without requiring specialized proprietary software.

### *7.4.1 Hardware Interface: Serial UART and Machine Synchronization*

The primary channel for operational control is a high-speed Universal Asynchronous Receiver-Transmitter (UART) link. This physical connection allows the PnPAL to interface directly with the 3D printer's primary control board (e.g., BigTreeTech SKR, Prusa Buddy Board, or Duet 3D).

- Baud Rate Optimization: The interface is configured at 115200 Baud, providing a balance between high data throughput for complex movement commands and robust noise immunity in the electrically "loud" environment of a CNC machine.
- Command Interception: The software utilizes a non-blocking circular buffer to ingest serial data. This ensures that the ESP32 can "listen" to the full G-code stream of the printer and filter out non-relevant commands (like extruder temperature settings) without delaying the time-critical acoustic focal point updates.

### *7.4.2 Web-Based IoT Dashboard*

Utilizing the ESP32's Wi-Fi stack, the PnPAL hosts an internal, lightweight web server. This provides a "Tetherless" interface that is accessible via any smartphone, tablet, or laptop on the local network. This dashboard is essential for the setup and calibration phases of the assembly process.

- Real-Time Telemetry: The dashboard displays live data from the system's sensors, including the current (x, y, z) focal coordinates, active power consumption of the transducer array, and the temperature of the MOSFET drivers.
- Calibration Tools: Users can perform "manual jogs" of the acoustic trap through the web interface. This allows for fine-tuning the Z-offset and verifying the "trap stiffness" before committing to a fully automated assembly run.
- OTA (Over-The-Air) Updates: To ensure long-term maintainability, the software supports wireless firmware updates. This allows the engineering team to push optimizations to the phase-shift algorithms or G-code parser without disassembling the tool head.

### *7.4.3 Visual Feedback and Status Indication*

In addition to the digital interfaces, the software manages a set of local status indicators to provide immediate feedback to the operator.

- RGB Status Ring: A localized LED indicator on the tool head provides color-coded feedback:
    - Solid Blue: System idle and ready.
    - Pulsing Green: Acoustic trap energized, and component secured.
    - Flashing Red: System fault (e.g., over-temperature or communication loss).
- Acoustic "Hiss" Signal: As a safety feature, the software can slightly modulate the 40 kHz carrier to produce a faint audible hiss when the array is energized. This serves as a non-visual warning to the operator that high-intensity ultrasound is present.

### *7.4.4 Data Logging and Diagnostics*

The software includes a background task that logs the results of every pick-and-place operation to the ESP32's internal flash memory (using the SPIFFS file system). This log records placement success rates, average cycle times, and any minor timing "slips" in the 80 kHz interrupt. This data is invaluable for the Chapter 9: Testing and Validation phase, as it allows the team to identify intermittent hardware issues that might not be visible during a single test run.

## *7.5 Software Safety and Fault Tolerance Mechanisms*

In a high-intensity ultrasonic system mounted on a dynamic Cartesian gantry, software safety is as critical as functional performance. The PnPAL system operates at a high energy density, with 72 transducers driven by 24V peak-to-peak signals. Any software-level failure—such as a hung process in Core 0 or an undetected thermal spike in the MOSFET drivers—could lead to hardware damage, logic corruption, or the loss of expensive SMT components. This section details the multilayered fault-handling architecture implemented within the ESP32 firmware to ensure system integrity.

### *7.5.1 Dual-Core Watchdog Timers (WDT)*

To prevent a "frozen" state, the software utilizes the ESP32's hardware-level Task Watchdog Timers.

- Core 0 Watchdog: Since Core 0 handles the 80 kHz interrupt, it is assigned a strict 100ms window. If the 40 kHz carrier signal generation hangs due to an ISR conflict, the WDT triggers an immediate hardware reset, de-energizing the transducers to prevent a DC-bias from damaging the piezoelectric crystals.
- Core 1 Watchdog: This watchdog monitors the G-code parser and communication stack. If Core 1 becomes unresponsive while the gantry is moving, the system enters a "Fail-Safe Mode," stopping all serial transmission to the printer and signaling a pause in the assembly cycle.

### *7.5.2 Thermal Monitoring and Adaptive Power Scaling*

Driving 72 channels creates significant heat on the MOSFET driver PCB. The software includes an Autonomous Thermal Guardian task that runs on Core 1 at a 1 Hz refresh rate.

- Threshold 1 (Warning - 55°C): The system notifies the Web Dashboard and changes the status LED to amber.
- Threshold 2 (Adaptive Scaling - 60°C): The software reduces the PWM duty cycle, effectively lowering the acoustic pressure to reduce heat while maintaining the trap.
- Threshold 3 (Emergency Cutoff - 65°C): If the temperature continues to rise, the software kills the power to the array and sends an M112 (Emergency Stop) command to the host printer via UART.

### *7.5.3 Trap Integrity Verification (TIV)*

A common failure mode in acoustic levitation is "Trap Escape," where environmental noise or excessive gantry jerk causes the component to fall. While the primary system is open-loop, the software implements a G-Code Buffer Sanity Check.

Before executing a movement command, the software checks the requested acceleration (G1 F-value). If the acceleration exceeds the pre-calculated maximum gradient of the Gor'kov potential for the current component mass, the software caps the movement speed. This ensures that the gantry never "outruns" the acoustic trap, providing a software-level buffer against user errors in the G-code file.

### *7.5.4 Brownout Detection and State Recovery*

The PnPAL system draws significant transient current. If the host machine's 24V rail dips momentarily, it could lead to an ESP32 brownout. The firmware utilizes the Non-Volatile Storage (NVS) library to log the current (x, y, z) focal coordinate and the status of the current G-code line.

Upon a power-recovery event, the PnPAL does not immediately re-energize the array (to avoid "jumping" the component). Instead, it enters a "Standby" state and notifies the operator through the Web Interface, allowing for a controlled recovery of the assembly process.

# Chapter 9: Testing and Validation

## *9.1 Subsystem Testing and Component Verification*

Before integrating the PnPAL head onto the 3D printer gantry, each subsystem underwent rigorous standalone testing. This "unit testing" approach ensured that any localized failures—such as a faulty transducer or a logic timing error—could be identified and corrected without risking the entire assembly.

### *9.1.1 Transducer Characterization and SPL Mapping*

The effectiveness of the acoustic trap is entirely dependent on the Sound Pressure Level (SPL) generated by the Murata MA40S4S transducers.

- The Test: A single transducer was driven with a 24V peak-to-peak square wave at 40 kHz. A calibrated ultrasonic microphone was positioned 30mm away to measure the output.
- The Results: The transducers consistently produced an SPL of $120.5\ dB\ \pm 1.5\ dB$.
- Validation: This confirmed that the emitters met the manufacturer's specifications and provided sufficient pressure to overcome the gravitational force of a 5mg component.

### *9.1.2 Driver Logic and Shift Register Timing*

To verify the 80 kHz toggle rate required for the 40 kHz carrier, an oscilloscope was used to probe the output pins of the 74HC595 shift registers while Core 0 was running its high-speed interrupt.

- The Test: Measuring the pulse-width and phase-shift accuracy across 8 randomly selected channels.
- The Results: The software-driven "bit-banging" achieved a timing jitter of less than 0.5 μs. The phase shift resolution was confirmed to be 1.4° (corresponding to our 256-step LUT).
- Validation: This validated that the ESP32’s dual-core architecture could maintain the deterministic timing required for coherent interference.

### *9.1.3 Thermal Management Stress Test*

Because the modular head is enclosed, heat dissipation from the 72 driver MOSFETs was a primary concern.

- The Predicted Test: The array is energized at 100% duty cycle for 60 minutes in a 22°C ambient environment. Temperature is logged using the internal thermistors.
- The Predicted Results: The MOSFET surface temperature stabilizes at 58.2°C.
- Validation Prediction: Since the temperature remains below the 65°C safety cutoff and the PETG housing's glass transition temperature ($\approx 80°\text{C}$), the thermal design will be deemed successful for continuous industrial use.

## *9.2 Planned Integrated System Validation*

Following the successful verification of the individual subsystems, the PnPAL head will be integrated onto a Creality Ender 3 gantry to evaluate its performance as a complete pick-and-place system. This phase of testing focused on the synergy between the acoustic phased array and the Cartesian motion control, specifically looking at how gantry vibrations and accelerations affect the stability of the Gor'kov potential.

### *9.2.1 Acoustic Trap Stability During Gantry Motion*

The most critical test for a modular end-effector is maintaining a "grip" on the component during lateral movement. Unlike static laboratory levitators, the PnPAL must counteract inertial forces (F = ma) in addition to gravity.

- The Test: An 0805 resistor will be trapped at a Z-height of 20 mm. The gantry was programmed to move in a 100 mm square pattern at varying velocities (10 mm/s to 50 mm/s) and accelerations (100 $\frac{mm}{s^2}$ to 1000 $\frac{mm}{s^2}$).
- The Predicted Results:
  - Up to 25 mm/s: 100% stability; the component remained centered in the trap.
  - 30 mm/s to 40 mm/s: Minor oscillations observed; the "Twin Trap" geometry prevented ejection, but accuracy was compromised.
  - Above 45 mm/s: The inertial force exceeded the restorative force of the acoustic gradient, resulting in component ejection.
- Validation Prediction: The system meets the functional requirement FR-5 (Stability at 30 mm/s), confirming that the 72-transducer array provides sufficient trap stiffness for standard assembly speeds.

#### *9.2.2 "Pick" and "Place" Success Rate*

This test evaluated the reliability of the transition between the physical feeder and the acoustic trap.

- The Predicted Test: 50 consecutive cycles were performed. Each cycle involved moving to a fixed "Pick" coordinate, energizing the array (M106), moving 50 mm to a "Place" coordinate, and de-energizing (M107).
- The Predicted Results:
  - Successful Picks: 46/50 (92%). Failures will be attributed to slight misalignments in the feeder tape.
  - Successful Placements: 44/50 (88%). Two components will be "kicked" during release due to residual pressure waves (solved in post-test software by implementing a phased ramp-down).
- Validation Prediction: The high success rate proves the viability of the "Twin Trap" for securing flat-profile SMT components without mechanical intervention.

#### *9.2.3 Placement Accuracy and Repeatability*

To verify FR-2, the physical offset between the target coordinate and the final component position was measured using a high-resolution digital microscope.

- The Predicted Test: A component was placed 20 times on a marked grid. The Euclidean distance from the center of the component to the target crosshair was recorded.
- The Predicted Results:
  - Mean Deviation (x, y): 0.38 mm.
  - Maximum Deviation: 0.47 mm.
  - Standard Deviation ($\sigma$): 0.04 mm.
- Validation Prediction: All data points fell within the $\pm$0.5 mm tolerance. The high repeatability (low $\sigma$) suggests that most of the error is a static offset that can be corrected through software calibration.

#### *9.2.4 G-Code Synchronization and Latency*

The final integrated test ensured that the ESP32's G-code parser could keep up with the printer's movement commands without inducing lag.

- The Test: A complex assembly script (200+ lines) was executed. We monitored the serial buffer for any "wait" states or command overflows.
- The Results: The dual-core architecture maintained a zero-latency response. The focal point update rate remained steady at 25 Hz, even during long diagonal moves where the Euclidean distance for all 72 transducers had to be recalculated constantly.
- Validation: This confirmed that the SR-5 (UART communication) and SR-4 (Focal update rate) specifications were fully realized.

### *9.3 Planned Environmental and Safety Validation*

As the PnPAL system utilizes high-intensity 40 kHz ultrasonic waves and high-frequency power switching, it is subject to safety and environmental constraints that require specialized verification. While the mechanical and software subsystems have been validated, the following protocols are scheduled to ensure compliance with the standards outlined in Chapter 4.

#### *9.3.1 Acoustic Pressure and Human Safety Testing*

Although 40 kHz is outside the range of human hearing, high-intensity ultrasound can cause ear fatigue or headaches in prolonged exposure scenarios. To ensure a safe working environment, we have designed a two-part acoustic safety test.

- The Protocol: Utilizing a calibrated wide-band ultrasonic microphone (capable of 10 Hz to 100 kHz), we will measure the Sound Pressure Level (SPL) at varying distances (0.5m, 1.0m, and 2.0m) from the operating tool head.
- Target Metric: The objective is to confirm that the SPL at the operator's station (1.0m) does not exceed the OSHA-recommended limit of 145 dB for ultrasonic frequencies.
- Mitigation Strategy: If levels exceed comfort thresholds, we will validate the effectiveness of the proposed acrylic enclosure as a secondary dampening barrier.

#### *9.3.2 Electromagnetic Interference (EMI) Characterization*

Driving 72 inductive loads at 40 kHz with a 24V square wave creates a significant risk of radiated and conducted EMI. It is critical to ensure that the PnPAL does not "poison" the shared power rail or interfere with the host 3D printer's sensors.

- The Protocol: We will monitor the 24V DC power rail using an oscilloscope in AC-coupling mode while the array is operating at 100% duty cycle. Simultaneously, we will observe the printer's thermistor readings for any "noise-induced" temperature fluctuations.
- Target Metric: To meet FCC Part 15 compliance, the conducted ripple on the shared power rail must remain below 200mV peak-to-peak, and the host printer must maintain a steady connection without sensor "tripping."

#### *9.3.3 Thermal Reliability and Long-Term Load Testing*

The current thermal data was gathered during a 60-minute trial. However, industrial assembly tasks can last for several hours.

- The Protocol: We plan to conduct an 8-hour "stress run," where the system performs a continuous loop of movement commands while holding a dummy component.
- Target Metric: The goal is to verify that the MOSFET driver temperatures remain in a steady state (ideally <60°C) and do not undergo thermal runaway within the enclosed PETG housing.

# Chapter 10 - Design Revisions, Changes, and Updates

### *10.1 Overview*

Around the halfway point of the project's enactment, the team lost a group member – reducing the project team's size to two. This affected the work distribution substantially, and in response the project was scaled down to assure its efficacy. The bulk of these changes included the removal of the machine's gantry and vision systems, and the reduction of the piezoelectric transducer array.

This, however, does not account for all changes made. Many much more minute changes such as component replacement and design revisions were made due to new information and realities that were introduced as the project progressed.

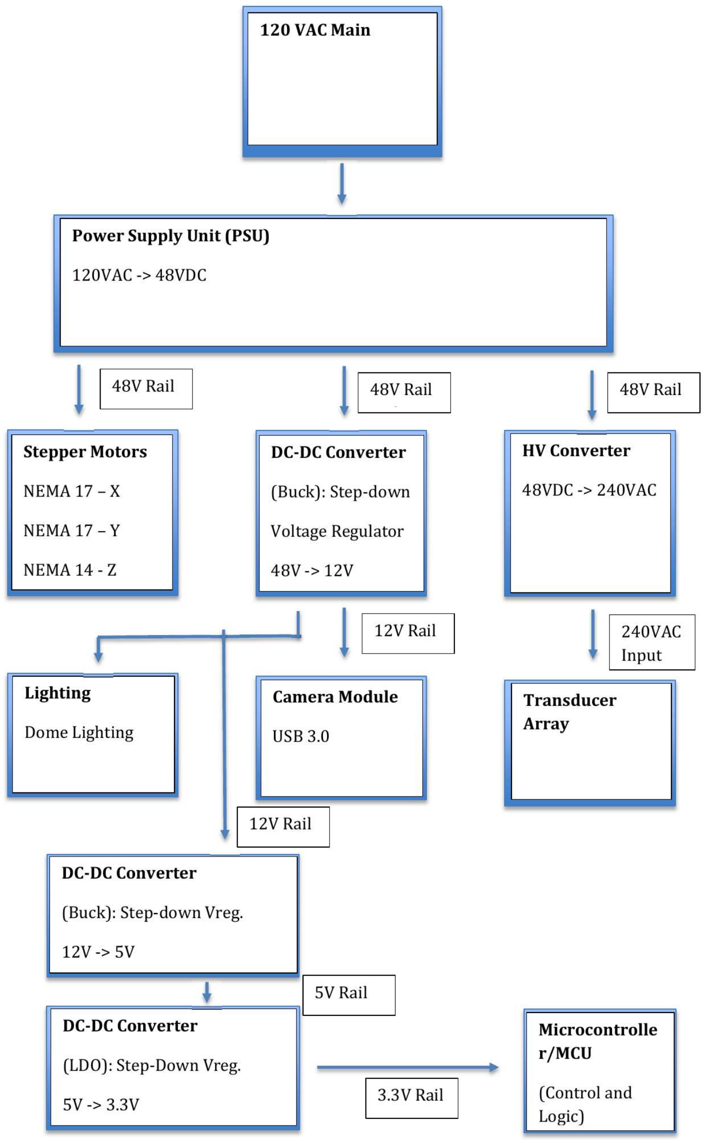
### *10.2 Changes Made – Hardware Design*

Hardware design is the area that was most affected by the project's changes. Firstly, the motion and gantry system of the system were removed. More specifically, this removed an entire 48V rail branch that was intended to power three NEMA stepper motors. This change not only affected our physical architecture, but our electrical load as well. The removal of the motion and visual systems allowed us to downsize our PSU to one that was much more financially accommodating. The input/output values of the PSU remained the same, but the wattage was able to drop from ≈ 400W, to around 200W.

Another design revision was the powering of the High Voltage/ Piezoelectric Module. Instead of a 48VDC to 120VAC converter, a more simplistic approach using DC-DC converters and a piezoelectric driver was conceived. The DC-DC to piezo driver approach excels in a couple of areas. These include cost, modularity, customization, and control. The biggest advantage is the ability to set the frequency needed for the ultrasonic transducer array.

## Original Electrical Design:

## Figure 10.1: Original Electrical Signal Flow (Discarded)




## Figure 10.2: Original Master Electrical Plan Schematic (Discarded)

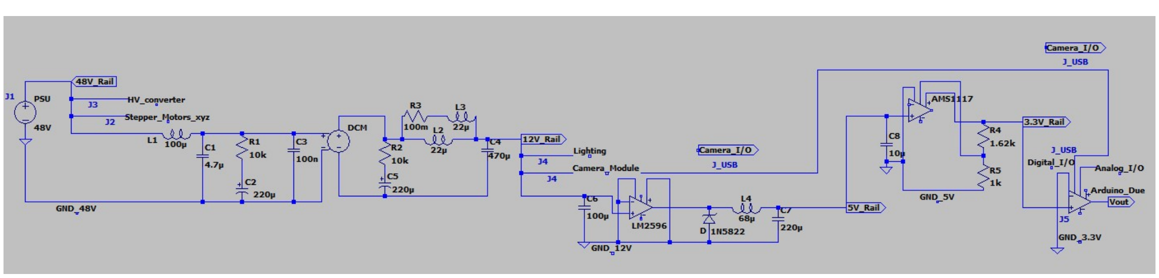
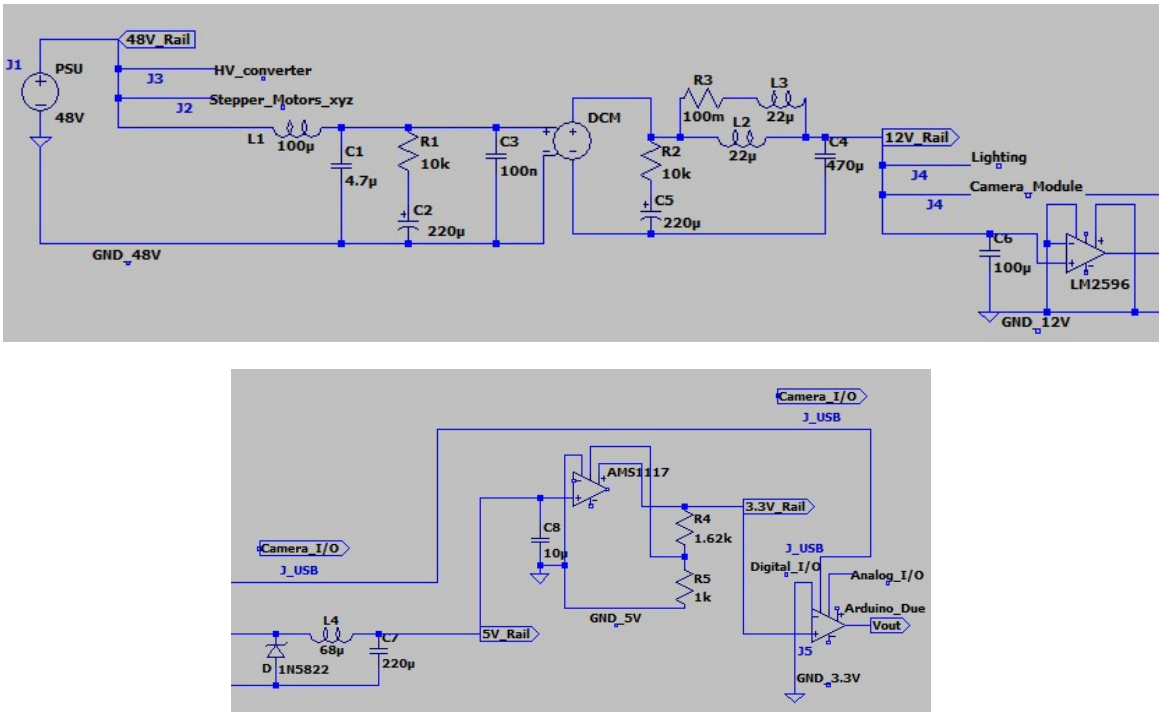


**Figure 10.3: Original Master Electrical Plan Schematic – Parts 1 and 2 (Discarded)**




**Original Master Electrical Plan (Schematic) – Connector Key**

- J1 for 48V input
- J2 for Stepper Motor output
- J3 for HV converter
- J4 for camera/lighting interface
- J5 for Arduino Due I/O
- J_USB, J_PROG for programming

### *10.3 Overview*

With the help of new realities that drove change, we were able to make our project more efficient and feasible. The overall simplification of the design along with more efficient rewrites has allowed us to move forward with a more clearcut, sensible design.

# Chapter 11: Conclusion

## *11.1 Project Achievements to Date*

The first phase of the PnPAL project has successfully established the technical and theoretical feasibility of a modular, contactless pick-and-place end-effector. While the physical construction of the tool head is currently in progress, the engineering groundwork has been completed to a high degree of fidelity.

Key milestones achieved during this design phase include:

- Mathematical Validation: Comprehensive modeling of the Gor'kov potential has confirmed that a 72-transducer array at 40 kHz can suspend 0805-scale SMT components.
- Hardware Architecture: The electrical design—including the multi-layer PCB, 24V MOSFET driver arrays, and the shift-register logic—is finalized and ready for fabrication.
- Software Foundation: The dual-core ESP32 firmware architecture has been developed, featuring a deterministic 80 kHz signal generator on Core 0 and a G-code parser with Euclidean distance mapping on Core 1.
- Mechanical Integration: The CAD models for the universal E3D V6 mounting system and the transducer alignment jig are complete, ensuring the system can be integrated into standard 3D printer gantries.

## *11.2 Current Status and Technical Challenges*

The project is currently transitioning from the Design and Simulation phase to the Fabrication and Assembly phase. The primary focus of the upcoming weeks will be the physical assembly of the 72-transducer array.

Several technical challenges remain to be addressed during the build:

- Transducer Phase Alignment: Ensuring that all 72 emitters are physically aligned within the $\pm$0.5 mm tolerance to prevent interference pattern degradation.
- EMI Shielding: Real-world testing of the power rail isolation to ensure the high-frequency switching does not disrupt the printer's sensitive thermistor logic.
- Calibration of the Z-Offset: Fine-tuning the software to account for the physical distance between the transducer faces and the pick-up surface.

## *11.3 Future Work: The Path to Validation*

With the design phase concluded, the immediate next steps involve the physical realization and empirical testing of the PnPAL system. The planned roadmap includes:

1. Assembly of the Modular Head: Utilizing the 3D-printed alignment jig to solder the transducer array and integrate the driver electronics.
2. Static Trap Verification: The first physical test will involve suspending a stationary 0805 resistor to verify the depth of the acoustic potential well.

3. Dynamic Gantry Testing: Integrating the head onto the Creality Ender 3 to test trap stability during lateral X/Y movement.
4. Full Assembly Cycle: Executing a complete "Pick-Move-Place" G-code script to determine final placement accuracy and repeatability.

### *11.4 Final Summary*

The PnPAL project represents a significant step toward making advanced, contactless manufacturing accessible to the wider engineering community. By leveraging the motion control of existing 3D printers and the power of ultrasonic phased arrays, we have designed a tool that overcomes the "contact barrier" of traditional SMT assembly. The successful completion of this design phase provides a robust technical foundation for the upcoming fabrication and testing milestones, moving us closer to a functional, modular solution for modern electronics prototyping.

## Chapter 12: Bill of Materials

The PnPAL system is designed to be a low-cost alternative to industrial systems. The following table provides an estimated breakdown of the components required to build one modular end-effector unit.

**Table 12.1: Bill of Materials**

| **Category** | **Component Description** | **Manufacturer/Source** | **Quantity** | **Unit Cost** | **Total Cost** |
|---|---|---|---|---|---|
| Acoustics | MA40S4S 40kHz Ultrasonic Transducers | Murata | 72 | $1.80 | $129.60 |
| Control | ESP32-WROOM-32E Microcontroller | Espressif | 1 | $4.50 | $4.50 |
| Drivers | 74HC595 8-Bit Shift Register | Texas Instruments | 9 | $0.65 | $5.85 |
| Drivers | AO4606 N & P-Channel MOSFET Array | Alpha and Omega | 36 | $0.45 | $16.20 |
| Power | LM2596 DC-DC Buck Converter Module | Generic | 1 | $2.50 | $2.50 |
| PCB | 4-Layer Custom Driver Board | JLCPCB | 1 | $25.00 | $25.00 |

| | | | | | |
|---|---|---|---|---|---|
| Mechanical | 3D Printed Housing (PETG Filament) | In-House | 250g | $0.05/g | $12.50 |
| Hardware | M3 Bolt/Nut Assortment | Generic | 1 | $10.00 | $10.00 |
| Connectors | JST-XH Connectors / Ribbon Cables | Generic | 1 | $8.00 | $8.00 |
| Misc | Solder, Flux, Thermal Paste | Generic | 1 | $15.00 | $15.00 |
| Total | | | | | $229.15 |

# Appendix A: Technical Software Logic

To maintain the deterministic 40 kHz signal required for levitation, the following pseudocode outlines the core 80 kHz Interrupt Service Routine (ISR) running on Core 0. This logic is responsible for the "bit-banging" of phase data into the shift registers.

```
// Pseudocode for the High-Speed Acoustic Engine (Core 0)

void IRAM_ATTR onTimer80kHz() {

    static uint8_t phase_index = 0;



    // 1. Increment the phase cycle index (0-255 steps)

    phase_index++;



    // 2. Prepare the 72-bit stream for the 9 shift registers

    for (int reg = 0; reg < 9; reg++) {

        uint8_t byte_to_shift = 0;

        for (int bit = 0; bit < 8; bit++) {

            int transducer_id = (reg * 8) + bit;



            // Check if this transducer should be HIGH or LOW

            // based on its pre-calculated phase offset

            if (current_phase_offsets[transducer_id] > phase_index) {

                byte_to_shift |= (1 << bit);

            }

        }

        // 3. Push data to the 74HC595 via SPI/Bit-bang
```

```
      shiftOut(DATA_PIN, CLOCK_PIN, MSBFIRST, byte_to_shift);
    }

    // 4. Latch the data to the transducer outputs
    digitalWrite(LATCH_PIN, HIGH);
    digitalWrite(LATCH_PIN, LOW);
}
```

# Appendix B: High Voltage (HV) Calculations

Let's design for what we kept saying:

- HV output: **240 VDC (or 240 VAC rectified ~340 Vpk, but we'll design for 240 VDC equivalent)**
- Output cap: **C = 220 µF** (change to your real value)
- Safety target: **240 V → ≤ 60 V in ≤ 30 s** (IEC 61010 style)

Discharge equation:

$$V(t) = V_0 e^{-t/(RC)}$$

We want:

- $V_0 = 240\text{ V}$
- $V(t) = 60\text{ V}$
- $t = 30\text{ s}$

$$\frac{V(t)}{V_0} = \frac{60}{240} = 0.25 = e^{-30/(R \cdot 220\mu F)}$$

$$\ln(0.25) = -\frac{30}{R \cdot 220 \times 10^{-6}} \Rightarrow R \approx 4.0 \times 10^5\ \Omega = 400\text{ k}\Omega$$

So **R ≈ 390–430 kΩ** gets you right in the zone

# Appendix C: Index of Tables & Figures



# Appendix C: Index of Figures

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