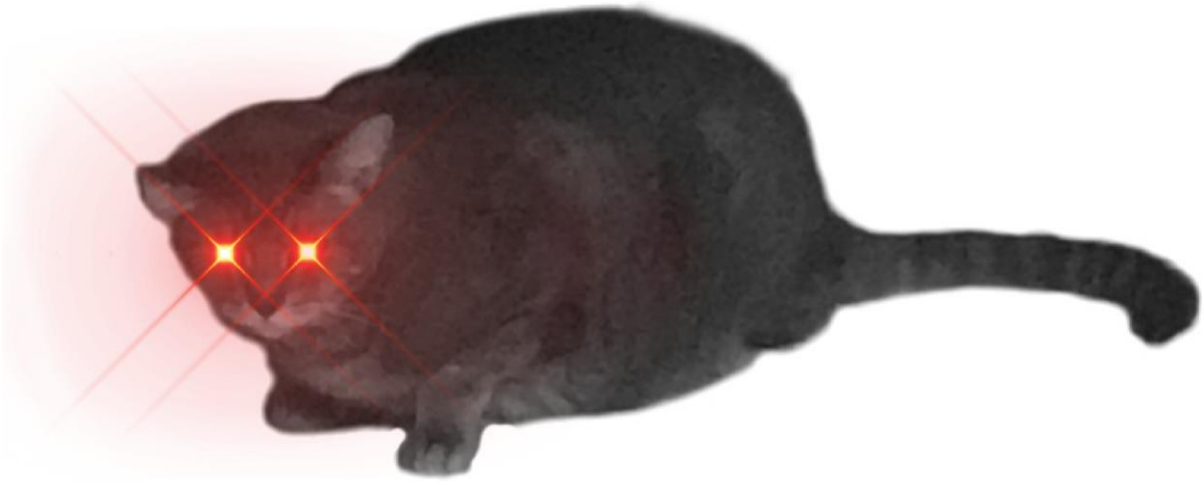
P.H.A.T.C.A.T.

PHASOR-HARMONIC ANALYSIS FOR TRANSFORMER CONDITION ASSESSMENT AND TELEMETRY



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1. Executive Summary

On all fronts—academic, political, and industrial, there is a great deal of change and growth occurring in the electrical power industry. This comes after a period of long stagnation which has resulted in a high need for educated, young power engineers. One key facet of power systems is their protection and control. Sparked by a desire to both learn and create a needed educational resource, PHATCAT was conceived to provide insight into the design and functionality of modern microprocessor relays, which are the heart of the power system's protection and control.

PHATCAT is primarily intended for protecting large, three-phase power transformers, such as those located in substations. It contains a suite of protective algorithms commonly used in power system protection, including time-inverse overcurrent, restrained current differential with harmonic blocking, and overexcitation protection (Volts/Hz). It uses transducers and digital signal processing to convert analog voltage and current signals into internal phasor representations of power system quantities. By manipulating these phasors, it accommodates different kinds of transformer connections and turns ratios. Additionally, PHATCAT provides all of the functionality necessary for interfacing with other substation equipment. It possesses DC sense inputs for reading binary statuses, such as circuit breaker positions. It also has switchable contacts for providing binary statuses to other devices or energizing circuits (e.g. a circuit breaker trip coil circuit). PHATCAT provides user-interactivity, displaying power system data on its front panel, indicating protective trips with LEDs, and receiving user-commands with pushbuttons. All of these functions are user-customizable with a desktop application – important setpoints for protective algorithms, transformer data, LED behavior, push button behavior, sense input behavior, and output contact behavior are all robustly customizable via a graphical user interface that supports user-defined Boolean expressions. These settings can then be easily downloaded to PHATCAT via USB.

This paper documents PHATCAT's design process, including key technologies and theory, design philosophy, relation to current industry practices, testing, and fabrication. The project's context is provided first, along with a detailed set of engineering requirement specifications for PHATCAT. Important technologies and protective algorithms are briefly discussed, and two state-of-the-art transformer protective relays are analyzed. A detailed discussion of PHATCAT's core components is then given and general hardware and software implementations are chosen. Real world design constraints, such as those imposed by sociopolitical factors and standards, are also analyzed. More detail is then provided regarding the detailed design of PHATCAT, including abbreviated circuit schematics and bills of material. The actual fabrication plan for PHATCAT is then provided, including printed circuit board (PCB) schematics. Next, the test plan for evaluating PHATCAT's performance is given. Administrative content, such as project milestones and the project budget are also documented before the project's final conclusions are presented. Appendixes are provided containing permissions for copyrighted material reproduced and references.

2. PROJECT DESCRIPTION

In the Project Description, the background of the project is first shared, along with the factors motivating its selection for Senior Design. The qualitative objectives are then provided—these statements define what the project should provide to the authors and readers, as well as what final prototype should be capable of on a high-level. Lastly, the required specifications are listed. These quantitative guidelines establish the required physical capabilities of those features of the final prototype necessary for it to achieve the project objectives.

2.1 PROJECT BACKGROUND AND MOTIVATION

The reliable availability of high-quality electric power is foundational in nearly every aspect of modern society. Furthermore, there is a great deal of academic and industrial development ongoing in the energy sector. UCF recently appointed a Director of Energy Initiatives, devoted exclusively to helping UCF become a leader in the field. Duke Energy, a utility serving ~ 2 million electric customers in Florida, is currently launching some of the most sweeping and expensive transmission upgrades in the company's history. All over the world, new applications are being pushed and tested to modernize the way power systems are engineered. A critical system within each aspect of power systems, from generation to distribution, is that which provides the system's protection and control.

Protection systems are responsible for detecting system disturbances (e.g., faults) and taking actions to mitigate their effects. Control systems are responsible for regulating power systems equipment for optimal system performance. Devices, referred to as 'relays,' are used to perform these functions. The first relays were electromechanical (Fig 2.1), but microprocessors, first applied in the late 1960's, have since risen to become the predominate technology (Fig 2.2). Modern microprocessor relays[1] receive analog voltages and currents from instrument transformers that correspond to voltages and currents in the power system by a known ratio. These signals pass through analog filters before being sampled digitally, from which phasor representations are derived. Most modern relay features work in the phasor domain (c.f. [2.1]). A wide variety of fault detection functions are in use today, each with varying requirements for proper application. This project seeks to design a microprocessor relay capable of performing the protection functions for a power transformer.

Power transformers facilitate the transfer of power between two points in a power system that are at different voltages (Fig. 2.3). This occurs often. High voltage (e.g., 230kV) is preferred for transmission of power due to its higher efficiency and lower voltage drop. Medium voltage (e.g., 13kV), on the other hand, is preferred for generation and distribution of power due to its lower insulation requirements.

Fig. 2.1. A traditional electromechanical relay. Reproduction permission requested from ABB.

Fig. 2.2 A modern microprocessor relay. Reproduced with the permission of GE Grid Solutions.

[1] [1] To those outside the power systems industry, this may sound almost like an oxymoron. However, this is commonly used terminology and stems from both their electromechanical heritage and their frequent use of switching as a response to disturbances.

Microprocessor relays are typically applied for larger (10MVA+) transformers such as those housed at substations and generation plants. Even the smaller, lower voltage transformers such as those at distribution stations, can cost several hundred-thousand dollars and weigh several hundred-thousand pounds. This makes them valuable assets that can take as long as a year to replace. As such, great care is taken to monitor their condition and ensure that, should a disturbance occur, they are de-energized before they can become damaged. However, it is not enough for this monitoring to merely detect disturbances. It must also be able to differentiate between different kinds of disturbances and behave appropriately.

Fig. 2.3. A distribution transformer in a substation. Photo by B. Ross.

Consider a distribution transformer that supplies multiple distribution lines. It is undesirable for a transformer's protection to trip immediately for a single faulted distribution line—this would take all distribution lines out of service. Instead, a different protection is designed specifically to detect faults on a particular feeder. It should trip first. However, this feeder protection may not always work perfectly. So, the transformer protection must serve as a backup, tripping when other protections are malfunctioning. In the industry, this process is referred to as 'coordination.' A protection system must not only be able to detect disturbances, but to differentiate between the different kinds of disturbances that necessitate different actions be taken.

This particular project is motivated by several drivers. Senior Design serves as the capstone achievement for the ABET engineering undergraduate. It is a demonstration of technical and interpersonal competency, as well as of dedication and self-motivation. In these ways, it serves to help validate that those who succeed in it are worthy of an engineering degree and the responsibility it confers. Through the completion of this project and the development of a working prototype, this validation is achieved. This specific project originated as a result of some authors' power systems backgrounds and their desire to further their knowledge in the field of protection and controls. A transformer was chosen as the various challenges associated with its protection serve as examples of the power of phasor-based protection but do not require communications for effective function. Support for protection communications was determined to be out of the scope for this project. As will be seen in Sections 2.2 and 2.3, the wide variety of functionalities required presents an interesting and complex project that requires knowledge in many different fields of electrical and computer engineering.

It is important to clarify that the purpose of this project is not innovation, it is education. It is only in recent years that energy has become a dynamic field; for many years, it was highly static when compared to industries such as communications and integrated circuit design. But the coal plants and radially-fed distribution systems that have powered America for over a century are no longer sufficient for today's sustainability and efficiency requirements. As a result, the energy industry is now facing a large body of complex work that must be undertaken at a time when many of their experts are retiring. Young engineers are very rapidly having to take on and execute multi-million-dollar projects. Furthermore, the ever-expanding role of communications in protection and controls has made cyber-security a cause of great focus

from regulating bodies. This had led to ever stricter and more complex compliance requirements being placed upon protection and controls engineers.

These factors culminate in what is a very challenging and dynamic time for protection and controls engineering, heightening the risk of human performance errors. The penalty for such errors can be quite severe. Service outages for thousands, millions of dollars in equipment damage, and even loss of human life can occur if protection and controls systems are not engineered to the highest level of robustness and resiliency. It is the authors' hope that this project's educational benefit will serve as a countermeasure, extending beyond their own personal growth to contribute to the industry, where other young engineers can gain deeper insight into how microprocessor relays function.

2.2 PROJECT OBJECTIVES

PHATCAT must carry out a series of protection functions that accurately detect certain system disturbances with the goal of protecting two-winding three-phase transformers. It must be able to differentiate between different kinds of disturbances that necessitate different action. These protection functions are to include instantaneous overcurrent, time-inverse overcurrent, current differential, overexcitation, and harmonic blocking. In order to carry out these functions, it should be able to perform all of the signal processing necessary. Incoming analog signals coming from three-phase potential transformers and current transformers must be converted into digital representations of phasors. The sequence components of these three-phase phasors must also be calculated before they can be used in the protection functions. The percentage values of certain harmonics also need to be calculated.

PHATCAT must be able to close and open output contacts. The term 'contacts' is used to make their function clear, but the actual mechanism may be electromechanical or solid-state. These contacts can be wired up so as to operate other equipment such as circuit breakers that will mitigate the disturbance's impact and/or remove the disturbance from the power system. It must also possess 'coils' that can sense active high/low inputs and use these in internal logic. This allows for sensing the closing of other contacts, such as those that represent breaker positions, or for certain auxiliary functions, such as the sensing of transformer alarms, to be performed by the relay.

PHATCAT must also support a modicum of flexibility; nearly every application of protective relays requires engineering specific to the situation at hand. Short circuit studies, custom logic equations, and wiring external to the relay are all used when protecting and controlling power systems equipment. In the current state-of-the-art, it is not possible to sell a transformer protection relay that requires no engineering work for its application. The relay must then allow for easy configuration of those characteristics that might need to be altered during its application. This is to be done through the use of a graphical-user interface (GUI) driven program running on a PC. This should allow for the creation of files that determine the relay's behavior as well as the retrieval of the relay's current configuration.

Field personnel must also be able to gain insight into the PHATCAT's measurements and perform basic configuration changes by interacting with it. A display showing the measured currents and voltages is to be used. The relay should have a setting for inputting used instrument transformer ratios and use this to present values in primary-side quantities. The relay should have a two-factor power switch that prevents accidental switching. It should also have LEDs and push-buttons or switches on the front panel. Some LED and push-button functions can be hard-coded, but some should also be available for use in custom logic equations. Fig. 2.4 depicts a concept of PHATCAT's physical construction. Fig. 2.5 and 2.6 relate hardware and software block diagrams of PHATCAT's functionalities.

In the documentation of all these features' implementation, reference will be made to specifications and features utilized in industry wherever possible. While it is not always feasible to meet these specifications given the time, capital, and labor resources available, the goal of this project is to inform the readers about microprocessor relays. As such, industry practices will be shared, even when their implementation lies outside the scope of the project.

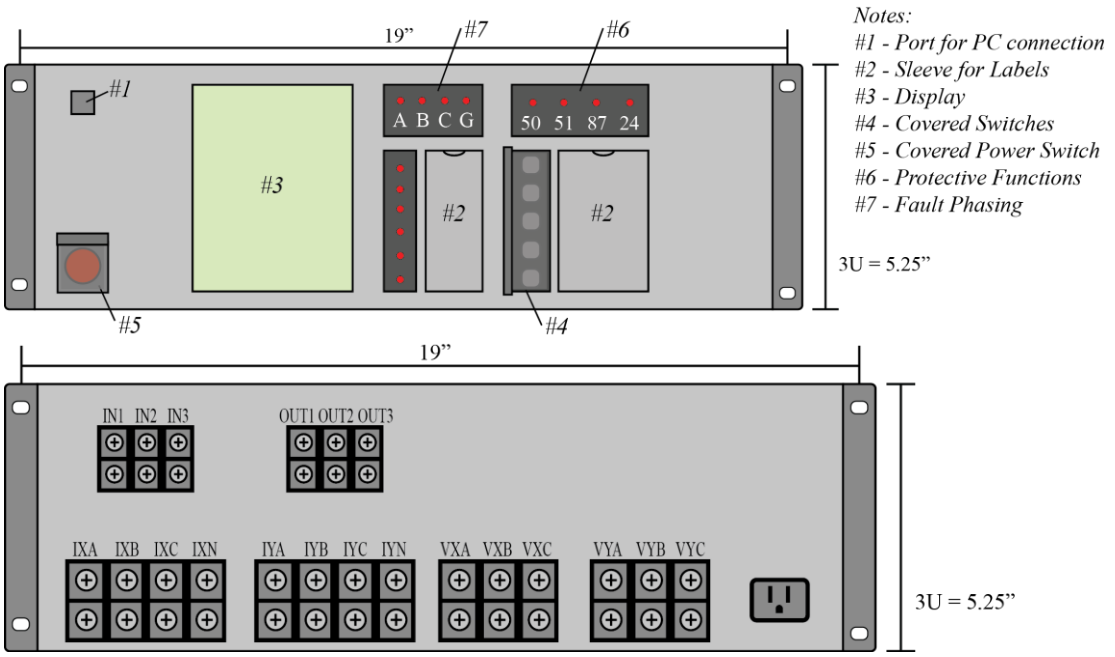

Fig. 2.4. Concept of microprocessor relay front (Top) and rear (bottom). By B. Ross

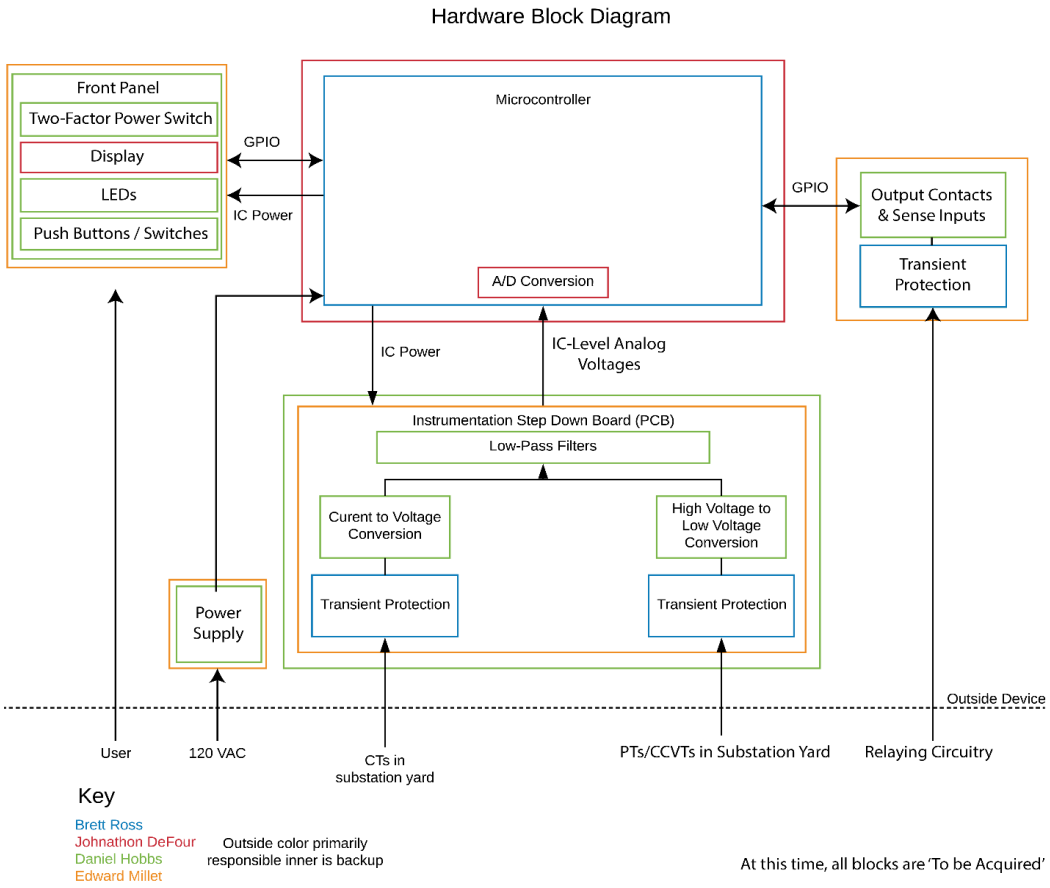

Fig. 2.5. Project hardware diagram. By document authors.

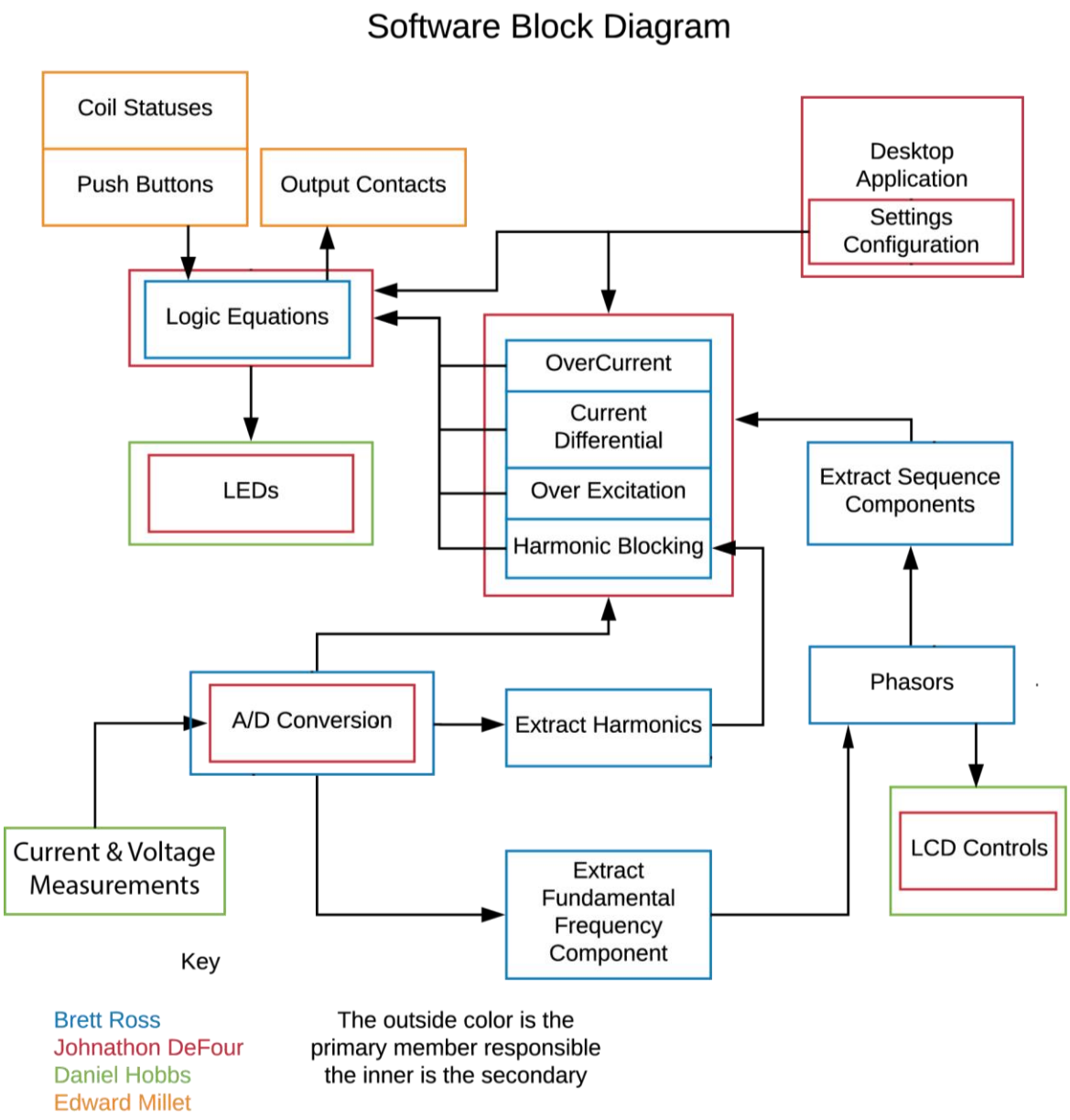

Fig. 2.6. Project software diagram. By document authors.

2.3 REQUIRED SPECIFICATIONS

In order to achieve the project objectives, the following specifications are required:

Inputs and Measurement

- 8 rear-panel inputs for analog current measurement.
  - They must have a continuous thermal rating of at least 5A RMS
  - They must accurately sense currents up to at least 30A RMS
  - They must have a one-second thermal rating of at least 30A RMS
  - They must have an effective series resistance (ESR) of less than 100 mOhm.
- 6 rear-panel inputs for analog voltage measurements.
  - They must have a continuous rating of at least 67 volts RMS
  - They must have an ESR of at least 1 kOhm.
- For the above analog inputs, the following is required:
  - An analog low-pass filter with a -3dB frequency of at least 2 kHz $\pm$ 10% shall be implemented
  - Digital representation of the percentage of the signal's content belonging to the second, fourth, and fifth harmonics, accurate to within $\pm$10%
  - Analog-to-digital conversion with a sampling rate of at least 650 Hz[2]
  - Tracking of the digitized signal's fundamental frequency within a range of 45 and 65 Hz
  - Digital representation of a phasor representing the RMS amplitude and phase angle of the fundamental frequency component of the signal. The reference used for the phase angle should be common to all analog inputs. Magnitude and phase should be accurate to within $\pm$5% and phase should be accurate to within 1°
- At least 3 rear-panel control inputs for detecting a 125VDC nominal active high signal. They should
  - Withstand a 125VDC potential difference
  - Draw less than 10mA at nominal voltage
- At least 3 sets of individually-controllable rear-panel output contacts. These can be electromechanical or solid state, so long as they:
  - Isolate a 125VDC potential difference when open
  - Can carry at least 2A nominal when closed
  - Have a voltage drop of no more than 1V at their nominal current
  - Can break 2A of current when called upon to open

Protection Functions

- Must have phase, neutral, and residual instantaneous overcurrent elements with configurable pickup and definite time delay.
  - The element trip time should be within $\pm$10% of the set trip time, with any additional delay to be less than 2 power system cycles
  - The actual element trip value should be within $\pm$10% of the set value
- Must have phase, neutral, and residual inverse-time overcurrent elements with configurable pickup, time-dial, and curve settings.
  - The element trip time should be within $\pm$10% of the set trip time, with any additional delay to be less than 2 power system cycles
  - The actual element trip value should be within $\pm$10% of the set value
- Must have an instantaneous differential element with a configurable pickup value.
  - The element must take no more than two power system cycles to operate
  - The element's actual tripping threshold should not deviate from its set threshold by more than $\pm$ 10%

[2] Nyquist Frequency of the highest needed frequency component

- Must have a restrained differential element with configurable pickup, slope one, slope two, and slope intersect settings.
    - The element must take no more than two power system cycles to operate
    - The element's actual tripping characteristic should not deviate from set characteristic by more than ±10%
- Must have an overexcitation element with configurable pickup and time delay
    - The element trip time should be within ±10% of the set trip time, with any additional delay to be less than 2 power system cycles
    - The actual element trip value should be within ±10% of the set value

External & User Facing Features

- At least fourteen front-panel LEDs
    - Four for indicating the phasing of a detected fault
    - One for indicating the device is powered on
    - Five indicators for protection functions (instantaneous overcurrent, time-inverse overcurrent, current differential, overexcitation, and harmonic blocking)
    - Four other user-programmable LEDs
- At least six user-programmable front-panel pushbuttons or switches
- One front-panel power button
- A front-panel display for showing measured current and voltage phasors
- A power supply capable of supporting all project systems from a 120VAC source
- An enclosure for the relay electronics suitable for mounting in a 19" equipment rack, such as those used for servers, with screw terminals for making external connections to sense inputs, output contacts, voltage sensors, and current sensors
- An application running on a PC that allows for end-users to configure protection functions and build custom control logic.
    - The application must facilitate delivering the user-defined configuration to the microcontroller
    - The application must facilitate retrieving the device's current configuration

Realistic Design Constraints

- The completion times of the documentation and prototyping associated with these specifications must abide by the milestones set forth in this document. (time constraints)
- Any assets to be paid for by a sponsor must have their purchase documented. Authors must provide technical grounds for exceeding the initial budget. (economic constraints)
- No components used in the final prototype may be noted by suppliers/manufacturers as obsolete or 'not for new design' at the time of their procurement (sustainability constraints)
- The front-Panel push buttons and power button must require two-factor operation (safety constraints).
- The device must not support any form of wireless communications or LAN connectivity. (sociopolitical constraints)

Standards Constraints

- All communications requiring a protocol should use an established standard in the manner intended by the protocol standards.
- All voltage sense, current sense, output contacts, and control inputs should have the following protections[3]:

[3] These are simplifications of ESD, EMI, Fast-burst Transient Immunity, etc. requirements to something demonstrable.

- Galvanic isolation in some form (e.g. optocouplers, transformers) between the outermost component and the rest of the relay.
- Overvoltage protection capable of protecting the input/output from a 50% overvoltage for at least 15 ms.
- No protection on current sense circuits is to create an open circuit, either intentionally or by failure

3. RESEARCH

In this section, several key technologies and relevant concepts are related to provide context for key aspects of PHATCAT's functionality. A brief market analysis of transformer protection offerings is then conducted. Core implementations for PHATCAT's functionality are then explored.

3.1 RELEVANT TECHNOLOGIES

Due to the project's specialized application, relevant technologies are presented before the market offerings, providing context.

3.1.1 POWER SYSTEM TRANSFORMERS

At a basic level, a transformer is a fairly simple device. Two coils of conductor are wound around a material with a high magnetic permeability (e.g. an iron core) such as to create a strong coupling of the magnetic fluxes through each of the coils (i.e. a high mutual inductance) (Fig. 3.1). As a result, a time changing voltage applied at the terminals of one winding generates a magnetic flux that in turn induces a voltage on the other winding. Faraday's law of induction relates the electromotive force (V) to the magnetic flux through a coil of *N* turns:

$$EMF = N\frac{d\Phi_B}{dt} \tag{3.1}$$

Because the voltage is proportional to the number of turns, a transformer with a perfect magnetic coupling relates the voltages in each coil by the ratio of the number of turns.

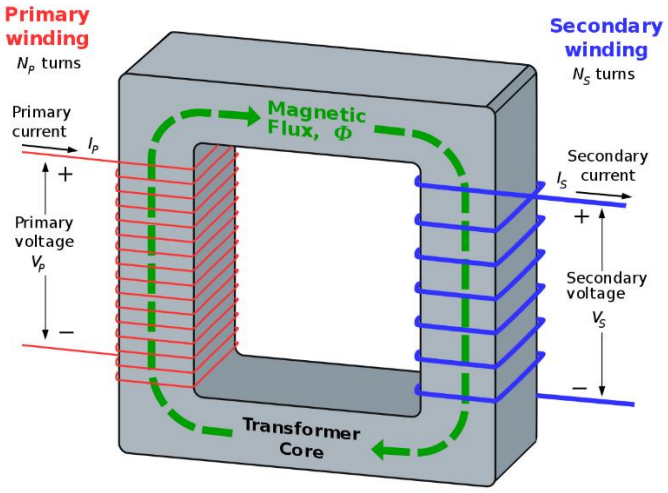

Fig. 3.1. A transformer's magnetic and electrical circuits. Credits to Bill C at the English language Wikipedia [CC BY-SA 3.0 (http://creativecommons.org/licenses/by-sa/3.0/)]

The currents flowing in the primary and secondary windings are inversely related to the voltages. Thus, if the transformer is lossless, power is conserved.

$$\frac{V_p}{V_s} = \frac{N_p}{N_s} \quad ; \quad \frac{I_s}{I_p} = \frac{N_p}{N_s} \quad ; \quad V_p I_p = V_s I_s \tag{3.2, 3.3, 3.4}$$

This relationship allows for transformers to facilitate the transfer of power between voltage levels. However, real transformers do not have this exact IV characteristic. An accurate steady-state model of a nonideal transformer is given in fig. 3.2

The series impedances model the resistance and self-inductance of the windings. The shunt impedance models two non-idealities within the transformer core: eddy currents and hysteresis loss. Eddy currents are unwanted currents induced in the transformer's core by the electromagnetic field. These cause losses and

core heating and are often mitigated through the use of nonconductive layers of ‘laminate’ that break up current loops and reduce the ability of eddy currents to flow. Hysteresis loss results from the energy required to align the mag

netic domains within the core material with the time-changing voltage. In reality, it is not a constant impedance value, but is dependent on past core states. For steady-state conditions, the shunt impedance of the transformer is very large, and the approximation is still very good.

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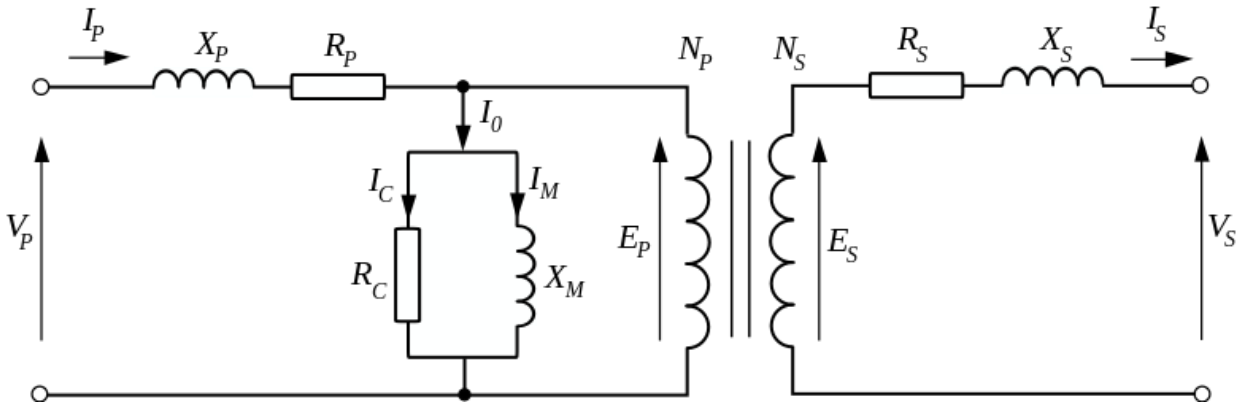


Fig. 3.2. A non-ideal transformer model. Credit to Cblambert [CC BY-SA 3.0 (https://creativecommons.org/licenses/by-sa/3.0)]

For proper transformer protection, it is important to understand that the current flowing through the core losses, called the ‘excitation current,’ can sometimes be large. During transient conditions, especially during initial energization, large amounts of excitation current flow to magnetize the transformer core to its new steady state. This transient, referred to as ‘inrush current,’ contains large amounts of harmonic content, and the need to avoid an unintentional trip during transformer energization is the primary motivation for this project’s incorporation of harmonic blocking. Another cause of large excitation current is ‘core saturation.’, Every iron core has a certain amount of flux it can produce. One this threshold is exceeded, the core begins to saturate and is unable to reproduce an accurate secondary current. This is modeled by a drastic reduction in the shunt impedance. This can cause damage to the transformer through excessive core heating. It can also cause the misoperation of certain protections. It can be shown that the degree of core excitation is proportional to the voltage divided by the system frequency. As such, ‘Volts/Hz’ or ‘overexcitation’ elements are used to protect against these conditions.

In three-phase systems, there are multiple ways to connect three sets of transformer windings. The first is ‘wye’ or ‘star’ connection (Fig 3.3). Three coils receive phase connections on one end and are joined in the center on the other. The center point may be grounded and/or connected to a neutral wire on which the system imbalance (i.e., the zero-sequence com) can flow. Another is the ‘delta’ connection (Fig 3.4). Three coils are connected end-to-end, forming a triangle. Phase conductors are connected at the vertices of the triangle. No neutral is used. A variety of transformer connections (e.g. Wye-wye, wye-delta, etc.) are formed that utilize these two connections in different combinations.

Depending on the combination of connections used, different transforms of phasor magnitude and phase angle will have to be applied to the read phasors in order to meaningfully compare high and low side currents. This gives rise to the need for the project to perform connection compensation within the relay. Additionally, many power system transformers contain devices called ‘load-tap changers’ (LTCs) that vary the transformer’s turns ratio by a small amount to improve voltage regulation. Protections that operate based on voltage or normalize values between the high and low sides of the transformer should be set to account for possible variation (~$\pm$5%) in the turns ratio.

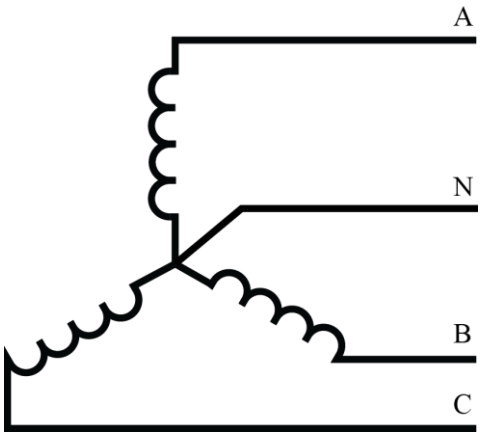


Fig. 3.3. Wye connection for three coils. By B. Ross

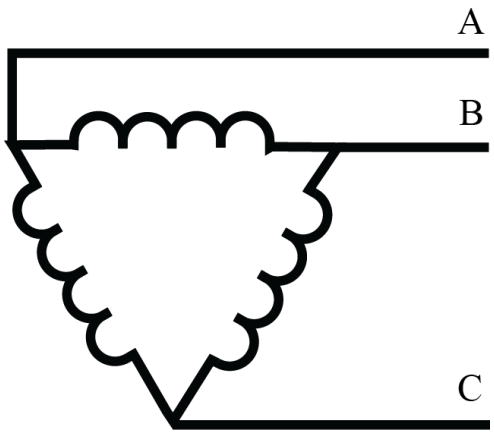


Fig. 3.4 Delta connection for three coils. By B. Ross

3.1.2 INSTRUMENT TRANSFORMERS

Devices that monitor electrical quantities in power systems face a challenge, namely, the magnitude of the quantities to be measured. 'Instrument Transformers' are often used to linearly step-down current and voltage magnitudes to those more suitable for distribution within an enclosure. Microprocessor devices (e.g., PHATCAT) often require additional internal hardware to further reduce the levels to board-level quantities (e.g. 30A to 10V). The physics of transformers are discussed throughout this paper, so this section will focus primarily on explaining how they are applied to relate primary power system quantities (e.g. 3000A, 230kV on a 300 MVA power transformer) to those available to devices such as PHATCAT.

Application of Current Transformers: Current transformers are usually applied as toroids (Fig. 3.5) that slip-over the primary conductor. They are often located within the bushings of circuit breakers (Fig. 3.6) and transformers. Their maximum provided turns ratio is often chosen to carry 5A at the rated ampacity of the rated current. For example, a 3000A nominal circuit breaker would have 3000:5 CTs. These CTs typically come with multiple taps that allow for a selection to be made from several different ratios. Multiple sets of CTs are usually provided within one piece of equipment, for use with different devices where sharing a common connection might constitute a reliability risk. A thermal rating factor (TRF) is given, which gives the nominal

Fig. 3.5. A pallet of taped toroidal CTs. Reproduction permission requested from Stemar.

Fig. 3.6. 230kV gas-insulated breaker with bushing mounted CTs. Photo by B. Ross.

thermal rating of the CT as a factor of its secondary ampacity. For instance, a 3000:5 CT with a TRF of 2.0 can carry 10A nominal on its secondary. A TRF greater than 1 is frequently necessary when tapping a CT below its maximum ratio, as the nominal primary side current will then induce a secondary current greater than 5A.

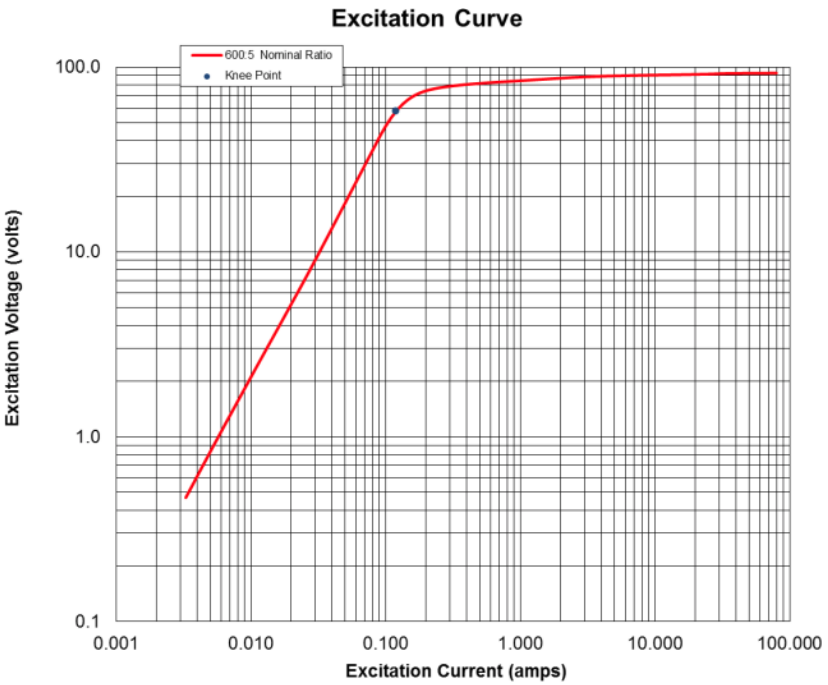


Fig. 3.7. A typical CT excitation curve. Reproduced with the permission of Voltage Disturbance.

The chief measure of protective CT performance is the location of the CTs 'knee point,' or, where the CT saturates. This can be visualized by looking at a CT's excitation curve (fig 3.7). The excitation voltage, or the voltage at the CT secondary terminals, is given to be a good indicator of how intense the magnetic flux inside the CTs core is (see Section 3.1.7 – Overexcitation Protection for a derivation). The excitation current, which is the shunt current required to sustain the magnetic circuit, is related to the voltage using this curve. On fig 3.7, the knee point occurs somewhere just after 0.1A. Up until this point, the ratio between excitation voltage and current is linear. In other words, the excitation impedance is constant. At and beyond the knee point, this relation becomes nonlinear and the impedance (the slope of the curve) overall becomes much lower. So, past the knee point, large harmonic content can be expected. Additionally, the excitation impedance will be greatly reduced. The excitation branch forms a parallel path with the relay sensing the CT current, so a reduction in excitation impedance will result in a portion of the current not being measured by the relay. Thus, it is very important that protection CTs do not enter saturation during a large fault current. This is the driver for PHATCAT's requirement that the current sensing circuit have an extremely low input impedance. The higher the burden, the higher the excitation voltage created for a given current, and the higher the excitation voltage, the more likely it is that the CT will saturate.

For CTs used for protective relaying, IEEE C57.13 provides guidelines for classification of CT accuracy. Given in the form *CX00*, where X is commonly 2, 4, 8, or 12. A C400 CT is accurate for an excitation voltage of 400V where the CT burden is 4 Ohms. The chief physical difference between a C400 and C1200 CT is the size of the iron core. By providing the maximum excitation voltage, this rating provides a measure of the performance of the CT's core that is much easier to work with than one given in Webers. By summing all of the impedances constituting the CT's burden (cable, relay coil, CT winding impedance), the excitation voltage for a given fault current is easily obtainable.

Application of Potential/Voltage Transformers: Potential or Voltage Transformers (PT or VT - the terms are used interchangeably) are usually installed as standalone devices and placed at the ends of runs of bus work or at line terminals. Much like loads, they are connected in shunt. They are designed to draw very little current, though some degree of oil or air cooling is still used. Because they are not subjected to extreme fields during faults the same way CTs are, their application is much simpler. For a given voltage level, the PT ratios are chosen to give secondary-side voltages for relaying, 67V and 115V options are common. Many times, PTs will have two secondary windings and taps for both 67V and 115V will be available on

each. Because we want to minimize heating in the PTs and any voltage drop in the control cables, which can be several thousand feet long, and are not sized to the thicker gauges that CT cables are, very little current should be drawn by PHATCATs voltage inputs

One modification of the PT worth mentioning is the capacitively-coupled voltage transformer (Fig. 3.8). The traditional PT (the three-winding transformer in the figure) is supplemented by a capacitive voltage divider. A compensation inductor, *L*, is added to compensate for the equivalent capacitance of the capacitive divider. At transmission voltage levels, CCVTs become cheaper due to the lower transformer turns ratio required. As such, they are commonly used. However, their frequency response makes them susceptible to damage from high frequency signals. The transients potentially induced by CCVTs is one motivator for the overvoltage protection in PHATCAT.

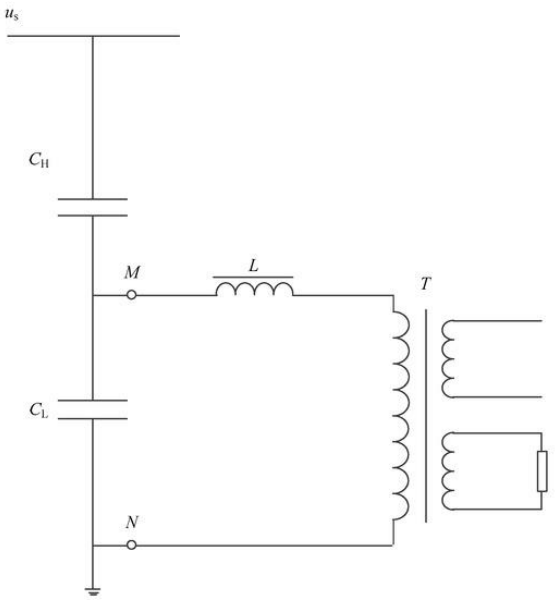


Fig. 3.8. Schematic of a Capacitor-Coupled Voltage Transformer. Reproduction permission requested from Bin Chen and Lin Du.

3.1.3 PROTECTIVE RELAYING CIRCUITRY

In order to understand some of the design philosophy underlying PHATCAT's functionality, some explanation is due regarding how protective relays are applied in a substation environment. While digital communications are playing an ever-increasing role in protection and controls, much information is still exchanged by opening and closing contacts. These are used to energize or de-energize inputs. Such inputs may be actual loads or coils for actuating electromechanical devices. Alternatively, they may be sense inputs, such as those used in PHATCAT, that simply translate the energized state into a logical '1' in the microprocessor logic levels. Fig. 3.9 gives an example of one of the most elementary applications of protective relaying circuitry. A contact in a protective relay (e.g., PHATCAT) is connected to the trip coil of a circuit breaker in the substation yard. A DC voltage source is provided, and the contact's position determines whether or not this voltage source energizes the circuit breaker trip coil. In this way, protective relays can have internal logic functions programmed to assert their various output contacts, opening the correct devices and sending informative signals to other relays. Similarly, the protective relays can have internal logic functions programmed to treat their sense inputs as a certain piece of information. One simple and common application of this is the detection of circuit breaker position (Fig 3.10, a '52/a' contact is an auxiliary contact in a power system circuit breaker that mirrors the breaker's position). Because the energized/de-energized state of the sense input follows the 52/a contact position, it effectively acts as a binary logic variable representing circuit breaker position. In fact, such relaying circuits can be thought of in terms of the logical expressions they implement. There are three basic tools: paralleling contacts to 'OR' them, cascading contacts serially to 'AND' them, and using normally-closed (as opposed to normally open) contacts to 'NOT' them (Fig. 3.11).

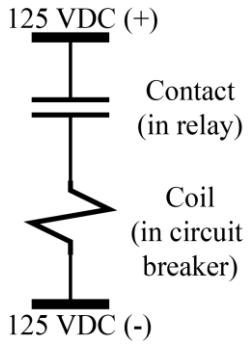


Fig. 3.9. Controlling a circuit breaker with a relay contact. By B. Ross

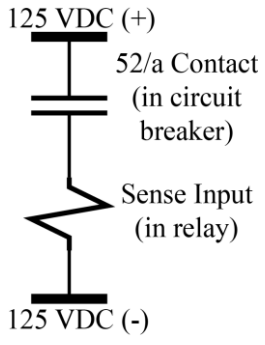


Fig. 3.10. Reading circuit breaker position with sense input. By B. Ross

These basic elements are combined into much more complicated control logics that provide the interactivity desired by the protection and controls engineer. This is why it is key that PHATCAT support user-defined logic – depending on the other devices at the substation and design preferences of the engineer, the role of PHATCATs sense inputs and output contacts will have to be customized.

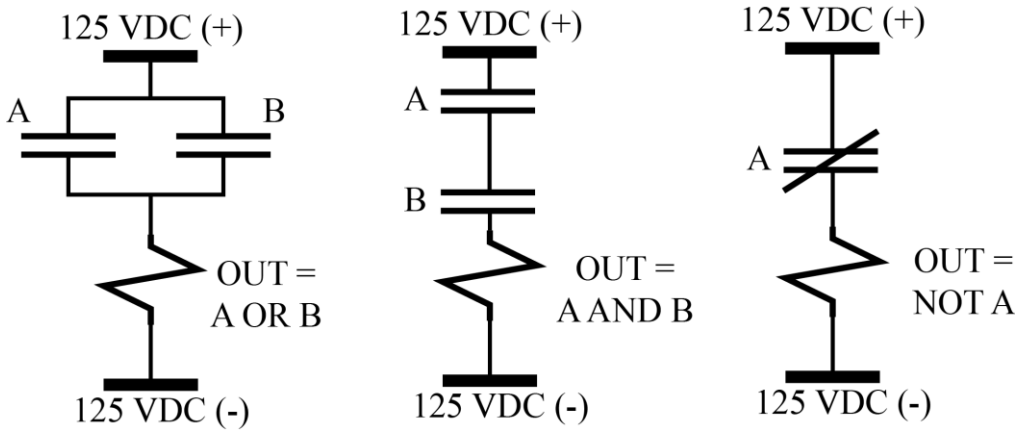


Fig. 3.11. Basic logic gates with relaying circuitry. By B. Ross

3.1.4 OVERCURRENT PROTECTION

Perhaps the simplest form of protection, overcurrent elements operate based on measured current. Instantaneous overcurrent elements (ANSI code: 50) simply compare the measured current to some preset threshold. A 'definite time' delay, measured in power system cycles, can be added to avoid accidental tripping for quick transients. Instantaneous overcurrent elements are usually set to high thresholds and are used to detect 'close-in' faults. That is, faults that are electrically very close to the measured point. In such situations, it is nearly always desirable that the protection operate as quickly as possible. However, there are many other fault scenarios where a single, instantaneous threshold is unacceptable. In order to preserve its ability to serve its loads, a power system should not remove more components than absolutely necessary to remove the disturbance. Time-inverse overcurrent elements (ANSI code: 51) operate with a time delay that is inversely proportional to the current. This allows for fast tripping for close-in faults but leaves some time delay to allow for protections closer to the fault to clear it. A 51 element's operating time is characterized by the following expression:

$$t_{op} = TD\left(a + \frac{b}{M^c - 1}\right)$$

The operating time, t_{op}, is inversely proportional to the ratio, *M*, of measured current to some chosen pickup current, which is the minimum current for which the element will operate. The time dial (*TD)* linearly scales the operating time. Coefficients *a, b,* and *c* are determined by the curve type chosen, and primarily affect the steepness of the curve. These coefficients are standardized and can be found in the operating manual of any relay with overcurrent elements. Consider a system where a transformer, protected by the PHATCAT's 51 elements, is to be coordinated with three distribution feeders (Fig 3.12).

The transformer overcurrent will still operate quickly for faults on the bus or distribution lines, but not as quickly as the distribution line protections (Fig. 3.13). Thus, it provides a backup without compromising coordination. 50 and 51 elements can operate on phase, residual, or neutral currents, and are suffixed by 'P', 'G', or 'N' respectively to denote the operating current. The residual current is the calculated sum of the phase currents and can be used in place of the neutral current if a neutral CT is unavailable. Residual and neutral elements are frequently set to be much more sensitive than phase elements, as the power system is mostly balanced during normal operations and sizable ground currents only flow during ground faults.

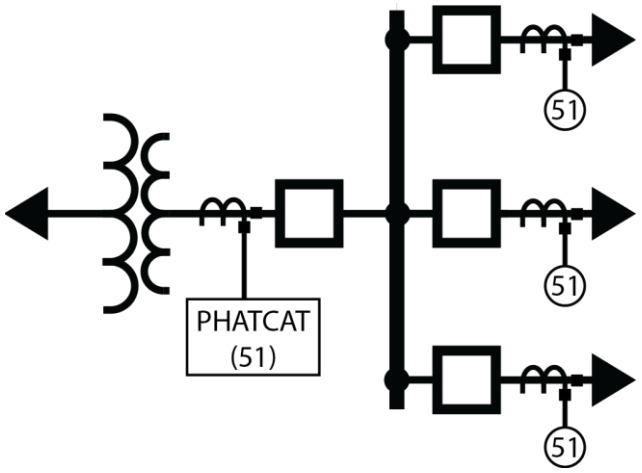


Fig. 3.12. PHATCAT as 51 on Distribution Transformer. By B. Ross.

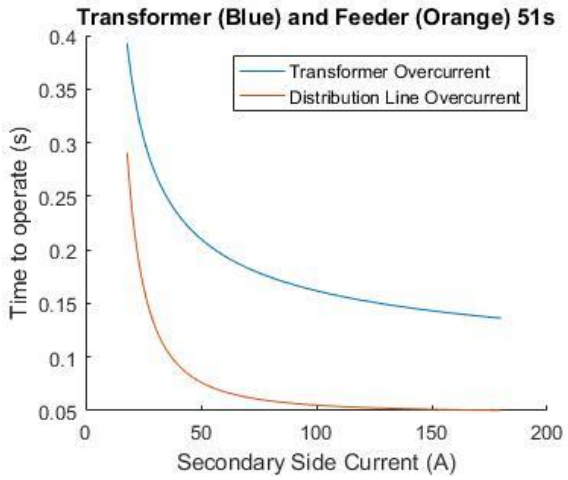


Fig. 3.13. Coordinated Overcurrent Settings. Figure produced with Matlab by B. Ross

3.1.5 Current Differential Protection

Current differential elements (ANSI Code 87) utilize Kirchhoff's Current Law to detect unwanted current paths. Current measurements are taken at every branch connected to a protected 'zone.' If the currents do not sum to zero, there is assumed to be some unwanted current path, i.e., a short circuit. This protection is extremely effective as it not only differentiates between proper operation and short circuit conditions, but it also works within a very clearly defined boundary. For faults external to the zone, the fault current will flow through the zone, but the currents will still sum to zero. For PHATCAT, this intended to be the primary protection.

The key to proper application of 87 elements is not the detection of the current difference during an internal fault, this difference is drastically larger than the steady-state value, which should theoretically be zero. Rather, it is mitigating factors that might create a 'false-differential'. For instance, an 87 algorithm must normalize currents measured at different voltage levels and remove any phase shifts introduced by transformer connections such as wye-delta. In order to avoid a false-positive for real-time error sources such as LTC changes, CT error, and noise, a 'restrained' differential is used (Fig. 3.14). In addition to the phasor sum of the currents (I_{OP}), a restraining quantity (I_R) is calculated. Its purpose is to estimate the magnitude of overall current flow and, based on the assumption that this is proportional to the error, increase the I_{OP} required to operate the 87 element. A minimum threshold (O87P) is set along with two slope values (SLP1, SLP2) and a slope intersection point (IRS1). An unrestrained pickup value (U87) can also be set.

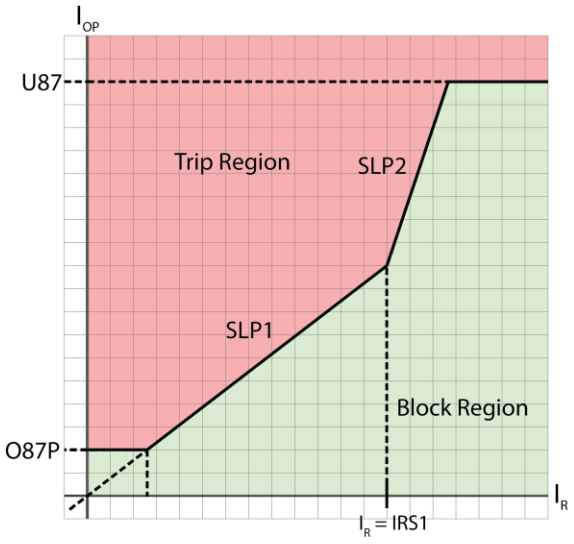


Fig. 3.14. Restrained Differential Element. By B. Ross.

Some transformers, such as delta-wye connected, only allow ground fault currents to flow on one side of the transformer. In the delta-connected winding, there is no path to neutral/ground, and any ground currents flowing in the wye-connected winding will remain trapped within the delta winding—they will not be measured by the CTs, which measure the phase current. In order to prevent a false differential for external ground faults,

the PHATCAT must remove the zero-sequence current component before performing its restrained differential calculations.

3.1.6 HARMONIC BLOCKING

Harmonic blocking is not used to trip protections, but rather to prevent protections from tripping for false positives. When a transformer is first energized, a large amount of current flows in the excitation branch. At this point, the transformer has not yet started to serve its load, so the through-current in the transformer is nearly zero. So, how is the differential protection to distinguish between an internal transformer fault and transformer energization? Because the excitation impedance of the transformer core is both nonlinear and time-varying during energization, large harmonics are produced. These harmonics are far in excess of what might be produced by a fault. Harmonic blocking simply compares the magnitudes of the second, fourth, and fifth harmonics to the magnitude of the fundamental frequency component. If any of these ratios exceed set percentage thresholds, the differential protection logic is blocked. The third harmonic is not used as there are many other sources of third harmonics in power systems that might cause undesirable blocking. Harmonic blocking also helps prevent false differential operation for other sources of harmonics such as power transformer saturation (overexcitation), CT saturation, and energization of other nearby transformers (e.g., another transformer bank connected in parallel).

3.1.7 OVEREXCITATION PROTECTION

As we've discussed, the excitation branch of a transformer models those losses incurred in the core of the transformer. If these losses are high enough, the core becomes damaged, degrading the transformer's impedance or even destroying it. When the flux within an iron core becomes too intense, it can saturate. During saturation, there are no more magnetic domains within the material that can be aligned to produce more flux. The effect is that of drastically decreasing the excitation branch's impedance, greatly increasing losses. By rearranging Faraday's law of induction, we can establish that this flux is proportional to the system voltage and inversely proportional to the system frequency:

$$EMF = Vsin(\omega t + \phi) = N\frac{d\Phi_B}{dt} \;\Rightarrow\; \Phi_B(t) + \Phi_0 = \frac{1}{N}\int Vsin(\omega t + \phi)dt = \frac{-V}{\omega N}\cos(\omega t + \phi)$$

By setting a threshold of V/ω to trip for, we effectively set a threshold of magnetic flux. This should be set to a value below the maximum magnetic flux that the core can withstand. PHATCAT will just implement an instantaneous threshold trip, as this proves proper implementation of the protection, but many manufacturers utilize time-inverse characteristics so as to avoid tripping for transient system states that will not persist long enough to harm the core.

If the transformer utilizes an LTC to regulate the voltage, the overexcitation element should be set to operate based on the side of the transformer without the LTC.

3.2 MARKET OFFERINGS

There are many companies that sell microprocessor relays, including GE, ABB, Schweitzer Engineering Laboratories (SEL), Siemens, Beckwith, and Schneider Electric, among others. Two top-of-the-line transformer protection relays, by one made by SEL and another by Siemens, are examined in detail. While these devices give a good representation of the breadth and depth of functionality available today from all these manufacturers, not all applications require such complex devices. For instance, the older and simpler SEL-587 is still used in new constructions at some utilities. Core protective functions, such as time-inverse overcurrent and restrained current differential, vary little in their behavior between products and vendors, though there are certainly quirks and variances to be observed. The main difference between older and newer microprocessor relays lies mainly in the number of inputs/outputs supported, the number of different functions performed by one device, and the variety and modernity of the communications systems offered.

The primary end-users of these devices are protection engineers at consulting firms, utilities, and businesses with large or specialized power needs. As such, they are marketed in a very technical manner, with an emphasis on features, standards, and numerical values. Vendors also heavily utilize industry conferences as an avenue for marketing. They often publish whitepapers on the proper application of protection functions. When they work with a utility to use their relays in a challenging or unusual application, they often like to publish a paper sharing it. Relay manufacturers also offer a variety of seminars and trainings on power systems topics. All these strategies benefit the industry by sharing knowledge while also helping relay manufacturers share their products, establish rapport with customers, and build their reputation as knowledgeable experts.

Notable features of the two analyzed market offerings will be presented, then a table will be given that compares their quantitative specifications with one another and with PHATCAT.

3.2.1 SCHWEITZER ENGINEERING LABORATORIES: SEL-487E

The SEL-487E (Fig. 3.15) is SEL's newest and most powerful transformer protection relay [3.1]. It supports up to five sets of three-phase winding currents, making it suitable for transformers with more than two sets of windings. It provides all of the protection functions typically used in transformer protection, including current-differential, overcurrent, overexcitation, restricted earth fault, and harmonic blocking. For each function, it supports multiple elements of the same function with different settings. These elements also have 'torque equations'— user-definable logical expressions that control whether or not the element is enabled. SEL touts the relay's ability to be used with a variety of kinds of transformers and in a variety of substation topologies. This is a vital marketing point as every customer has different needs and tested practices; they want to be engineering their equipment to fit their application, not the other way around. SEL also mentions the relay's ability to track breaker operations and through-faults over time. Such data is valuable for equipment owners, power system circuit breakers and transformers are expensive pieces of equipment and must have a long service life to produce value justifying their cost. Circuit breaker operations and external faults put stresses on these components that can increase their maintenance needs and shorten their lifespans. The SEL-487E provides information that asset management entities can use to improve preventative maintenance and repair. Another aspect of the 487E that SEL emphasizes is its flexibility with a wide variety of communications architectures. Some of these are for Supervisory Control and Data Acquisition (SCADA) and others are for relay-to-relay communications. While many utilities have yet to fully utilize all of the benefits modern communications systems can bring, relay manufacturers have been pushing the boundaries forward.

The SEL-487E starts at $6750 but configuring it to include the fullest of its functionality brings the cost up to a $10,435. This is mainly driven by the inclusion of additional networking functionality and a larger number of higher-performance I/O.

Fig 3.15. SEL487 relay. Reproduction permission obtained from SEL, inc.

3.2.2 SIEMENS: SIPROTEC 7UT87

The 7UT87 is a part of Siemens' SIPROTEC 5 generation of relays (Fig. 3.16). It is the generation's most powerful and robust transformer protection relay. This generation stresses the relays' modular nature [3.2]. All of the relays use the same form factor for their base and allow for horizontal expansion via additional modules. With this modularity, it supports up to 9 sets of three-phase current measuring points. It possesses all of the standard transformer protections, including current differential, restricted earth fault, overcurrent, etc. One interesting protection is that of an impedance protection designed for transformers (21T). Siemens stresses the flexibility of the DIGSI 5 software used to configure the devices. A tremendous variety of functions are included in the relays and the software is used to combine those desired by the user into a custom arrangement of features. Customers then buy a certain number of 'function points', which then determine how many concurrent features they can run. This serves customer needs on a more specific basis by allowing absolute customization, even on a software level. Another feature Siemens highlights is the relays' conformance to cyber security requirements. Such assurances are critical as protection and controls engineers are under close scrutiny as they tackle the potential vulnerabilities introduced by modern communications systems.

Cost data for the 7UT87 was not available online but can be expected to vary significantly depending on the desired function points and expansion modules.

Fig 3.16. SIPROTEC series relays. Reproduction permission obtained from Siemens AG.

3.2.3 PHATCAT VERSUS MARKET OFFERINGS

With two market offerings related, some highlights can be compared so as to illustrate the ways in which PHATCATs performance has been curtailed from the industry standard so as to comply with the project's realistic design constraints. Note that this list is not exhaustive, there are many useful features included in these devices that it is simply out this project's scope to discuss. Additionally, these represent the maximum capabilities offered for each device. For market offerings, there are several configurations available for customers to strike the right balance between cost, functionality, and form factor.

Table 3.1. Comparison of PHATCAT and market offerings

Product:	SEL-487E	SIPROTEC 7UT87	PHATCAT (specified)
Measuring Points:	18 Currents, 6 Voltages	32 Currents, 15 Voltages	8 Currents, 6 Voltages
Measurement Ranges:	91A, 300V	500A, 200V	30A, 200V
Current Measurement Accuracy[4]:	Magnitude: ±0.2% ± 4 mA Phase: ±0.2°	Not given	Magnitude: ±5% Phase: ±1°
Voltage Measurement Accuracy:	Magnitude: ±0.1% Phase: ±0.5°	Not given	Magnitude: ±5% Phase: ±1°
Current Differential:	Restrained, Unrestrained, Negative Sequence	Restrained, Unrestrained	Restrained, Unrestrained
Harmonic Blocking:	2^{nd}, 4^{th}, 5^{th}	2^{nd}, 3^{rd}, 5^{th}	2^{nd}, 4^{th}, 5^{th}
Overcurrent:	Instantaneous, Time-inverse, Adaptive, Directional	Instantaneous, Time-inverse, Voltage-Dependent, Directional, Negative Sequence	Instantaneous, Time-inverse
Volts/Hz:	Instantaneous, Time-inverse	Instantaneous, Time-inverse	Instantaneous
Protection Accuracy[5]:	±1% to ±5% ± 0.10A	2%	±10%
Protection Delay[5]:	0.5 cycle to 1.75 cycle (8.33ms – 29.17ms)	20-33 ms,	2 cycles (33.3ms)
Sense Inputs:	Optoisolated, Up to 250 VDC/VAC, <5mA drawn	Up to 300VDC, <2.5mA drawn	Optoisolated, Up to 200VDC, <10 mA drawn
Output Contacts:	Standard: Carry 6A, Break 0.3A @ 125VDC, <6ms	Standard: Carry 5A, Break 30VA, Close 8 ms	Carry 5A, Break 10A
	Hybrid: Carry 6A, Break 10A @ 125VDC, <6ms	Fast: Carry 5A, Break 30VA, Close 4 ms	
	High-Speed: Carry 6A, Break 10A @ 125VDC, Pickup 10us,	High Speed: Carry 5A, Break 1 kVA, Close 0.2 ms	
		Power: Carry 5A, Break 1 kW, Close 16 ms	
Personnel Interaction:	12 pushbuttons, 26 LEDs, Display with detailed menus and substation view	Arrows and keypad, Display with detailed menus and substation view, Many LEDs, Physical key access	6 pushbuttons, 14 LEDs, Display listing key quantities
Notable Additional Features:	Restricted Earth Fault, Over/Underpower, Station DC Monitoring, Open-Phase Detection, Event Reporting, C61850, Breaker Wear Monitoring, Synchrophasors	Restricted Earth Fault, Distance protection, Power swing blocking, Arc protection, Synchrophasors, LTC control, C61850, Event Reporting,	Made with love

[4] These are only guaranteed for a certain operating range. For exact range, consult manufacturer datasheet.
[5] These vary based on the protection type. For exact values for each protection, consult manufacturer datasheet.

3.3 CORE COMPONENTS AND PARTS SELECTION

In this section, the features required for the hardware and software implementations of project specifications are analyzed, and implementation options are proposed. Pros and Cons are weighed, and decisions are made as to the implementation to be used. Major components, such as the microprocessor, are chosen so that more detailed design can begin. Minor components (e.g. an exact model of diode) are chosen in Section 6 as their required specifications will be dependent on other, more major parts selections.

3.3.1 ELECTRONICS PROTECTION

An electrical substation is a very hostile place for electronics, filled with many electromagnetic phenomena capable of destroying them. Current sensors must, by the very nature of the application, be exposed to bursts of high current. System over-voltages are less common, but still seen, and CCVTs exhibit transient behavior that can damage unprotected voltage inputs. Output contacts may have to switch high-current circuits with electromechanical devices in them. Likewise, sense inputs may be energized by electromechanically operated contacts from other devices. Personnel interacting with the device may hold charge, presenting an electro-static discharge (ESD) hazard. If the equipment enclosure is close to yard equipment, or if the relay is used in switchgear, the relay may be exposed to strong external fields from primary-side equipment during disturbances. All these real-world phenomena are regularly present in power systems and constitute an array of risks that can be mitigated by protecting the relay at points where it interfaces with the outside world. Properly verifying an electronic device's hardening against such factors requires highly specialized testing that is far beyond the scope of this project. Instead, two aspects of electronics protection that can be practically demonstrated by the authors have been chosen for further study. The first is transient over-voltage protection and the second is galvanic isolation.

Voltage Transient Protection: When exposed to voltages beyond their rated values, components can fail in a variety of ways. Diodes may undergo a destructive reverse-breakdown. Capacitor dielectrics may break down. In Ohmic devices, excessive heating may be caused by the resulting current flow. The presence of sudden, brief spikes in voltage, such as those caused by ESD, at the relay's inputs and outputs should be avoided. This can be done with a quick-responding voltage regulation circuit that can and will dissipate the energy contained within the transient. Most common overvoltage protection circuits used diodes. A diode behaves much like an open circuit until it is exposed to certain voltage, at which point the insulating mechanisms break down and conduction at a relatively constant voltage drop occurs. When a diode is placed across two input terminals, this has the effect of 'clamping' the voltage to a certain maximum. Several different kinds of devices are used in overvoltage protection, each with different tradeoffs.

Transient Voltage Suppressors (TVS): Transient Voltage Suppressors (TVS) are a specialized kind of diode that is designed to turn on extremely quickly and dissipate large amounts of energy for a short period of time (Fig. 3.17). They are similar in their operation to Zener diodes, but are intended specifically for withstanding transients. Thus, their protective performance is superior. However, their imprecise regulation under reverse-breakdown conditions makes them a poor choice for continuous regulation.

TVS are available in both uni-directional and bi-directional packages. In their bi-directional form, two TVS are placed in series. During an overvoltage, one diode becomes forward-biased while the other experiences reverse-breakdown. The result is an overvoltage protection that functions for large positive or negative voltages. One important characteristic of a TVS is its 'dynamic resistance'. During high-speed transients, such as ESD, there is still a notable ESR with the TVS. In these situations, it is better modeled as a resistor in series with a voltage source than a voltage source. This is important to understand when picking the diodes for each circuit. For while a TVS diode must break down for an overvoltage, it must also keep the voltage within the absolute maximum rating of the device it's protecting. For PHATCAT, the overvoltage to be applied will be 150% of the channel's rating. So, we would calculate the current expected to flow through the TVS for this event and ensure that will keep the voltage within the rated maximum voltage. In other words, V_{CL} must be below the absolute maximum rating of the protected device and V_{BR} must be

above the desired operating range of the protected device. Another important factor to keep in mind with TVS is their capacitance; while the input signals in PHATCAT are DC or relatively low frequency, it should be noted that TVS diodes will ultimately decrease the bandwidth of the channels they protect.

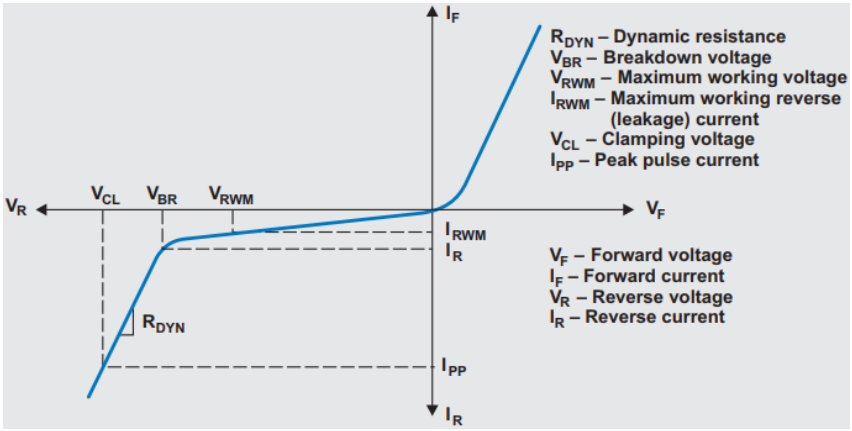


Fig. 3.17. I-V Characteristic of a TVS Diode. Courtesy of Texas Instruments.

Metal-Oxide Varistors (MOV): Metal-Oxide Varistors (MOV) are voltage-varying resistors that are similar to diodes in many ways. The material between the two electrodes of the device consists of many metal-oxides which effectively act as many back-to-back diode pairs. Much like diodes, these experience a breakdown past a certain forward or reverse voltage and begin to conduct. MOV are capable of dissipating larger amounts of power than TVS, but, with every breakdown, the material within them degrades. Thus, they have a lifetime rated energy that they can dissipate before they can no longer properly regulate voltage. MOV are better suited for high-power applications such as mains protection, while TVS are better suited for protecting electronics.

Schottky Diodes: Schottky diodes utilize a metal-semiconductor junction instead of the traditional PN junction. The result is a smaller built-in potential and consequently a lower forward voltage. This makes them capable of very fast switching but leaves them with a relatively low reverse-breakdown voltage. In protection circuits, they may be needed where the reverse-breakdown voltages common to a TVS are too high to offer protection.

Overvoltage Protection Selection: For the voltage and current sensing, sense inputs, and output contacts, the rated voltages will be on the order of 5 – 12V. This makes TVS diodes a suitable selection. The exact model will have to vary based on the channel's rated voltages. It should break down for any voltage above the recommended operating range but clamp the voltage to less than the absolute maximum rating for a 15ms pulse of 150% overvoltage. If the recommended operating range and the absolute maximum ratings are the same, the recommended operating range must be de-rated for this project. Series resistors should be used to limit the current that flows during an overvoltage, but care should be taken not to compromise the accuracy of the circuits during normal operating conditions. For differential inputs, care should be taken to not only limit the differential mode voltage but also to limit the common mode voltage with both respect to ground and V_{cc}. If a TVS can not be found with a low enough voltage for the application (e.g. if a pin must be limited to V_{cc} + 0.3V but must swing to V_{cc}) then a Schottky diode will be used.

There is one important factor to consider when applying protection diodes to the current sense circuit. A high CT ratio is being used, meaning that the secondary side current will be small (on the scale of mA). All diodes have some nonzero leakage current when they are turned off. This alternate current path may result in some induced CT current not passing through the sense resistor. Thus, the protection diodes used in the current sense circuit must have a low leakage current.

Galvanic Isolation: There are two ways that current can destroy components, thermal and mechanical. All real-world components have some nonzero resistance. The heat dissipated by the components is given by the expression $P = I^2R$, where P is the amount of power in watts, I is the current flow, and R is the resistance. At high enough currents, this heat can destroy components. In power systems, fault current magnitudes in the tens of thousands of amps are common. Such faults generate extremely powerful magnetic fields that

exert force on conductors. Just like high wind or excessive weight, these forces can exceed the mechanical strength of power system structures such as transformers. If an open circuit is acceptable, a fuse or circuit breaker can be connected in series. A fuse melts if a designed current threshold is exceeded, opening the circuit. Household and commercial circuit breakers operate similarly but instead of melting, they switch contacts, making them resettable. Circuit breakers for utility-level power systems require more complex control, such as can be provided by PHATCAT. We wish to provide PHATCAT with some protection against any harmful currents that may flow from external sources and damage its electronics. This is best accomplished by eliminating any electrical connection between PHATCAT's core electronics and its various inputs and outputs. There are two commonly-used methods for coupling electrical circuits without connecting them with a conductive path: magnetic coupling and optical coupling.

Magnetic coupling between two circuits is achieved when a time-changing voltage in one circuit is induced in response to the magnetic flux generated by a time-changing voltage in another circuit. This allows for the reproduction of a sinusoidal input signal while maintaining isolation. This is most commonly realized through the use of a transformer, which is really no more than a device designed to maximize this magnetic coupling.

Optical coupling between two circuits is achieved when a voltage in one circuit causes a semiconductor device to emit photons that, in turn, cause excess carrier generation in a photo-sensitive semiconductor device, causing a voltage. This is most commonly realized through the use of an optocoupler. Optocouplers have an advantage over transformers in that they can pass a DC signal and do not create a magnetic field that can cause noise, but they cannot transfer an appreciable amount of power. They also cannot, on their own, reproduce a sinusoidal signal; the input-controlled LED simply supplies the base current for a photo-sensitive BJT.

There is a third kind of device method for obtaining isolation - an isolation amplifier. An isolation amplifier is not a third method physical mechanism of isolation. Rather, it is an amplifier implemented on an integrated circuit that utilizes magnetic or optical coupling to provide isolation as well as amplification. Modern isolation amplifiers can provide the benefits of both optocouplers and transformers. They are compact, can replicate both AC and DC, and generate little noise. For each part of PHATCAT that interfaces with outside signals, a method of isolation must be chosen.

For the current sense inputs, the CT being used to sense the input current inherently provides isolation. (see 3.3.2 - Current Sensing for more details).

For the voltage sense inputs, either an isolation amplifier or an isolation amplifier must be used; a sinusoidal voltage must be reproduced linearly at the isolators output.

For the output contacts and sense inputs, only a 'high' or 'low' signal must be passed through. Since this signal will be DC, an optocoupler is the simple solution.

Voltage Sensing Part Selection: If an isolation amplifier is used, the isolation circuit simply takes a ±10V max voltage from a resistive voltage divider and reproduces it at the output. If a voltage transformer is used, a turns ratio may be selected that both steps down the voltage and provides isolation. Regardless of the method, there are several important characteristics of this isolation circuit. It should have very minimal phase shift, though it does not need a large bandwidth. A differential input and output is preferred, so that common mode noise can be canceled at the ADC. It does not need to drive any load. In many projects, the bulk of a transformer rules it out. However, PHATCAT will fit in a 19" rack and sufficient height must be allowed for easy access to screw-terminals on the rear. This makes space a lesser concern. Listed below are the isolation amplifier and transformer found to be most suited to the project's needs:

Table 3.2. Considered Transformer and Isolation Amplifier

Component:	Triad Magnetics 237-1554-ND Transformer	TI ISO124 Isolation Amplifier
Input Voltage:	115V RMS	Up to ±18V
Output Voltage:	10V RMS	Up to ±18V
Isolation Strength:	2.5kV RMS	1.5kV RMS
Cost:	$4.80	$20

The TI amplifier selected boasts very impressive amplifier characteristics, with .01% linearity. The lack of external components and fixed unity gain make its application very simple. Reference designs are available on the web that allow for comparable (but lower) performance at a much lower price point, but these require additional design and many discrete components. A suitable transformer is available that, likely due to its very low power rating (1VA), is very cheap. This brings a hidden benefit—the low-performance core cannot produce a high secondary current, meaning that there is some current-limiting built-in. It provides superior isolation capabilities at a much lower price point. It can be expected that, being a transformer, it will be less accurate than the amplifier. However, because the current in it will be very low (the protection and ADC circuit is expected to have an input resistance on the order of megaohms), there will be little temperature change and the error will be fairly constant. The signal processing can then be calibrated to account for any standing component error. Thus, the Triad Magnetics 237-1554-ND Transformer will be used to provide isolation for the voltage sensing circuits.

Optocoupler Selection: For the sense inputs, the optocoupler takes in a low voltage, stepped down from 125VDC via voltage divider, that turns on the LED and thus biases the BJT. This BJT can be used with a GPI pin with a built-in pull-up or pull-down resistor to set the input high or low. This makes the optocoupler requirements fairly simple. It should be able to withstand the microcontroller voltage level. For the sense inputs, it need not drive any load. For the output contacts, it may have to be used to bias a BJT with a greater current-carrying capacity in order to energize the coil. It need not switch exceptionally fast or isolate against exceptionally high voltages. Thus, a Vishay TCMT4100 optocoupler will suffice. It comes in a four-channel package, conveniently allowing for one component for the sense inputs and output contact isolations, respectively.

3.3.2 Current Sensing

There must be some method for converting the high-amperage signal provided by input CTs to a voltage suitable for ADC. Two methods are considered.

Hall-Effect Current Sensor: A Hall Effect sensor is a device which can be implemented throughout circuit design to measure current flow. The current can then be read as a low voltage source proportional to the current flowing through the sensor. What's important to understand is how these sensors utilize the Hall Effect and how that could exactly apply to in this design. When a current is sent through a semiconductor, a continuous flow of current is passed through the material [3.3]. Once placed inside a magnetic field, the flux deflects the charge carriers known as electrons and holes [3.4]. Reference figure 3.18 for a diagram visualization of how this effect is seen.

As these charge carriers separate, a potential difference is produced across the semiconductor. The voltage measured across the plate is called the Hall Voltage and is proportional to the magnetic field perpendicular

to the device. The voltage is typically in the range of a few millivolts even with a strong magnetic field. Typically, an op-amp is used to improve the signal strength and sensitivity of the device [3.5].

Now that a background in how a Hall Effect sensor works, a comparison of the advantages and disadvantages can be discussed. Looking at the disadvantages first, since this component relies on the magnetic field to measure the current, external interference can distort the readings. Since the voltage is in millivolts, the accuracy is very sensitive. This leads into another downfall of Hall effect, which is the drift in DC offset as temperature increases.

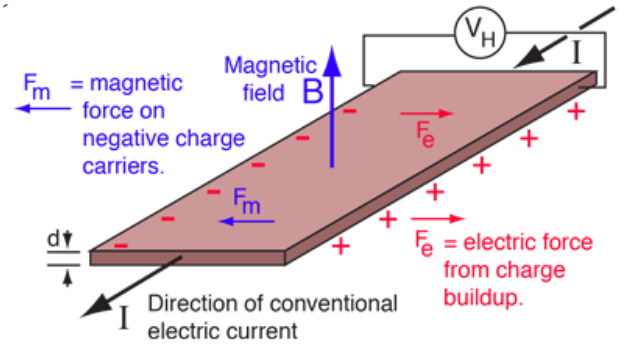


Fig. 3.18. Hall effect seen in an IC. Reproduced with the permission of HyperPhysics, copyright Rod Nave, Georgia State Univ.

The sensors have a broad operating temperature range from $-40^{\circ}C$ to $150^{\circ}C$ depending on the component design [3.6]. As the temperature of the semiconductor increases, the resistivity changes which relates to conductivity of semiconductors. The current flow increases as the resistance decreases which is known to be a contributing factor to the resulting Hall Voltage. It is also a basic equation seen from Ohm's law, V=IR. With an expected max peak amperage of 30 amps, the temperature will influence the voltage signal which is already sensitive due to the low voltage across the semiconductor plate.

Equally important that will now be discussed are the advantages and benefits why these IC sensors are used in electronic designs. Hall Effect sensors provide an accurate output voltage when operating within preset criteria from the datasheet. While inside of the recommended operating range, the sensor will be able to monitor the current and provide galvanic isolation to the cascaded electrical components. This is a major consideration when protection is desired. Also, the sensor offers a nonintrusive addition of resistance since the input and output are isolated. Additionally, the power consumption is low. This is particularly important when high current is going to be measured. The thermal heat dissipated by the IC is dependent upon the design and is specific to each component.

Implementing the use of an IC using the Hall Effect sensor will allow for high currents to be measured and transverse them into low voltage signals. The signal output will be an analog linear output which will need to be converted to digital for the microcontroller to eventually interpret. The signal read will be directly proportional to the magnetic field created by the current flowing across the IC. The Hall Effect will allow the voltage created to be read which will allow us to relate it to the current. This will be a critical part in the relay design which allows for the quotative measurements in the current fluctuation.

Current Transformer: A second component which will be considered in the implementation in the relay design for current sensing is a current transformer (CT). A CT is a device designed to have an input on the primary input which is then reduced by a specific ratio. The secondary coil provides a proportional step down to the current flowing in the primary winding which is now the output of the transformer. These CT's allow for reading high currents with low current instrumentation.

For example, a 5-ampere rated multimeter could be used to read power distribution line with over 3,000-amperes flowing through the line.

The fundamentals behind how the current is reduced is known as the transformer turn ratio. The ratio refers to the number of times the wire has been wrapped around the transformer core [3.7]. Refer to fig. 3.20 for an illustration how the core is constructed. The equation used for these components is known as $\frac{N_p}{N_S} = \frac{V_p}{V_S} = n$. Where n is equal to the turn ratio of the primary relative to the secondary. In this case, the turn ratio is designed so the resulting current will be stepped down to a more quantitative level for sensitive instruments.

Referring to back figure 3.1, the design illustrates that the two coils do not physically touch. They are linked magnetically by the fields induced by the windings wrapped around the laminated iron core. When an alternating current flows through the windings, the magnetic flux increases dependent on the amount of current and number of turns in the winding. This phenomenon is known as Faradays law of electromagnetic induction [3.8].

One of the key benefits that a CT offers in terms of design is the galvanic isolation. There is no direct path for the current to flow, the only current flowing will be indirect and related to the magnetic flux in the iron core. This offers the benefit of isolation where radically different voltage potentials are seen and where the result of this isolation being violated could result in hazardous conditions to sensitive components.

Referring to fig. 3.19, the location of the ammeter will be replaced with a current sense shunt resistor which will provide a low voltage signal. This is described in further detail later in this section. Additionally, it's important to note that if the multimeter or resistor is taken out of the circuit, it must be replaced with a short. The reason for this is derived from ohm's law. With V=IR, the resistance can be considered going to infinity as the current flow will also be reduce. This results in the voltage drop across an open circuit to surge and become high enough to destroy sensitive components connected to the transformer.

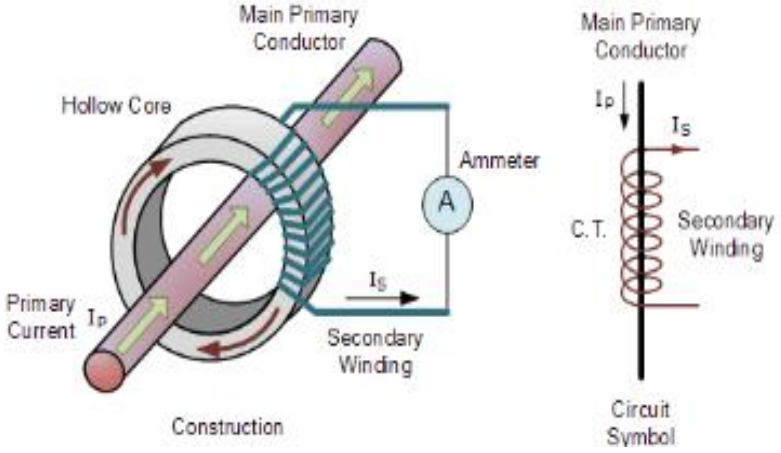


Fig. 3.19. Current Transformer with terminals. Reproduced with the permission of Electronics Tutorials www.electronics-tutorials.ws

The low voltage seen at the resistor will be used in determining phase and current magnitudes on the primary side by knowing the ratios in which the transformer has been designed for. This component provides galvanic isolation, precision and a reduction in the current which is crucial in the design of a relay.

There are a few important concepts that must be introduced to fully understand the principle of how the current transformer will be implemented to effectively step down the current. The term "effective" is meant to derive the concerns when using a CT and how it can become a burden if the component is not picked to meet the specifications of the project. Starting with the foundation, Faraday's law can be considered one of the most applied principles in the application of a transformer. Faraday's law states that the magnitude of induced electromagnetic fields is equal to the rate of change of flux per rate of time. The following equation $\in= N\frac{d\Phi_B}{dt}$ is the mathematical expression to predict how the magnetic induction is quantified. N is the number of turns of wire wound around the core, Φ_B is the magnetic flux through a single loop of the wire.

The turn of the wire must be extensive enough to create a mutual induction between the primary and secondary windings. Usually a soft iron alloy core is used as ferromagnetic material which enhances the magnetic field and acts as a resistance as the core begins to saturate. The saturation rate is defined as the internal magnetic field strength at which the core begins to lose the linear rate at which the magnetic flux is amplified.

The method behind magnetism breaks down into quantum mechanics but, for this research paper, it is sufficient to refer to this phenomenon as the alignment of the domains inside a ferromagnetic material which creates a magnetic field. As the current flowing through the wire wound around the core, the domains in the core begin to align. As more domains begin to align, the core begins to reach saturation. Fig. 3.20

shows representation of the characteristic curve of a CT reaching saturation.

The region before V_k is a linear relationship where the core behaves within normal operating conditions. The V_s represents the RMS value of the sinusoidal voltage at the rated frequency (in this design, 60Hz) and as it increases with the current, the core's ability to resist the alignment of domains begins to decrease. The majority of the current from the primary winding is shunted away from the secondary winding and creates an internal magnetic field inside the CT. Upon reaching saturation, a large increase in current will be seen with small changes in the voltage. This is also expected based upon the saturation graph of a CT. Reaching saturation is an undesirable characteristic as the output on the secondary coil will no longer be a linear relationship which can be analyzed.

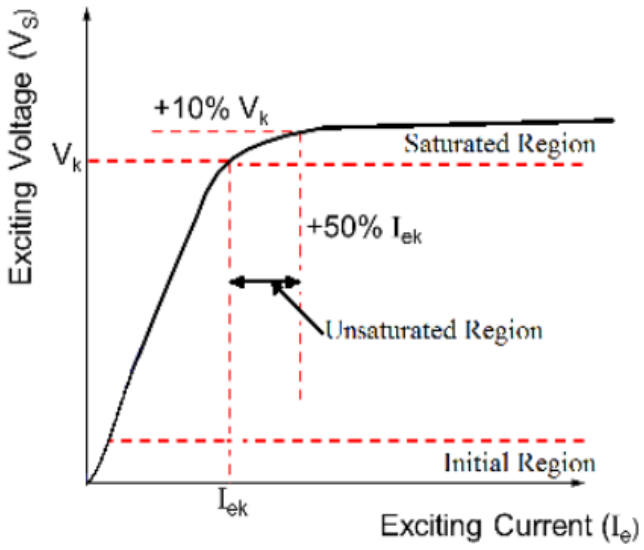


Fig. 3.20. Saturation of a CT. Reproduction permission requested from the International Journal of Pure and Applied Mathematics.

An additional concern of saturation involves the core reaching the point at which the rate at which domains have been aligned, the resistance in the core becomes small. For illustration of this point, fig. 3.2 will be used as an example of a non-ideal transformer layout. The load seen in parallel R_C & X_m is considered the real and imaginary parts of the resistance (known as impedance) seen by the iron alloy core. As the core domains begin to align, the total impedance of this load begins to decrease.

Since the current is known to take the path of least resistance coming from Ohm's Law, a problematic issue for the sense resistor begins to occur. If the datasheet recommended unsaturated region is passed, the core impedance could begin to experience a higher flow of current. This results in a faulty reading across the sense resistor as some of the current from the primary is no longer being proportionate to the secondary winding.

In addition to the concerns of the saturation, the direct current resistance (DCR) can become problematic if not properly dealt with. DCR is defined as the resistance of an inductor as a result of the resistance of the wire used in the winding [3.10].

Most cases, the length of wire is not usually considered since the voltage drop is insignificant. But in transformers, the length of wire used for the windings can be considerable in length. From table 3.4 one of the transformers has a turn ratio of 2500. The length of wire can have a voltage drop across it as the length increases, the resistance of the wire becomes must also increase. The formula $R = \frac{\rho l}{A}$ can be used to calculate the resistance of the windings. By knowing l, the length of the wire, A is the cross-sectional area and ρ is the constant resistivity of the specific material, the total resistance of the windings can be calculated.

A solution to reducing the resistance seen from the length of the wire is to increase the cross-sectional area of the wire. By using a larger gauge wire, the electrons have less resistance to flow through the wire allowing for a lower voltage drop across the length of wire. Since this is not a viable option for a pre-designed transformer, the DCR must be considered in the calculations of the sense resistor. If not, the value of the current sensed will be a false reading as the voltage drop across the windings is not considered.

Referring to table 3.4, the component CR8350-2500-N is expected to have an internal resistance of 57 Ohms which is the resistance predetermined from the manufacture. Considering the resistance will have a

direct impact on the sense resistor, a voltage divider is utilized to calculate the actual voltage of the sense resistor. The following equation $V_{sense} = \frac{R_{sense}}{R_{sense}+R_{DCR}} * V_{induced}$ will be used to calculate the actual voltage on the R_{sense} resistor. By knowing the voltage and resistance, Ohm's law will be utilized to calculate the current. The current seen at the R_{sense} will be the stepped down value which is proportionate to the primary side of the transformer. Fig. 3.21 provides an example of the voltage divider circuit which will be used in calculating V_{sense}.

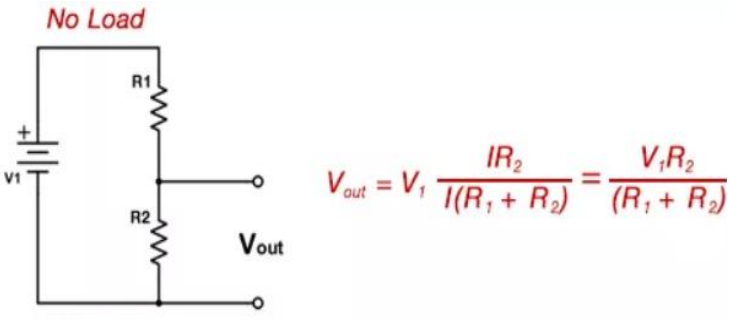


Fig. 3.21. Voltage Divider with no load. Reproduction permission requested from Digikey.

In the professional industry, the sense resistor implemented is commonly found to be a low burden resistor. The reason for this is to reduce the error present in the secondary winding output. The secondary winding will be connected to the sense resistor which will be the load seen by the transformer. For this analysis, R_o will be the sense resistor, connected to the transformer in fig. 3.2 as a secondary-side load. The excitation current I_m determines the maximum accuracy achievable by a certain transformer. The excitation current can be considered a portion of the primary current that causes hysteresis and the eddy current losses of the core. If the values of L_c and R_e are to low due to the permeability of the core is low, the core loss is likely to be high resulting in only a fraction of the current ratio $\frac{I_p}{n}$ will flow through the secondary winding. The fraction of current mentioned is contributing factor to the accuracy of the voltage across R_o. The input current (I_{in}) is comprised of two components, the excitation current (I_m) and the load current I_o. The equation for the current input can be expressed as $I_{in}^2 = I_m^2 + I_o^2$. Then solving for I_m the exciting current equation can be derived to be $I_m = I_{in}\left[1 - \left(\frac{I_o}{I_{in}}\right)^2\right]^{1/2}$. This expression is shown as a graphical representation in fig. 3.22 for the interpretation of how the excitation current and output current will be seen as the input current is increased. The R_e will determine the accuracy of the output current on the secondary terminal as it will shunt part of the input current I_{in} away from the primary windings.

The error in the current I_m will be proportionate to the value of output current going through the sense resistor which will skew the resulting voltage across the load resistor. This can cause a skew in the data and the analysis of real value. By lowering the resistor value R_o relative to the resistance seen by I_m, the current will follow Ohm's law and the current I_m will be reduced as the output current will increase.

Therefore, the accuracy of the voltage seen by the sense resistor will increase, providing a more precise reading in the data. Achieving the highest accuracy relies upon the sense resistor load value and the impedance of the transformer. In practice, the resistor value must also be large enough to produce a readable voltage signal in which the magnitude of the signal will not be affected by the noise in the system. There is a balance in which the sense resistor will be chosen in which the accuracy

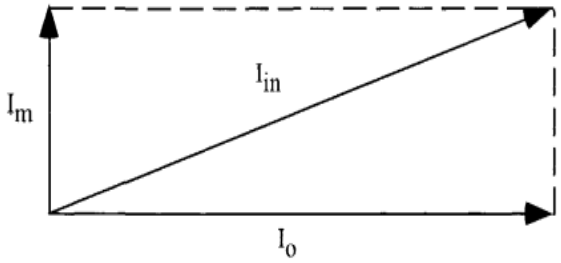


Fig. 3.22. Input current relationship. Reproduced from TRANSFORMER AND INDUCTOR DESIGN HANDBOOK Third Edition, Revised and Expanded, COLONEL WM. T. MCLYMAN, Kg Magnetics, Inc., Idyllwild, California, U.S.A. for educational use only

will be high enough while the signal produce stays within the range desired.

A current transformer operates on the concept of having a primary input current and secondary output current and that the two of them ideally operate directly proportionally to each other. The primary will try to output a constant current to the secondary coil and the connecting load independent of the size (total impedance) of the load seen. In this design, the transformer will operate into a resistive load until the voltage induced is reached where either the saturation of the core is reached, or it cause voltage breakdown. The current injected into the primary winding of the transformer is not dependent on the secondary load current. Therefore, if the load that is connected to the secondary winding is removed while the primary load is connected, the flux in the core will spike since there is no longer an opposing current on the secondary winding.

While testing the current transformers, everything from the discussion above must be considered and analyzed. This will ensure that the components will operate as desired once integrated with the rest of the components in the relay.

Diving into the current sense shunt resistor, again Ohms law will be used to create a voltage across this resistor at know resistance value. By knowing the value of the resistor in addition to the voltage across it, the current can be measure using $I = \frac{V}{R}$. The values predicted were found in the methodology selection below being around 0.4 to 12mA. With a value for the current, and a desire of a voltage to be a max ±10V, the sense resistor can be specified to be being around 800Ω.

This will provide the following 10 volts by simply solving for $V_{Sense} = 12x10^{-3} * 830\Omega$ where $V_{Sense} = 9.96V$. The current sense shunt resistor is planned to have a ±1% accuracy. This will change the V_{Sense} by ±1%. So, the real expected V_{Sense} at the max amperage will between $V_{Sense} = 9.85V$ & $V_{Sense} = 10.05V$. The real expected V_{Sense} at the minimal amperage will between $V_{Sense} = 335mV$ & $V_{Sense} = 329mV$.

The voltage signals will be increased or decrease depending on the current sensed at the current sense shunt resistor. This will be done using a PGA and controlled by the microcontroller which will determine the value of the signal and decide on the gain level. This will allow for low signals to be amplified for the microcontroller to read. It will be much easier to sense a 2V signal in comparison to a signal in millivolts.

The thermal heat generated in a resistor changes the resistance dependent upon the type of component. Each resistor component is specified with a parts per million per degree centigrade (ppm/°C) which is rate at which the resistance of the component begins to break down at the temperature increases. With a max current rating of 12mA, the power dissipated by the resistor can be estimated using the simple equation $P = IV$. Plugging in the values for I_{max} and V_{max} the P_{max} is calculated to be 120 mWatts (W).

With the knowledge on values the current sense shunt resistor will be exposed to, the component can be selected and chosen to meet the desired specifications. With only 120mW being dissipated by the resistor, it will allow for the temperature of the resistor to be relatively low which will keep the value of the resistance steady. In the methodology selection below, table 3.3 will be used to compare different components which were found to be suitable choices for the design requirements.

Methodology Selection: Table 3.3 below is for quick reference of the characteristics these two components have. This will be used in analyzing which will be the best fit for the design in this project. The data below was taken from datasheets from an electronic supply website. Another concern while researching these components was the availability of the components. As technology starts to progress, electronic designs evolve and soon replace the components which have been chosen for implementation. The components considered from the websites a sufficient stock that if they are discontinued, the design specification will not suffer. An additional step taken to avoid this catastrophe is to purchase extra components in the worst-case scenario they get damaged.

The transformer listed in table 3.3 has a 2500:1 current ratio with a ±10% accuracy and a 57 ohm through hole. The max amperage on the primary input of the transformer will be 30 amps, at this value the secondary

output will be seen around 12mA. With a low of 1 amp on the primary side, the output on the secondary output will be seen around .4mA. Knowing this, the current sense shunt resistor can be scaled to produce a max 10-volt signal which will be compatible with the components cascaded in the schematic.

The hall effect IC listed in table 3.3 is rated for a 30-amp input with a linear output. After considering a few different IC components, the ACS712 was a good medium for comparing the two devices. The hall effect has a linear relation similar to the current transformer. The linearity of which the voltage and the current relate can be attributed to the saturation of the flux concentration as the max current of the IC is reached. This specific IC can withstand a 100A overcurrent transient pulse for 100ms and operates normally from $-40^{\circ}C \ to \ 85^{\circ}C$. The voltage output ranges 2.5V to 4.5V from 0-30amps but is also dependent on ambient temperature of the IC. Having a varying output which is dependent of the temperature is a concern since the design will be incased and heat may vary. Although, the output error is much lower than the current transformer at only ±1.5%.

Unlike the current transformer, the hall effect sensor requires a power supply for proper implementation and creates a low-offset voltage. The off-set voltage can affect the value of voltage signal which would obviously affect the output and would have to be considered when the signal is analyzed. Stated previously, another concern is the sensitivity of these components to magnetic fields. The concern of having 8 IC's which are sensitive to magnetic fields can lead to complications when integrating the components in this design.

Table 3.3 Current Sensing Methodology Comparison

Characteristic	**Current transformer**	**Hall Effect Sensor**
Component	CR8350-2500-N	ACS712ELCTR-30A-T
Linear output	Strong (100amps)	Medium(30amps)
Cost	$13.23	$4.50
Galvanic Isolation	Strong	Strong
Footprint	14x37mm^2	5x6 mm^2
DC offset	No	Yes
Sensitivity	Low	High
Phase Shift	Very low	Medium

After discussing the desire of the components in this design along with the advantages and disadvantages, the current transformer has been selected for the following reasons. A linear output is a major desire where the voltage from the sense resistor will need to follow a proportionate to the current flowing through it. As seen from table 3.3, the cost of a CT does run a bit higher than that of the hall sensor, but it comes with its valuable trade off. The phase is going to be an important factor in monitoring the signal and the magnitude of the harmonics.

While there can be some phase shift, it will much less than the phase shift that can be seen in the Hall Effect. Additionally, the footprint that the CT has will be slightly bigger then the sensor, but this comes with the benefit of a having a higher saturation level of the iron core. The size of the core allows for a higher saturation level which provides a larger range of a linear output. Along with size of the core, the windings

of the CT provide for the ratio to be larger so a smaller current can be produced in the output of the CT. Another reason the CT was chosen was due to the sensitivity of the sensor in comparison of the two.

Any outside magnetic field or noise could be high enough to affect the ~2.5-4.5V signal the sensor can produce. The strength of the voltage from the CT can be controlled by the value of the sense resistor which can be adjusted according to desire. For these reasons, the current transformer looks to be the best choice for the current sensing methodology.

Table 3.4 compares the current transformers considered to be used in this project. Each component comes with its advantages and disadvantages. Table 3.4 will be used to optimize the process of picking the best-case solution.

Table 3.4 Current Transformer Comparison

Characteristic	**Current Transformer**		
Component #	CR8350-2500-N	DROK - 200072	CR7-SHL-152
Frequency range (Hz)	20.0 – 1.0k	50.0/60.0	50.0-400.0
Max current input current with linear output (Amps)	100.0	100.0	40.0 VA
DCR rating (Ω)	57.0	42.0	Not supplied
Max voltage for saturation (V_{RMS})	10.5	Not supplied	Not supplied
Operating temperatures (°C)	-40.0 - 85.0	-40.0 – 85.0	-20 – 75.0
Turn Ratio	2500:1	1000:1	1500:5
Cost $	13.23	4.80	50.25

The initial selection of components will begin with the current transformer which was compared with the hall effect sensor in table 3.3.

Starting with the CR8350-2500-N transformer, this component is available for PCB mounted option which allows for easy implementation when designing the PCB. The revenue grade core is made from silicon steel providing the most linear response over the current level at a max of 100Amps. This quality will be detrimental in the design specification as a linear response up to max of 30Amps will be necessary to analyze an accurate voltage to current relation.

The more extensive design, the nanocrystalline amorphous, comes with the same core but with a higher saturation and linear response for high frequency applications. Since this relay will be for a 60Hz input, there is no need for the expensive device. Lastly, the turn ratio is 2500:1 which provides a very low sense current on the secondary winding. This will allow for a sense resistor value to be chosen with precision which follows the design constraints covered above. The accuracy of this transformer is designed with power metering in mind, so the accuracy is precise.

Secondly, the DROK-200072 transformer was included in the comparison for the benefits of the price and the linear output of up to 100Amps. This transformer includes a clamping design which allows for the

transformer to open, allowing wires to be left untouched and still have the current analyzed. This unit does not come with PCB mounting but rather two terminal wires which are connected to the secondary winding. A concern with this component would be a faulty connecting between the two clamping points which could interfere with the proper current sensing.

In comparison with a solid ring design, the possibility is eliminated reducing any chance of a faulty reading from a loose connection. Also, the voltage saturation is not included in the data sheet which would leave testing the device before fully committing to this component. The testing for the voltage saturation would include raising the voltage of the secondary winding until voltage until the CT is in saturation. This saturation point is reached with the voltage output no longer linearly relates to the current which is on the primary winding. The current will increase at a nonlinear rate as the voltage will not increase anywhere close to the same rate. The test voltage will then be slowly reduced to zero which will demagnetize the transformer as no current will be passing through the primary winding.

The test results will then be plotted in a logarithmic scale and evaluated to find the transition "knee point" at which saturation of the core is reached. This is an easy test to preform but could be a fruitless endeavor as the result of the core saturation could be to low for the desired voltage signal across the load resistance.

In summary, although this component provides the same characteristics as the previous component, it does not provide the guarantee of that the first transformer provides. The turn ratio is also lower at a 1000:1 ratio which will provide more current on the secondary terminal. This is not an issue but a worthy mention as the sense resistor will must be calculated to accommodate the difference.

Lastly, the CR7-SHL-152 transformer was included in the comparison as a viable candidate transformer as an ANSI certified power metering transformer. This unit is designed for minimal phase angle error and high accuracy output. The transformer selected has an accuracy of 0.3% at a load of 1.8 ohms on the secondary winding. This accuracy begins to decrease as the load resistance increases. With a turn ratio of 300:1, the max current of 30Amps would be at 100mA. With a max voltage of 180mVolts, the signal would be too low for a practical use.

In this case, the design cannot depend on the 0.3% accuracy that this transformer provides. It is still a viable option as the accuracy should not change much but the price of the component is significantly higher than the other components compared. Also, the voltage saturation is not included in the data sheet. This would require the same testing described earlier above in this section to be completed to determine the saturation voltage. The SHL version does not include PCB mounting feet but rather has wires connected to the terminal which would need to be mounted to the PCB.

In summary, though CR7-SHL-152 has supreme accuracy but the accuracy does not include the range in which the transformer will be operating at. Also the price of each component would is quite large in comparison with the other transformers. This is a reason that must be considered where eight current transformers will be implemented and the cost can surpass the budget planned. So although the accuracy and phase delta would be impeccable, the cost may have a larger impact in the consideration of this component.

After the discussion above and the table 3.4. the component CR8350-2500-N is the initial design component which will step down the current to analytical level. This is due to the advantages it provides and the simplistic implementation. As seen in the table 3.3 was that the cost was more than the sensor, but the phase will be a critical step in this power relay build. As such, the CR8350-2500-N current transformer will be implemented for the current sensing section of this design.

Table 3.5 Current Sensing Shunt Resistor Comparison

Current Sense Shunt Resistor			
Component #	Y0101830R000F9L-ND (Vishay Foil Resistors)	100 series – type 106 (Riedon)	71-RS2B-830 (Vishay)
Tolerance %	±1.0	±0.005	±1.0
ppm/°C	±2.0	±2.0	±20.0
Electrostatic Discharge (ESD) kV	25.0	-	-
Power rating (W)	1.0	1.0	3.0
Temperature Coefficient of Resistance (TCR) °C	-55.0 ~ 125.0	-55.0 ~ 145.0	-65.0 ~ 250.0
Cost $	11.65	Pending	2.07

The next component selected for this section is the 71-RS2B-830 current sensing shunt resistor. This was selected due to the tolerance flexibility and the ability to have samples provided by Vishay. The ppm/°C is higher than the other components in the table but again with only 120mW being dissipated by the resistor, this does not seem to be a point of concern. It is the cheapest resistor listed while still providing the desired specifications. After discussion with the members of this design, the 71-RS2B-830 current sensing shunt resistor will be implemented for the current sensing section of this design.

3.3.3 Low-Pass Filters

In order to understand the application of electronic filters, the basic operation of how these filters work must first be explained. The circuit theory of an electronic filter first starts with a network that alters the characteristics of the signal frequency. The characteristics most often altered is the magnitude and phase which is dependent on the frequency. Active filters ideally keep the signal isolated in efforts to keep from allowing noise being introduced into the system. Filters are used implemented in circuit design to emphasize the signals within a predetermined frequency range and reject any signals outside the range.

The signals inside the range of the filter are within what is called the passband of the filter. The other important part to note is where the -3dB frequency is set which is also known as the cutoff frequency. The cutoff frequency is where the gain of the signal has dropped 3 decibels or 0.707 of its maximum voltage. The signals outside specifications that are past the -3dB are considered within the skirt or transition region and have an attenuated gain. Simply put, this allows for the system to discern between the signals desired and which are to be ignored. From Texas Instruments a very simplistic diagram of how a filter can affect the amplitude of a signal as the frequency increases in shown in figure 3.23 below [3.11].

There are active and passive filters with each having their advantages and disadvantages. A passive filter has few parts and doesn't require a power source but the roll-off of the filter is fixed based upon the resistor and capacitor used. They also have no gain which doesn't allow for the signal amplitude to increase. Additionally, there is no isolation between the input and output so the impedance will be seen between these two can be rather high.

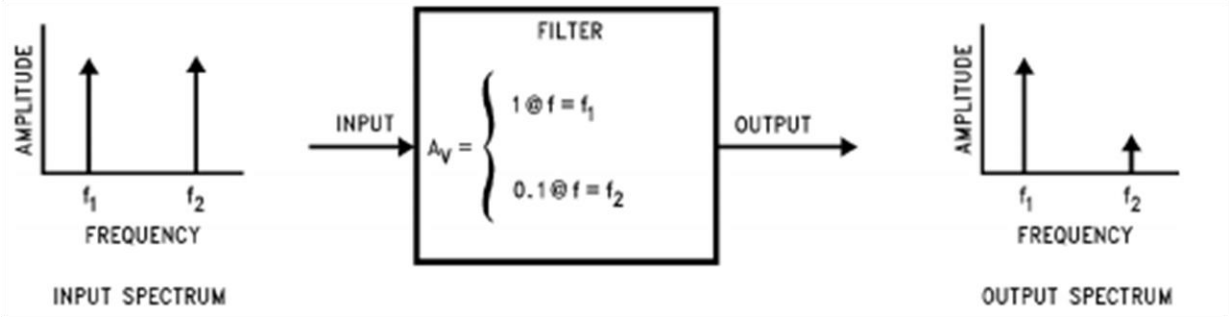


Fig. 3.23. Amplitude vs. frequency affected by a filter. Reproduction permission requested from Texas Instruments.

Active filters require a power source, but they can also be built to provide gain for the signal. The operational amplifier provides isolation between the input and the output allowing for the impedances to be higher on the input and lower on the output. Additionally, by cascading active filters, the roll-off can be much sharper which provides a quicker attenuation of the signal. Since our design requires a roll-off which can be altered and the addition of isolation, an active filter will be implemented for this project.

The power relay that is being built will have low frequency signals which are desired while the high frequencies will be attenuated. Knowing this, a low-pass filter will be chosen with the goal to isolate the low frequency signal and attenuate the higher frequencies. The desired range of frequencies will be from 60Hz to 300Hz. This range will include the fundamental frequency of 60Hz and up to the 5th harmonic of 300Hz. The harmonics are important in this case because they will allow for us to detect certain events in the power system.

The waveform distortion is made from higher frequency waveforms that are part of the fundamental frequency of the signal. From the distortion present in the fundamental waveform, PHATCAT will perform the harmonic blocking functionality described in the Relevant Technologies section. Fig. 3.24 shows the progression of harmonics and how they are superimposed to the fundamental waveform [3.12].

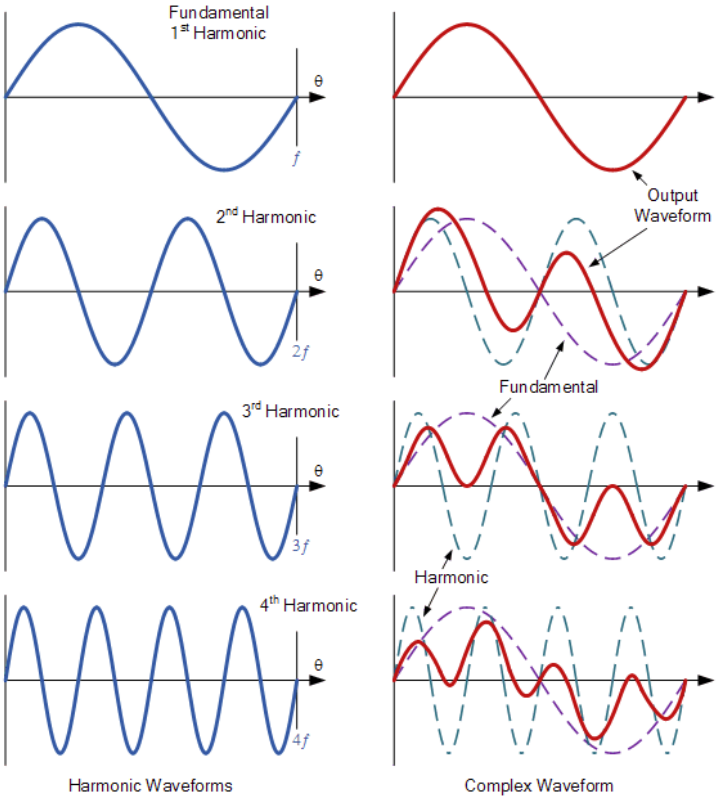


Fig. 3.24. Fundamental frequency and additional harmonics. Reproduced with the permission of Electronics Tutorials www.electronics-tutorials.ws

Knowing that a lowpass filter will be used, the filter type can now be discussed. Four of the most common filters implemented are the Chebyshev, Elliptic, Butterworth and the Bessel designs (Fig. 3.25, 3.26). Starting with the Chebyshev design, these filters are designed for steeper roll-off but allow for ripple to be seen in the passband. The ripple and steepness of the filter are inversely proportional to each other meaning as the roll-off becomes faster, the ripple must increase. This is lousy for the electronics in the electrical system as the spike in the passband must be considered. The spike means the magnitude of the

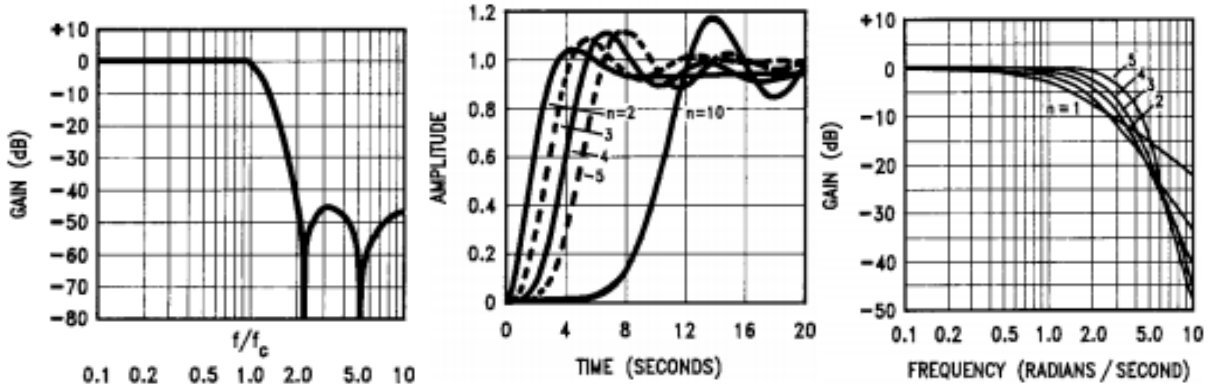


Fig. 3.25. Elliptic (Left), Chebyshev (Center), and Bessel (Right) filters at various orders. Reproduction permission requested from Texas Instruments.

signal causes a spike in voltage with can affect the signal output and any components attached. The faster roll-off provides a sharper transition with a lower order filter.

Ultimately, the Elliptic filter provides the steepest roll-off but the amplitude will see ripple in both the bandpass and stopband. The phase response also becomes non-linear which adds complications when analyzing the phase output. Implementing this filter will result in the fastest attenuation with the lowest order filter but comes with the negative impacts to the phase and ripple. Since the phase will be important in analyzing faults, this filter would provide significant consequences trade-offs for the increase in the attenuation rate.

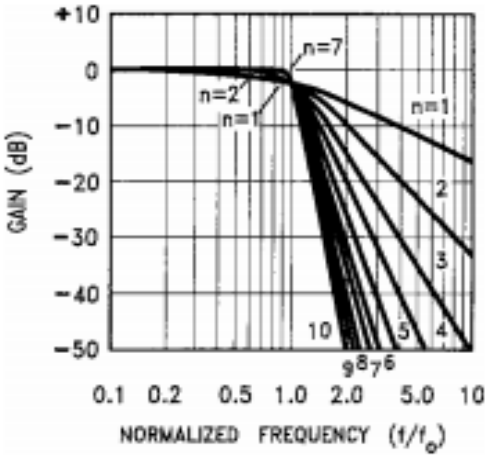


Fig. 3.26. Butterworth filter of various orders. Reproduction permission requested from Texas Instruments.

Next, Butterworth filter, the passband provides a maximally flat response where no ripple can be seen in the filter response. This is helpful when distortion of the signal is critical and affecting it becomes a desire by the circuit designer. The roll-off is smooth and monatomic for each pole of the filter. Each pole increases the order along with the roll-off rate allowing for faster attenuation.

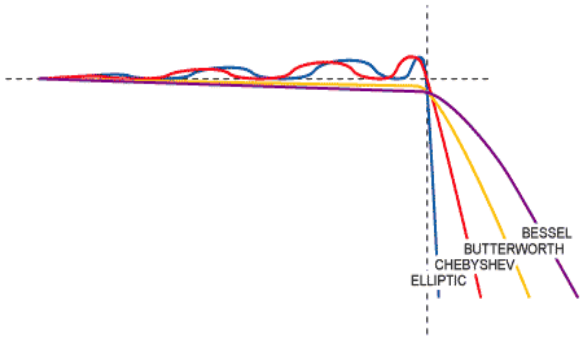
With a single pole filter the roll-off rate is 20dB per decade for each pole implemented. If a 6-pole Butterworth filter is implemented, the roll-off rate with be 120dB per decade. This would require 3 operational amplifiers but still provide the linear relationship in the phase. There has been a table developed by mathematicians where the resulting Butterworth polynomials relate to the order of the filter.

Lastly, the Bessel filter is designed for more of a relaxed roll-off rate with the slowest attenuation of the signal. Similar to the Butterworth filter, there will be no ripple in the passband and provides a fairly linear phase response. Much like the attenuation, the phase linearity will increase with each order of the filter. This filter would be ideal if the attenuation of the signal was not a concern but when compared to the Butterworth filter, the order of the filter can be less and yet provided a faster roll-off.

Reference to table 3.6 can be used to see a quick comparison of the four classic filter types. This table compares the important factors which will be crucial in picking the ideal filter for the electrical circuit design. After the discussion of five main types of filters, the advantages of each filter were discussed and are compared in table 3.6. Considering the desire of a steep roll-off along with a maximally flat passband the two filters further researched were the Bessel and Butterworth filter. Due to the roll-off of a Bessel being much slower and requiring additional stages in comparison to the Butterworth design, the Bessel was

dismissed as a consideration in this design. Therefore, the type of filter being implemented in this electronics design will be the Butterworth filter.

Table 3.6. Four common filter design comparison. Permission for filter response image requested from Texas Instruments.

Filter Type	Passband	Rolloff	Phase Response	Filter Response
Butterworth	No ripple	medium	Medium	
Chebyshev	Some ripple	Steep	Medium	
Elliptic	Most ripple	Steepest	Worst	
Bessel	No ripple	slow	Best	

At first, there was consideration to build a 6th order Butterworth filter in the implementation of this design. The filter was going to be a hand-full of op-amps which had been chosen with the intentions that they meet the criteria and could be integrated seamlessly with other components. Along with the op-amp, the resistors and capacitor components values would be derived using the Butterworth table and calculating accordingly. This would lead to the development of the criteria such as the roll-off rate and noise in the signal. By selecting precision components, the filter would be constructed.

Through the research of another component, the analog to digital convertor (ADC), an integrated circuit was found which provides the benefits of a 6th order Butterworth filter. The ADC will use a binary search algorithm to identify anomalies in the signal and communicate with the microcontroller. Low value signals will be boosted with an onboard PGA while having a unity gain for higher value signals. A more thorough and in-depth discussion on the ADC can be found in Section 3.3.6. The component ADS8588S from Texas Instruments will be the component implemented to cover the design needs of the Butterworth filter while offering built-in protection.

3.3.4 Programmable Gain Amplifier

One challenge associated with signal processing for power systems protection is the wide range of amplitudes the current signals can take on. Our largest specified current signal is 30A, and industry-grade relays can often measure in excess of 100A. More sensitive protections, such as ground overcurrent elements, are frequently set to be quite low, comparatively. They may have a pickup value of only 0.5A. Thus, our relay must be accurate within the specified performance for a range of ~36dB. This range is even greater in industry-grade relays. To be as accurate as possible, the analog voltages going to the ADC should have several characteristics:

A) They should all fall within the voltage range the ADC can withstand
B) None of them should be so small as to be difficult to discern from noise
C) None of them should be so large as to cause distortion or clipping
D) The ratio of the signal at the external device input to the voltage seen by the ADC should be as small as possible so as to maximize usage of the ADC's resolution

An amplifier with a large gain will improve (B) and (D) but worsen (C) and possibly violate (A). An amplifier with a small gain will ensure (A) and (C) but worsen (B) and (D). However, using a programmable

gain amplifier (PGA), the benefits of both small and large gains can be realized. As the name implies, a PGA is an amplifier with a gain that can be varied with digital logic. For small signals, the digital logic should increase the gain, maximizing use of the ADC's resolution. For large signals, the digital logic should decrease the gain, to avoid clipping or distortion.

The key specification for PGAs is the number of discrete gain levels they provide. The trade-off is simple: more gain options require more digital data lines to select them. The gains may also be linear or exponential. Given that, for this application, the measured values will either be small (steady-state) or large (fault conditions), it makes sense to use an exponential scale. Using a scale that is a multiple of 2 provides the added benefit of allowing computationally-fast adjustment of internal values as the gain changes. Another factor for consideration is the number of different ongoing gain selection processes to be implemented. If a PGA with 8 gain options (3 gain-select lines) was used for each channel, 42 digital lines would be required just for the PGAs! This is excessive. Rather, it is preferable to group certain quantities based on the likely similarity of their magnitudes. For instance, during normal operations, all of the voltage inputs will be similar (remember that even though the high and low side of the transformer may be at very different voltages, the PTs will normalize them down to the same voltage for input into PHATCAT). During a nearby three-phase fault, all the voltages will be depressed. So, the same gain-select lines can be used for all the voltages. Similar logic is used to group the phase currents and neutral currents. Note that in the event of an unbalanced fault, there may not be uniformity among the measured three phase quantities. The PGA's gain control logic should prioritize accurate measurements for the faulted phases (i.e. optimize gain for the highest current measurement and lowest voltage measurement) but must take care to avoid clipping other measurements. As a result of this optimization, only $3*\log_2(N)$ input control lines will be needed to implement PGAs with N selectable gains. The price for this optimization is that measurements for un-faulted quantities will be less accurate during a fault. This could potentially affect the accuracy of protection algorithms that operate based on many different quantities.

Several PGAs were considered. Their key characteristics are listed in table 3.7.

Table 3.7. Programmable gain amplifiers considered

Chip:	**LTC 6910**	**MAX9939**	**ADS8588S (within ADC)**
Input Range:	11V, rail-to-rail in and out	$\pm$16V (Output: -0.3V to V_{cc} + 0.3)	$\pm$10V
Gain Options:	0, 1, 2, 4, 8, 16, 32, 64	0.2, 1, 10, 20, 30, 40, 60, 80, 119, 157	Not given (internally controlled)
Cost:	$2.84	$1.81	$0 (in ADC cost)
Other Features:		SPI-Programmable	Automatic Control

Notice that the third option is actually contained within the chip selected for ADC. This means that *no additional hardware or control lines are necessary for this implementation*. The block diagram in the chip's data sheet shows a distinct PGA for every channel, meaning that the tradeoffs previously made regarding accuracy are no longer necessary. These factors, joined with the fact that the ADC automatically regulates the PGA gain to achieve the exact purpose the team is trying to achieve (maximizing both resolution and dynamic range), makes the PGA included in the ADS8588S the clear choice. If the ADC did not include a PGA, the LTC6910 would be used. It provides a wide input and output range as well as gains that can be accounted for with a computationally rapid multiplication/division by a factor of two.

3.3.5 ANALOG-TO-DIGITAL CONVERSION

The analog-to-digital conversion process will convert the low-voltage signals coming from the programmable gain amplifier filters into logic-level digital values for the microcontroller. Many microcontrollers contain an ADC unit, but, as will be discussed, there are several features desirable for this project that are only found in dedicated ADCs.

Conversion Method: There are three ADC methods commonly used. Flash conversion utilizes comparator circuitry with a resistor ladder. There is a comparator for every voltage step, meaning that an *n-bit* ADC requires 2^n comparators. Due to the large number of comparators used, these devices consume lots of power and can take up a lot of IC real-estate. However, flash conversion is very fast. A successive approximation converter (SAR) still uses comparators but adds counting logic. Starting with the MSB (n = 1), the magnitude of the input voltage is compared to a voltage reference of $V_{ref} / 2^n$. If the input is greater, the value is set and $V_{ref} / 2^n$ is subtracted from the input. In this way, the region of possible inputs is iteratively divided in two until all output bits have been set. As such, an *n-bit* successive approximation takes *n* cycles to perform. This presents lower hardware requirements than flash conversion but is slower. SAR represents a balance between flash conversion and the third method of ADC, sigma-delta conversion. Sigma-delta utilizes techniques such as oversampling and noise shaping to produce a high-speed, 1-bit digital output that is then decimated down to a more easily usable data rate. Because it does not rely on the resistor networks used in SAR and flash conversion, it is capable of extremely high precision. However, this comes at the price of a reduced speed.

For this project, 14 data streams will theoretically need to be sampled at at least 600 Hz, giving a theoretical minimum throughput of 8.4 ksps. However, preliminary evaluations of the signal processing implementations using Matlab suggest that a sampling rate of up to 6.5kHz should be available, giving a maximum practically needed throughput of 91 ksps. Since the signals will have to be compared to determine their relative phase angles, any skewing introduced by asynchronously sampling 14 channels should be minimal. At 60Hz, a mere 46.3 us of delay constitutes a 1-degree phase angle error. If the channels are sampled sequentially, a 3.56 us acquisition time is needed to keep all signals within 1-degree of error. However, if the acquisition time can be made constant, then it can be manually accounted for. In addition to this low delay requirement, the final error in measured values should be less than 5%. Considering that there will be substantial challenges associated with high-precision frequency measurement required for FFT results, little of this 5% error should come from the ADC. As such, a sigma-delta ADC will be used if one can be found that meets all other requirements, however, an SAR ADC will likely have to be used.

Input Method: There are three types of common input methods for sending analog signals to ADCs, single-ended, fully differential, and pseudo-differential. A single-ended input compares all input signals to a common node, usually the analog ground. This is sufficient for most applications. A fully differential input takes both a positive and negative terminal for each input. This provides good 'common mode' noise rejection—any noise signal present on both the positive and negative inputs is canceled out when the difference between inputs is taken. A pseudo-differential input samples from the noninverting input with respect to its common ground but switches the input connection to the inverting input during the hold stage, effectively using it as a reference.

For this project, a professional-grade protective relay test-kit will ultimately be used to demonstrate PHATCAT's functionality. This will likely produce high-quality input signals. However, in a substation, there are many powerful electromagnetic fields that can cause substantial noise. As a result, fully differential outputs are desired for their common mode noise-rejection. Note that this will drive requirements on the hardware for transient protection and analog filters.

Input Range: ADC inputs can be either unipolar or bipolar. In other words, they are designed for range 0 to V_{cc} or range $-V_{cc}$ to V_{cc}. Since all input signals will be sinusoids with (ideally) no DC component, a bipolar input range is desired. A summing amplifier can be used to provide a DC offset, but it is desirable to avoid this extra component. Additionally, ADCs come in a wide variety of operating voltages. A higher

voltage range will decrease the signal-to-noise ratio (SNR) and thus reduce the impact of noise on accuracy. ±10V has been noted as a fairly common voltage that is larger than most others available. This gives a ratio of 3A/V for current measurement and 20V/V for the current and sense inputs, meaning that 50mV of noise will cause only 0.15A and 1V of measurement error (5%).

Output Interface: The process of communicating 14 separate data streams to the microcontroller has the potential to introduce difficulties in implementation and troubleshooting as well as delays. An SPI interface is preferred over an I2C interface due to the noise-immunity its level triggering provides. It will likely be simplest if the ADC supports fourteen individual SPI outputs.

Parts Selection: Several ADCs have been selected that are well-suited for meeting the outlined requirements.

Table 3.8. Analog-to-digital converters under consideration

Device	Analog - AD7616	TI - ADS8588S	Maxim Int. - MAX1270
Conversion Method	SAR	SAR	SAR
# of Bits	16	16	12
Input Method	Single-Ended	Single-Ended	Single-Ended
Input Range	±10V	±10V, ±5V	±10V
Output Interface	SPI, 16 outputs	SPI, 16 outputs	SPI, serial output
Est. Throughput	2 x 1 MSPS	200 ksps per channel, simultaneous	110ksps
Number of Channels	16	8	8
Additional Features	ESD, analog voltage clamp, 39kHz Butterworth (1^{st}),	ESD, analog voltage clamp, built-in PGA w/ auto range, 24kHz Butterworth (3^{rd})	Faulted input protection
Cost	$27	2 x $13	2 x $12.50

All chips utilize SAR as their ADC method, implying that they offer a balance between speed and accuracy. At ±10V, twelve bits of accuracy corresponds to a resolution of 2.4mV. Given that the signal will likely have more than 2.4mV of noise, we conclude that any listed ADC provides enough accuracy. Unfortunately, none of these chips support fully-differential inputs. These were found to be most common in sigma-delta ADCs designed for low-throughput, high resolution. However, given that the frequencies measured are relatively low and a low pass filter is being added, this is not an essential feature. The TI and Analog ADCs have a dedicated SPI-capable digital output for every channel, while the Maxim ADC only has a single output. The single output may add complexity and additional delay due to the time multiplexing. All three ADCs have sufficient throughput capabilities, but the TI offers the greatest overall throughput. Its

simultaneous sampling will prevent skewing, improving the accuracy of phase measurements. Of the three chips, the AD7616 is the only one that can support all fourteen channels on a single chip. For the others, two chips will have to be used.

Note that both the Texas Instruments and Analog Devices ADCs are specifically recommended for their application in protective relaying and the monitoring of power grids. The TI documentation details example applications which provide valuable insight into proper application of the ADC. Because this chip is specifically designed for measuring power system variables, the information contained in this documentation is invaluable to the authors. Of the three chips, the TI ADC has the most additional features beneficial to the project's goals. An internal Butterworth will further improve the SNR, and built-in overvoltage protections will supplement those already present in project. The built-in PGA automatically adjusts the input gain so as to maximize usage of the ADC's dynamic range, implementing the functionality desired for the project without any additional engineering. Due to its blend of high accuracy and performance, simultaneous sampling, and array of useful features, two Texas Instruments ADS8588S ADCs will be used for PHATCAT.

3.3.6 Direct Memory Access (DMA)

DMA allows a peripheral device to control the memory of the device without the intervention of the CPU (Fig. 3.27). This makes interrupts faster and can allow for faster data transmission between devices. Since PHATCAT will need to continuously process sampled data from fourteen analog channels, DMA can also limit the amount of time the CPU is being used and can limit the amount of power consumed by the device [3.13]. DMA may aid in preventing an excessive amount of CPU cycles from being spent on storing samples in memory. There are different ways that DMA can transfer data and those will be discussed below.

Block DMA: Block DMA was the first version of DMA that was used in early processors. In block DMA the processor does not have access to the memory bus until the process is complete. This could be useful in bringing large chunks of data and avoiding having to use the CPU as the middle man in the operation. The act of removing the processor from the memory bus may stall the CPU for long periods of time so this method is no longer used in current faster processors [3.14].

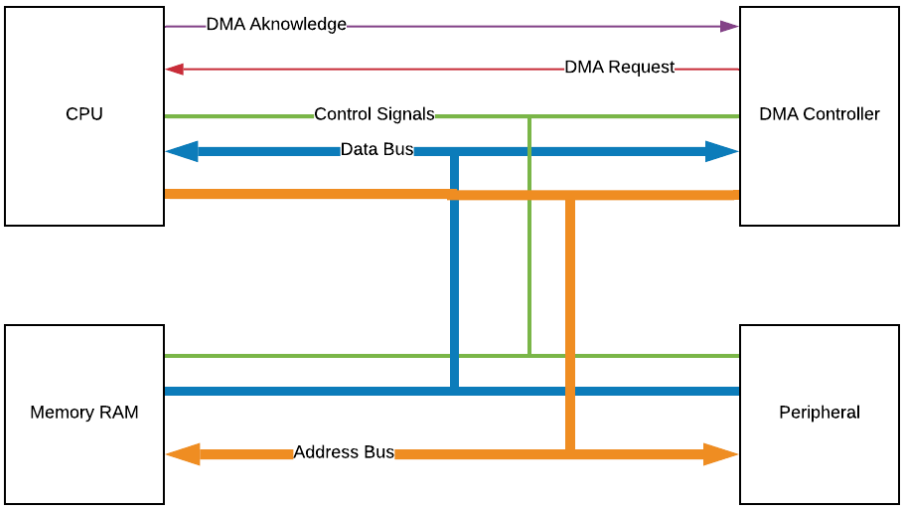


Fig 3.27. DMA Block Diagram by John DeFour

Burst DMA: In burst DM A the bus is only taken away from the processor in spurts where data is transferred and then control is returned to the CPU. This process runs over and over until the entire DMA process is complete. This can be used in conjunction with transparent DMA found below to optimize transfers when the CPU is doing other operations.

Transparent DMA: Is a smarter approach to DMA and it will monitor when the CPU is using the bus and will only take it away when the CPU is not actively using the memory bus. It is the slowest of all the DMA methods but does not impose and wait time on the CPU.

DMA Operations: All the methods of DMA transfer discussed above can be used to send data to different locations between the devices. These different locations of the transfer will be discussed as well.

Memory to Memory: In memory to memory transfers, the DMA will transfer data from one memory location to another memory location. This is very useful in transferring large data sets like in computer graphics. This is usually done with buffers in communications.

Memory to Peripheral: In memory to peripheral transfers the data from the memory into a peripheral. This application method is usually not used due to its niche use case.

Peripheral to Memory: Peripheral to memory transfers are usually used for peripherals that work with large blocks of data. This is commonly used in communication with cameras and SD card readers.

Peripheral to Peripheral: This mode of transfer is also very uncommon. Direct communication between peripherals is generally not a good idea because of the inability to check for errors. It is usually a better idea to use memory and CPU to make sure the data is not lost.

DMA in PHATCAT: DMA is a very useful tool to use in embedded applications to allow for faster run times. After into DMA and its uses. It has come to light that DMA performs best when large data sets are transferred between memory and peripherals. It can be very useful in these cases to limit the amount of time the CPU is bogged down by slow IO operations. However, in instances where the amount of data being transmitted is smaller than several kilobytes of data. It can slow down the whole process because the process of setting up the communication with the DMA may take longer than the CPU just handling everything directly [3.15]. Due to the smaller sizes of the data that will be transmitted between devices, it is unnecessary to use DMA to speed up the communication. It will be experimented with in testing of the device to see if any benefit is added by having DMA communication.

3.3.7 OUTPUT CONTACTS

In order to control external circuitry, the relay must have controllable output contacts. To implement controllable contacts into the relay, two circuits are needed, a primary circuit and a secondary circuit. The primary circuit is directly connected to a GPIO pin of the development board in the relay and is designed in such a way to supply a large enough voltage and current to the coil associated with the output contacts to actuate and close them. The secondary circuit is connected in series with the normally open contacts. The normally open contacts create a normally open circuit for the secondary circuit and therefore the secondary circuit is controlled by the primary circuit which is controlled by the status of the GPIO pin on the development board of the relay. The controllable output contacts are needed to deploy specific protection logic that is programmed within the relay. A typical output contact would be actuated in a power protection scheme to open a specific breaker in a substation in order to isolate or clear a fault to protect major equipment and assets associated with the Bulk Electric System (BES). Two types of contact devices were considered for implementation into the relay circuitry, Solid State Relays and Electromechanical Relays.

Solid-state Relays: Solid State Relays (SSR, Fig. 3.28) are purely electrically switching devices and do not have any physical contacts or moving parts. The SSR completely isolates the input from the output using an ‘opto-coupler’ which is a type of light sensor. Also referred to as an ‘opto-isolator’, it consists of an input infrared LED and a photo sensitive device that reads the infrared beam intensity at the same level as the electrical input signal and therefore switches “ON” the output circuit. There are many photo sensitive devices that can be used to read the infrared light beam from the LED such as: single photo-diode, photo-transistor, photo-resistor, photo-SCR, or a photo-Triac. The output switching device that is generally used for DC is a transistor and for AC is a Triac/Thyristor combo. A RC Snubber Circuit is required across the output in order to compensate for any noise or voltage transients, although most SSR Relays include the circuit with the device. [3.16]

The Electromechanical Relay (Fig. 3.29) is one of the most widely used relays in the market today. Electromechanical Relays (EMR) are switching devices that open and close contacts using magnetic induction and mechanical moving parts that are activated by an electrical control signal. Some of the components used in the relays are contacts, coils and an iron core with an armature and a yoke. The EMR's coil is wrapped around the iron core and a small electrical signal passes a current through the coil generating a magnetic field. The magnetic flux is converted into a force that is applied to the armature which closes or opens the contacts and completes the output circuit. A spring is typically used between the yoke and armature in order to reset the relay when the circuit has been turned "OFF". A RC Snubber Circuit is also required and has to be added in order to prevent arcing across the contacts. The SSR initially was highly considered for our project due to its many benefits. The SSR has an increased life span, high reliability, almost immediate response time and very little electromagnetic interference with the signal since there are no generated magnetic fields or physical contacts that can create arcs during contact separation. Also, the input control signal is generally low enough to directly interface it with most integrated circuits.

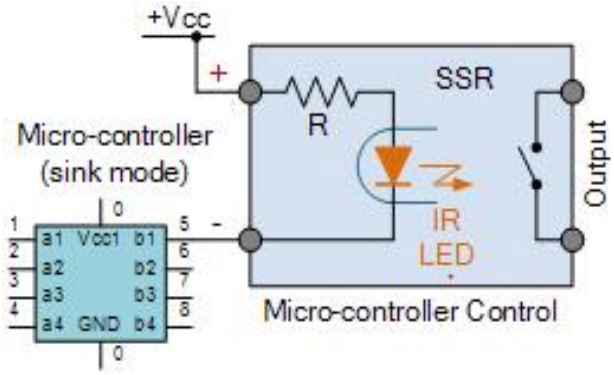


Fig. 3.28. Solid-State relay. Reproduction permission requested from www.electronics-tutorials.ws

When considering the EMR, the magnetic mechanical device operates slower than the SSR due to its moving parts and having to generate a magnetic field. The mechanical parts, especially the contacts, wear out through constant movement and arcing that shorten the life span of the relay. Also, there is large back electromagnetic force that happens when the circuit is turned "OFF" and the magnetic flux collapses in the coil of the relay. The induced reverse voltage may be higher than the switching voltage and could damage other devices connected to the relay circuit.

The SSR sounds like a steal so far doesn't it? Sadly, we ended up having to choose the EMR for our project due to the voltage drop of 1.6V-2V that happens when the SSR is turned "ON". The industry's common practice is to wire multiple contacts in series for a power control circuit to create an "AND" logic for programming and control purposes. For example, wiring three SSR's in series would cause a voltage drop of 4.8V-6V. This could drastically reduce the magnitude of our signal, even though within our project there will not be any contacts wired in series, it is important for us to stay as close to industry standards or practice as possible.

Types of Electromechanical Relays:
There is a large variety of EMR relays in production today with a wide range of voltages, currents and power ratings. For our project, the EMR should be able to carry 5A nominal, break 10A of current, and isolate 200V of potential difference when the contacts open. Three different types of relays were considered for our project: The

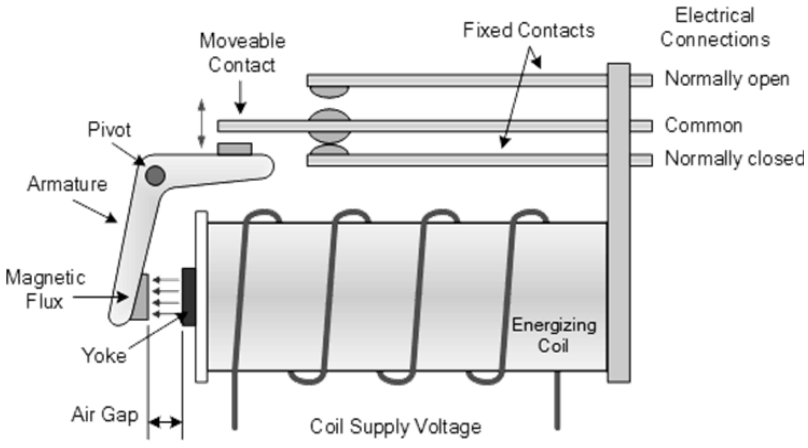


Fig. 3.29. Electromechanical Relay. Reproduction permission requested from www.electronics-tutorials.ws

Multimode Relay, IM Relay and Miniature Signal Relay.

Table 3.9. Electromechanical Relays Considered

Part Number	IM Relay IM06GR	Multimode Relay MT331110	Miniature Signal Relay EE2-12NU
Manufacturer	Potter & Brumfield	Potter & Brumfield	Kemet
Termination Style	Gull Wing	Plug-in, 11 Pin (Octal)	Gull Wing
Contact Arrangement	DPDT	TPDT	DPDT
Contact Form	2 form C, 2 (CO)	3 form C, 2 (CO)	2 form C, 2 (CO)
Contact Rated Voltage	220 VDC	240VAC	220 VDC
Contact Rated Current	2A	10A	2A
Switching Capacity	125VDC ≈ 0.5A	110VDC ≈ 10A	125VDC ≈ 0.48A
Operate Time	3ms	15ms	2ms
Release Time	5ms	10ms	1ms
Bounce Time	3-5ms	4/10ms	Not Specified, typ. 3-5ms
Coil Rated Voltage	12VDC	110VDC	5VDC
Coil Operate Voltage	9.6VDC	82.5VDC	3.75VDC
Coil Resistance	1.315kΩ	10kΩ	178kΩ
Rated Coil Power	140mW	1.2W	140mW
Cost	$2.33	$20.88	$1.90

Multimode Relay MT331110: The Multimode Relay was initially considered due to the fact that the device met all of our initially estimated specifications. The contact ratings were good for a potential difference of 240VAC and 10A of current. The device is capable of breaking a load current of 10A at about 110 VDC by wiring the three contacts in series. The relay incorporated different types of sockets to 'plug' into with different types of mounting applications which would help for a PCB mount to not damage the relay during the soldering process since you would be soldering the socket to the board and not the relay itself. However, the Multimode Relay could not be a part of our design due to its slow operating time.

One of the most important factors for protecting equipment is speed. How fast you are capable of detecting a fault and tripping a breaker or multiple breakers to isolate a fault is imperative for minimizing damage to the system and equipment. The operating speed for the Multimode Relay is 15ms. This happens to be an average speed for all relays with the same rating and cost. This operating time is pretty slow when comparing it to the contacts of a relay used widely in the industry for transformer protection, the SEL-487E with an operating time of 6ms. Now, considering relays with a smaller breaking capacity, we noticed a

decrease in the operating time of the relay. Therefore, in order to obtain a faster operating time while staying within the budget, the breaking capacity of the relay would have to suffer.

IM Relay (IMR): The IM Relay and Miniature Signal Relay were found with a decrease in operating time, breaking capacity and cost compared to the Multimode Relay. The IM Relay has an operating time of 3ms which is 12ms faster than the previous relay. The breaking capacity of the relay when considering the high current model is capable of breaking 5A up to 24VDC or 0.48A at 220 VDC where the previous relay was capable of breaking about 10A at 110VDC or 0.75A at 300 VDC. The IM Relay shall be capable of breaking a current of 5A with a nominal voltage of 12VDC. The cost of the IM Relay is $2.33 per unit which is about $18.55 less than the Multimode Relay. Therefore, the gain is relay that is 12ms faster at operating and is priced at $18.55 less, but the loss is the breaking capability of 5A less with a lower nominal voltage 12V, which in reality is a good thing in one sense, since the power dissipated will be a lot less.

Miniature Signal Relay (MSR): The Miniature Signal Relay is the relay that has been chosen to be incorporated into the design of our project. The reason for this selection is due to the fact that the MSR is 1ms faster than the IMR and is $0.43 cheaper too. The documentation in regard to the specifications by the manufacturer, Kemel, is very thorough and neat. The loss is that the contact switching capability and nominal current is 2A instead of 5A.

Relay Characteristics: The specific model of the MSR will be from the EE2 Series which has certain characteristics that make it ideal for many different applications. These characteristics include switching type, contact form, contact arrangement, and termination style. The most common characteristics of relays/switches will be identified and discussed while highlighting the specific attributes of the relay chosen for our design in the next few sections.

Switching Type: A typical switch in a circuit has two positions, the ‘ON’ position producing a closed circuit that allows current to flow or the ‘OFF’ position producing an open circuit, cutting off the flow of current. However, there are different types of switches. The most common type of switch perhaps is the switches found in our homes or at work that we use every day known as ‘toggle’ switches or sometimes ‘décor’ switches depending on the style. The toggle switch remains in its current position until actuated. Once actuated the switch will change from the ‘ON’ position to the ‘OFF’ position or vice versa. Therefore, the behavior of such a switch is a ‘latching type’, where the switch remains in its position until actuated. Another common type of switch is known as a momentary switch. A typical momentary switch only switches ‘ON’ when being actuated and immediately switches ‘OFF’ when actuation stops. A good example of this would be a button you would push on your gaming console controller. [3.17] The behavior of the momentary switch would be a ‘non-latching type’. This behavior identifies with the chosen MSR relay model where the relay contacts will only be switched when the coil is actuated or energized identifying our relay as a ‘non-latching type’.

Contact Form: There are three different types of contact forms found in switching devices, these include Form A, Form B, and Form C. These ‘Forms’ identify a switch’s contact position. Contact Form A is when the switch’s contacts normal position is ‘normally open’ (NO). Contact Form B is when a switch’s contacts normal position is ‘normally closed’ (NC). Finally, Form C is when a switch has both types of contacts and when actuated the switch will ‘changeover’ from normally closed contacts to normally open contacts and the normally open contacts to normally closed contacts. Contact Form C is the Form of contacts that are present within the chosen MSR relay model.

Contact Arrangement: There are many different types of contact arrangements, the three most common arrangements seen in most switching devices are Single Pole Single Throw (SPST), Single Pole Double Throw (SPDT), and Double Pole Double Throw (DPDT). The number of poles identify the number of circuits and the number of throws identify the number of terminals the circuit can be switched between. Therefore, the SPST contact arrangement has a single circuit that can be switched to one terminal, where the SPDT has two terminals. The DPDT contact arrangement has two circuits that can be switch simultaneously between two terminals. The contact arrangement of the chosen MSR relay model is the

DPDT arrangement which is unnecessary for our particular application where only one circuit is required to be switched to one terminal. However, the DPDT contact arrangement is equivalent to two SPST contact arrangements. Therefore, only one set of the contacts will be used for our application, so the DPDT contact arrangement is overkill, but can still accomplish the particular tasks needed for the design.

Termination Style: The termination style is specifically how the switching device will be connected to the circuit. Since the relay output circuits will be designed on a PCB, the two termination styles for a PCB application is a through-hole mount or a surface mount. The through-hole relay termination type will be used in order to easily connect to a breadboard for testing purposes and the surface mount will be used in order to be incorporated into our PCB circuit design.

3.3.8 SENSE INPUTS

The PHATCAT Relay shall have 3-rear control inputs for detecting 125VDC nominal active high signal. The 125VDC signal will be connected to a series resistor to lower the potential to an appropriate level to supply the rest of the circuit. The circuit is then split to two different resistors with one connected to ground and another connected to an opto-coupler transistor photo sensitive device. The current divider is used to allow approximately 10mA of current to flow through the infrared LED side of the optocoupler. The LED illuminates the photosensitive transistor and the current is transferred with a specific current transfer ratio of about 75% between the collector current of the transistor and the forward current of the LED. The collector of the transistor will be directly connected to the development board outputting a high of 3.3V. Another General-Purpose Input Output (GPIO) pin of the development board will be reading in the status of the emitter voltage. For a GPIO pin, just because there is nothing connected to the pin does not necessarily mean that the pin is reading 'low'. The emitter end of the transistor will be connected using a pull-down resistor to ground. The pull-up or pull-down resistors are used to ensure that the GPIO pins are reading what they are intended to read whether 'high' or 'low'. When the photo sensitive transistor is operating in cutoff mode, the transistor will behave like an open circuit. For a pull-down resistor, the GPIO pin is connected to the emitter side of the transistor which has been grounded out by the open circuit, thus reading 'low'. When the transistor is no longer open and operating either in forward active mode or saturation mode, the resistor will pull-down the voltage of 3.3V to be seen at the GPIO pin connection, thus reading 'high'. Therefore, 125VDC signal will be will be safely read and input into development board GPIO in order to operate specific protection logic. Typically, sense inputs are used for monitoring the status of specific equipment within the substation. For example, if the status of a breaker in the substation yard changed from closed to open, the relay would receive a 125VDC input signal from that breaker.

3.3.9 LED INDICATORS

The PHATCAT Relay shall have a total of fourteen LED indicators located on the front panel of the relay. The LED's will be used to indicate when different tasks associated with the built-in logic of the relay have been performed.

- Four of the LED's will be used specifically to indicate the phasing of a detected fault. To accomplish this, the LED outputs will be associated with G (Ground), A (A Phase), B (B Phase), and C (C Phase) for the 3-Phase Power System. For example, if a phase to ground fault occurs, then the LED's associated with the ground (G) and the particular phase (A, B, or C) the fault occurred on will be illuminated indicating the type of fault.
- One LED shall be used to indicate that the relay is powered on. When the toggle power switch has been turned on, the LED associated with power indication will be turned on as well.
- Five LED's shall be used to identify protection functions (instantaneous overcurrent, time-inverse overcurrent, current differential, overexcitation, and harmonic blocking) will be used during

specific scenarios in order to protect the transformer. To see more details on the different protective functions and the logic that drives them, please refer to sections (3.1.4 - 3.1.7).

- Four LED's shall be programmable by the user for specific functions that will be determined by the power system layout and location of where the relay will be incorporated to protect the asset.

Communication of Led Drivers: The communication protocol for the device requires serial input interfacing and parallel output interfacing. Parallel interfacing allows multiple bits of information to be sent at the same time which increases the speed of transferring the data. One of the big perks of the LED driver is the reduction in the number of GPIO pins required from the microcontroller to control the LEDs and an increase in outputs data through parallel interfacing. Therefore, multiple LEDs can be controlled with a minimal amount of inputs. This is accomplished through serial communication with a single data input pin for transferring one bit at a time, starting with the most significant bit first. The MAX6979 LED driver is composed of a 4-wire serial interface and the TLC6C598-Q1 LED driver is a 5-wire serial interface device.

Shift Registers and Clocks: The LED Driver shifts in data using shift registers and latches them in parallel shift registers saving the data that was input using D-Latch Registers. The data is shifted in usually on the rising edge of the clock signal. The MAX6979 LED driver uses one clock signal to shift in the data and latch it in the parallel shift registers, where the TLC6C598-Q1 LED driver uses two clock signals. A serial clock signal to shift in the data and a register clock signal to store the data. Typically, an output pin is enabled in order to send the saved data to the output using parallel interfacing. The MAX6979 single device has 16 outputs, where the TLC6C598-Q1 single device only has 8 outputs.

MOSFETs: MOSFET stands for Metal Oxide Semiconductor Field Effective Transistor. The MOSFET is made up of 3 different leads; the Gate, the Drain and the Source (Fig. 3.30). The gate is separated from both the drain and the source by a thin insulating material. The MOSFET alters the flow of charge carriers through the drain to source channel using an electric field that is generated by an applied voltage at the gate. Therefore, the device acts like an open circuit until the gate potential is overcome with a large enough voltage. When the gate potential is overcome, and the gate voltage is larger than the voltage across the drain and source, then the device is operating out of the saturation region. When the MOSFET operates out of the saturation region, this means that the device is in constant current mode which is utilized in the LED drivers. Constant current is important, since a LEDs brightness is determined by it. The very characteristics of an LED show that very little voltage can dramatically change the amount of current that is seen, which is the most important reason for the current regulation or need for constant current. [3.18]

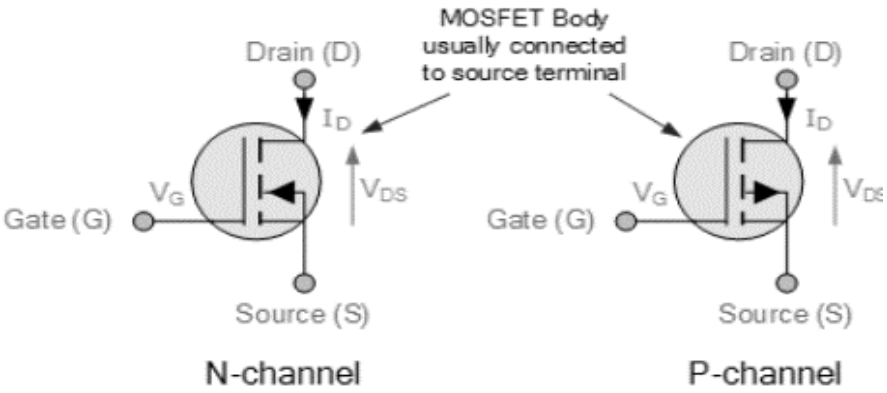


Fig. 3.30. N-channel and p-channel MOSFETs. Reproduction permission requested from www.electronics-tutorials.ws

Open Drain Outputs with Constant Current Sinking: The data latched and stored in the parallel registers can be sent to the output which is output with constant current sinking using MOSFETs with a maximum value of current set by a resistor or resistors. Current sinking means that the current is flowing into the device versus current sourcing which means the device is supplying current through the output. The current is constant due to the fact that the MOSFET is operating in saturation mode which produces a constant

current. Open Drain means that the Drain is left open but connected to an external pin and the Source is connected to ground, thus sinking the current through the open Drain. The MAX6979 LED driver is capable of allowing a max sinking current of 60mA and an output voltage of 5.5V. The MAX6979 model uses a single external resistor for constant current sinking, where the TLC6C598 model needs an external resistor with each LED circuit. The TLC6C598-Q1 LED driver is capable of a max sinking current of 50mA and an output voltage of 40V.

Table 3.10: LED Driver Comparison

Product	**MAX6979**	**TLC6C598-Q1**
Manufacturer	MAXIM	TEXAS INSTRUMENTS
Number of Outputs	16	8
Serial Interface Inputs	4	5
Logic Supply Voltage	-0.3V to +6V	-0.3V to 8V
Logic Input Voltage Range	-0.3V to +6V	-0.3V to 8V
V_{ds} Voltage Range	-0.3V to 6.3V	-0.3V to 40V
R_{set}	360ohms	N/A
OUT Sink Current	60mA	50mA
Continuous Power Dissipation	1067mW	Not Specified
Operating Temperature Range	-40C to +125C	-40C to +125C
Cost	$8.00	$1.01

The two LED driver devices accomplish the same thing but are relatively different. The advantages of the Maxim LED driver are the fact that the single device has 16 outputs, only requires a single external resistor for sinking the currents at the output, only uses a single clock to read in data and has only 4-serial data inputs. The TLC6C598-Q1 LED driver has only 8 outputs for a single device and would have to connect a second device in series to get the total number of 14 outputs that is needed for LEDs. The TLC6C598-Q1 model requires a resistor per LED circuit, 5-serial data inputs and 2 clocks to shift data in and store it. Therefore, the MAX6979 LED driver will be incorporated into the design to drive the LEDs of the relay.

3.3.10 Push Buttons and Power Switch

The PHATCAT Relay will have a total of six user programmable pushbuttons or switches and one power pushbutton or switch that will be located on the front panel of the relay. The difference between a switch and a pushbutton is that a switch changes between the ‘ON’ and ‘OFF’ state when actuated where a typical pushbutton changes state only while actuated. However, there are pushbuttons that do ‘latch’ to the next state and therefore switch from the ‘OFF’ to the ‘ON’ state or vice versa. Considering the features of switches and pushbuttons, the power switch will be a toggle switch with a protective cover to prevent accidental shutdown of the device. The toggle switch will be used to completely de-energize the relay. In order to shut down the relay safely without damaging any software or hardware components, the power

switch shall be programmed through the microcontroller to “Power Down”. The six user programmable pushbuttons or switches shall be momentary pushbuttons, a non-latching type is needed to send an impulse signal to the microcontroller and perform in a single occurrence the specific function that the user programmed. The difference between switching types is discussed in more detail in section 3.3.7. The momentary push buttons shall be protected by a cover or guard to prevent accidental switching and meet the two-factor safety requirement for operating a specific relay function.

There are three different types of toggle switches considered to be used as the power disconnect for the relay. Considering table 3.11 below, the first toggle switch considered was the MS2011SS1W01/UC by the manufacturer NKK Switches. The voltage and current ratings are sufficient for the following application and the price of $3.37 is a decent, low price for a power switch. However, the diameter size is about 6.50mm which is only about a quarter inch. For a power switch, a quarter inch diameter is just too small for a power switch on the front panel of the relay. The next switch considered is the C3900BA by the manufacturer Bulkin**.** The following switch has better voltage and current ratings than the MS2011SS1W01/UC and is about half an inch in diameter which is a more standard size for a front panel switch. The price difference is about $1.69 more for the new switch. The last switch considered is a S1A by the manufacturer NKK Switches. The S1A a slightly lower voltage rating than the C3900BA model switch from 36V to 30V, but the current rating is higher from 14A to 20A. Either way the ratings again are sufficient for the relay application since it won’t be a direct power disconnect but will be programmed through the microcontroller to power the device on and off safely. The S1A is also a half inch in diameter and the cost is $0.69 cheaper. Plus, the termination type is solder lugs which a much sure connection compared to quick connect lugs. Therefore, the S1A by NKK Switches shall be used as the power switch to safely shut down the relay.

Table 3.11. Power Toggle Switch Comparison Table

Product	**MS2011SS1W01/UC**	**C3900BA**	**S1A**
Manufacturer	NKK Switches	Bulkin	NKK Switches
Voltage Rating-DC	30V	36V	30V
Current Rating-DC	4A	14A	20A
Actuator Type	Standard Round	Standard Round	Standard Round
Actuator Length	10.5mm	17.50mm	17.50mm
Termination Style	Solder Lug	Quick Connect 0.25” (6.3mm)	Solder Lug
Mounting Type	Panel Mount	Panel Mount	Panel Mount
Panel Cutout Dimensions	6.50mm (Diameter)	12.70mm (Diameter)	12.50mm (Diameter)
Cost	$3.37	$5.06	$4.37

The six other switches shall be momentary push buttons with an LED ring around the center of the push button that will constantly be in the energized state. The momentary push buttons will be used to send a 3.3V impulse signal across a resistor to an opto-coupler device. The opto-coupler transistor photo sensitive device will be designed to draw enough current to “turn on”. The emitter of the transistor will be directly

connected with a pull-down resistor to the microcontroller reading a high of 3.3V. The collector end of the transistor will be connected to ground. When the photo sensitive transistor "turns on", the General-Purpose Input Output (GPIO) of the microcontroller will be connected directly to ground and go from reading a HIGH (3.3V) to reading a LOW (0V), thus being "pulled down". Therefore, when the logic level goes "LOW" or is "pulled-down" the microcontroller will be enabled to execute specific logic that will be programmed by the user. For example, a push button could be used to open or close a breaker in the substation yard to isolate a section of bus for maintenance purposes or in case of an emergency.

Three different types of momentary push button switches were considered for our relay. The first switch considered was the Ulincos Momentary Push Button Switch (U16B1SW). Initially, the appearance of the switch with the LED Ring at the center and the option to keep the LED "ON" even when the push button was not being pressed, caught our attention as to add a nice cosmetic feature. This specific push button created more of a desire to have appearance in mind as major components are chosen for the relay project.

The next switch to be considered was the TE Connectivity Momentary Push Button (AV1610R112R04). The ratings for the switches were the same, the only thing that was different from the first switch, is the cost being approximately two dollars more and the termination type being soldering lugs instead of screw terminals. Also, the documentation that the push button had to offer was very thorough.

The last switch considered was the E-Switch Momentary Push Button Switch (PV6F240SS-341). This switch has even better documentation with the price difference of $.50 more than the TE Connectivity Alco-Switch, and a higher voltage rating of 48V instead of 36V. The other rating considered for all of the switches are practically identical, therefore the decision will be based primarily on the cost of the product and documentation availability. The TE Connectivity Alco-Switch has good documentation and is priced at $11.75, where the Ulincos Switch cost is less at $8.89, but there is little to no documentation for the device. The E-Switch device cost $0.50 more with better documentation and a higher voltage rating. However, the documentation provided for the TE Connectivity Alco-Switch is sufficient enough for our application. The voltage rating for our application will not be an issue either, so a voltage rating of 36V is good. Therefore, the TE Connectivity Momentary Push Button (AV1610R112R04) will be incorporated into the relay design as our programmable push buttons to execute specific tasks determined by the user for a specific application. Table 3.12 is referenced below in regard to the decision-making process.

Table 3.12 Momentary Push Button Comparison

Product	**PV6F240SSG-301**	**U16B1SW**	**AV1610R112R04**
Manufacturer	E-Switch	Ulincos	TE Connectivity
Rated Voltage	48V	36V	36V
Rated Current	2A	2A	2A
Contact Resistance	50m-Ohm	----------	50m-Ohm
Termination Type	Solder	Screw	Solder
Packaging	Tubing	----------	Tray
Cost	$12.25	$8.89	$11.75

3.3.11 DISPLAY

The display to be housed in the front panel is a key feature of the project. The display will be user-facing, making it very important that the display is clear and easy to read. The display will enable the user to visualize the phase angles of the transformers output. Which can be analyzed to make sure the transformer is in normal operation or experiencing a fault. Important features of the display will be examined below before selecting a product that best fits the project's needs.

Graphics: There are two types of displays that can be used in embedded systems. The character and numeric only display that can display a set amount of character on screen and nothing else. These displays are usually monochromatic and will have segments that can be turned on or off to show characters and numbers as needed. These require much less power electrically and computationally to operate. Making them ideal for portable battery powered devices. There are then the more advanced screens that have a resolution and behave like small monitors. They operate by activating pixels the screen that can be used to display a range of colors. Making it possible to display video and animations as well as more advanced graphics on the screen. These displays require much more power electrically and computationally to operate and special connections to connect to the microcontroller. Making these displays better for always plugged in devices that want to display a wide arrange of graphics to the viewer.

Manufacturer: Buying from a well-known, reliable manufacturer is important. Such a manufacturer simplifies troubleshooting by offering good documentation and customer service. The manufacturer may also have sample code to help integrate the display with the microcontroller.

Characters: The amount of characters that the screen can display is important. So, it's possible to display all of the data required for our device. Usually the format is characters per line x number of lines. Meaning a 16x4 would have four lines of sixteen characters possible displayed on the device. The device will be displaying a lot of characters due to the many phasors we will be displaying. Making this a very important part of our display.

Pins: One of our biggest concerns when using the display is how many pins it would take to use. Seeing as we require several IO pins for the three channel currents and voltages. It is necessary to limit the amount of pin real estate that our display would be taking up. Because we will have so many other inputs and outputs that will be using the pins on the microcontroller. The character display requires the pins to controls the segments of the display either on or off. Also, LCD displays require two extra pins to power the backlighting of the device. This is not required for OLED screens.

Interface: More advanced displays require different connections than simple pins on the IO of the microcontroller. The most common connections are the Serial Peripheral Interface (SPI), Universal Asynchronous Reception (UART), and Inter-Integrated Circuit (I^2C) for microcontroller's interactions. These communication methods will be explained later in the paper in Section 3.3.13. Displays can also be connected with USB, HDMI and Display Port in some instances but is generally very difficult to do without an Operating System (OS) found in some devices like the raspberry pi. This is due to the fact that the developer must write their own graphics drivers or purchase a device with a standalone display controller device.

Display Type: Displays come in many shapes and sizes. There are general character LCD that can come in three different formats: FSTN, STN, and TN. TN stands for Twisted Nematic and is the cheapest option, having lower contrast and fewer colors available. The refresh rate is the fastest of the three. Super Twisted Nematic has more contrast and a slower refresh rate. Finally, Film compensated Super Twisted Nematic has the best contrast and most colors but the worst refresh rate of all. (focuslcs). The more advanced graphical displays can also come in several flavors from LCD to OLED. LCD screens generally use TFT (thin film transistor) to display. OLED (organic light emitting diode) require less energy and has a better contrast and more vibrant picture.

Size/Visibility: Displays can vary vastly when it comes to size. For the sake of the project the display should be large enough to be easily visible on the front panel. We would like to have a display that is 8 inches diagonally. Which is the same way TVs are measured. The reason for this is that it is big enough so that the characters can be visible on the screen from a few feet away. Also, if it was much larger it would take up to much room on the front panel. Which is going to fit into a 19-inch server rack. Displays also have a different number of segments for the characters being represented on the display. The more segments used for characters the clearer the picture will appear to the viewer. However, as stated above the more segments in the display the more pin connections necessary to control them. The standard is the 7-segment display that we have all seen on digital watches and in labs.

Touch: Many of the higher end screens have capacitive touch capabilities pre-installed on them. For the device the ability to have touch screen interaction is not required. It could be used in a stretch goal for our project.

Table 3.13 compares several display options that were considered.

Table 3.13 Display options considered

Device	NHD-0440WH-ATMI-JT#-ND	NHD-0440WH-ATFH-JT#-ND	NHD-7.0-HDMI-N-RSXN-ND
Manufacturer	Newhaven Display Intl	Newhaven Display Intl	Newhaven Display Intl
Characters*	40x4	40x4	800 x 400 pixels
Backlit	Yes (White)	Yes (White)	Yes (White)
Dimensions*	190 x 54 x 13.6 mm	190 x 54 x 13.6 mm	165 x 104 x 16.5 mm
Character Format	5 x 8 dots	5 x 8 dots	N/A
Power VDD	4.75 ~ 5.25 V	4.75 ~ 5.25 V	4.75 ~ 5.25 V
Interface	Parallel	Parallel	HDMI
Cost	$24.90	$25.20	$93.00
Pins Necessary*	18	18	N/A
Display Type	LCD	LCD	LCD
Graphics	No	No	Yes
Touch	No	No	No
Type	STN	FSTN	TFT

These are not the only displays that were considered. Other devices such as OLED screens with advanced graphics capabilities were also explored, with touch capabilities. As well as E-INK displays which can be used for very low power devices. However, due to the much higher cost of such displays and their difficultly to integrate into the design. They have been excluded.

The **NHD-0440WH-ATFH-JT#-ND** is a character and numeric only display that is a decent size and has enhanced contrast and viewing due to FSTN. Making the cost considerably lower than the more advanced graphics displays. For the characters, we need and the budget we have all of the displays will require 18 pins. Making us unable to use less than 18 pins for a simple to use character display. This display will fit our needs.

3.3.12 MICROCONTROLLER

The microcontroller is the heart of the device. The project's subsystems and oriented around representing real-world data in a format acceptable for digital computation via the microcontroller. There are many factors to be considered when choosing a microcontroller. Many of the factors driving this project relate to the microcontroller's I/O and signal processing capabilities. The factors considered in this design will be explained one-by-one, then the primarily considered options and final choice will be presented.

Clock Speed + Program Memory: Estimating the needed clock speed and program memory for a given project can be very difficult. There is no one-size-fits-all empirical method, and experience is needed to make accurate estimations. Guesses made by the authors are unlikely to be accurate. As such, the microcontroller selected will likely be far more powerful than is ultimately necessary. However, the consequences of underestimating these basic needs can be catastrophic when working under the time constraints presented by Senior Design. Mitigating this risk is more important than the cost-savings associated with a less powerful device. In a real-world design process, the prototype can be used to estimate the computational burden presented by the features, and a similar, but less-powerful microcontroller can be used in the second iteration. Still, despite this initial uncertainty, other aspects of the microcontroller can be spoken about with more certainty

Word Size: Every microcontroller is designed to operate on a certain number of bits for both data and instructions. This number is known as the 'word size'. Generally, microcontrollers with larger word sizes are more complicated but more powerful as a result. The ADC chosen for PHATCAT produces a 16-bit, two's compliment number. The chosen microcontroller should then support at least a 16-bit word size. Otherwise, it will either be difficult to manipulate the 16-bit values or resolution will be lost.

Internal ADC Capabilities: In the ADC selection section, several important characteristics of the ADC methods have been discussed. Authors had difficulty finding microcontrollers with on-board ADCs capable of meeting the project's demands. Thus, no on-board ADC will be performed, instead the values will be streamed in from the ADC.

Direct Memory Access (DMA) Functionality: Since the device is designed to perform real-time evaluations of the power system's state, latency in servicing interrupts should be minimized. The ADC will be constantly measuring values and supplying them to the microcontroller via communications. DMA allows for peripherals to store their inputs directly into the microcontroller's memory, without the need for an interrupt. This will decrease the performance impact of having many real-time functions running alongside all of the input updating and signal sampling. This is an important feature as it improves PHATCAT's speed, which is one of its most crucial characteristics.

I/O: Many inputs and outputs are required for this design. Table 3.14 tabulates the estimated needs based on the hardware chosen in the previous sections. Multiple functions are often multiplexed into the same pin, and schematics are not yet developed. The GPIO pins may end up being needed to perform another function or additional unforeseen connections may be needed. As such, there should be some overhead on the chosen microcontroller.

Table 3.14. Estimate input and output needs for microcontroller

Function	Main Component	Pin Needs	Pin Purposes
ADC	(x2) ADS8588S	2 x 32 GPIO	Parallel Interface (16 data, 3 control), Configuration (13)
Output Contacts	(x3) EE2-12NU	3 x 1 GPO	Enable optocoupler
Sense Inputs	(x3) TBD	3 x 1 GPI	Read optocoupler output
LED Indicators	MAX6979	4	Serial Interface
Push Buttons	(x6) AV1610R112R04	6 x 1 GPI	Read High/Low
Power Button	S1A	1 GPI	Read High/Low
Display	NHD-0440WH-ATFH-JT#-ND	12 x 1 GPIO	Parallel Interface (8 data, 2 control), Chip Enable (2)
Total:	**93 Pins**		

A majority of the pin requirements come from the ADC. This is a byproduct of its 16-bit parallel interface and the multiple configurable functionalities, as well as the fact that two are needed to support the project's 14 analog signals. In reality, many of the configuration pins will either be constant (and thus can be tied to V_{cc} or ground) or common between the two chips (in which case one pin can be used to control both). The ADC supports a two-wire serial connection, but the project's demands for high synchronism between channels make a parallel interface preferable.

Memory: Aside from the memory needed to store the microcontroller's program, there will be two main memory needs worth estimating beforehand. One is the storage of the samples from the ADC and the other is the storage of the user-defined settings. Additional memory will be needed for the storage of variables, so a good amount of overhead should be left over once these needs are conservatively considered. Based on the signal processing methods chosen and ADC configuration options available, the memory needs for holding the sampled values are as follows: At a preliminary sampling rate of 6.25 kHz for 22.22ms, fourteen channels of the ADC will produce 1,946 16-bit numbers, requiring 3.892 kilobytes of volatile memory. These needs are then fairly minimal and are unlikely to constrain the design.

The user-settings needs can be estimated based on the number of settings and the length of the string or float required to hold them. These will need to be stored in non-volatile memory. They are estimated in table 3.15. These needs total to a mere 3.684 kilobytes. Once again, we see that the memory needs for this project are very minimal. This would not be the case if we needed to store many settings presets or high-resolution event data. Nearly any microcontroller capable of satisfying our other requirements will satisfy our memory needs.

Floating-Point Functionality: The various signal processing functions will require large amounts of floating-point operations to be conducted. Lots of scaling (multiplication) will have to be done. Various operating quantities and mathematical functions will have to be evaluated for every measured window. The most computationally burdensome of these tasks is likely to be the magnitude and phase calculations for the phasor representations. These require both square roots and inverse tangent functions. These functions will have to be performed frequently and rapidly. It is of great benefit if the microcontroller has a unit

dedicated to these sorts of calculations. Otherwise, there is a possibility that more advanced numerical methods will be required to achieve the necessary speed.

Table 3.15. Memory needed for storing user-settings

Type of Setting	Types of Needed Data	Needed Space
Push Button, LED, Output Contact, and Sense Input Logic Equations	Strings of up to 128 characters each.	16 x 128 bytes
Protection Logic Equations and Setpoints	Strings of up to 128 characters each, Floating Point Values	2 x 128 bytes, 40 x 2 bytes
Power System / Equipment Data	Strings of up to 128 characters each, Floating Point Values	10 x 128 bytes, 10 x 2 bytes

Development Board Availability: While the final prototype will need to feature an author-designed PCB using the microcontroller, a development board will be needed for both software development and testing of subsystem integration. Since breaking-out a microcontroller manually is a difficult and time-consuming process, it is preferable if an affordable development board that provides the needed capabilities can be obtained.

Communications Capability: The microcontroller must be capable of interfacing with a desktop PC via a USB connection for programming and end-user configuration via the application. If USB is not supported, UART is required and an adapter cable can be used. I2C and SPI protocols should be required to allow interfacing with any external ICs.

Debugging Capability: Not all microcontrollers have the ability to support on-board debugging directly with a desktop computer. Many require external debuggers/programmers, which are not necessarily cheap. It is preferable that the chosen chip support debugging without the need for extra equipment.

Power Consumption + Low Power Functionality: In many embedded systems applications, power consumption is usually of vital importance. However, microprocessor relays usually have a dedicated DC source fed from a station service transformer. The portion of the station with this transformer may become de-energized, but protection functions must still be carried out for the rest of the station. Consequently, the DC source also charges a large battery bank serving as a backup for the substation DC. Decreasing relay power consumption drives down the station battery-bank requirements, decreasing the sizing required. However, relay power needs are dwarfed by other station loads such as HVAC, circuit breakers, and lighting, and thus PHATCAT's power consumption is not nearly as important as its rapid response.

Microcontroller Options: With the relevant specifications and their importance to the project defined, several options can now be considered. Other less specification-driven factors considered in these selections include quality of documentation, ease of use for beginners, popularity in the hobbyist community, and recommendations from past successful senior design teams. All of these increase the likelihood that, during troubleshooting, good resources will be available for the specific issue. The main options considered are tabulated and compared in table 3.16.

All three of the examined microcontrollers are extremely powerful devices with clock speeds and program memories far in excess of what is needed for this project. However, this is by no means a bad thing, and is in part a consequence of the desired DMA and floating-point functionalities, which are typically present in the more powerful microcontrollers. All the examined microcontrollers support a wide variety of interfacing capabilities and will excel in this regard as well. The Microchip controller is short on I/O, but these requirements can be reduced by tying certain configuration pins on the ADC together or to V_{cc} or ground.

All of these platforms would be suitable for PHATCAT, but the TI chip, from its premium-performance Delfino line of C2000 processors stands out in several ways.

The first is its internal processor. While the other selections have powerful ARM chips, the Delfino uses a C28X processor. In addition to a floating-point unit, the C28X has specialized units for operations with trigonometric functions (TMU) and complex numbers (VCU), both of which are key for constructing and manipulating phasor representations of power system variables, as well as for performing FFTs. Thus, the Delfino will offer extremely high performance for the types of tasks PHATCAT must carry out. Additionally, the Delfino has a coprocessor that runs concurrently with the 28X. By delegating functions, high responsiveness for mission-critical tasks (e.g. protection algorithms) can be ensured even when the primary processor is faced with many, less important tasks, without degrading the system's ability to carry out either task. PHATCAT is not implementing the communications and event reporting data functionality common in modern protective relays, so this is not greatly needed. However, for a more feature-rich device, this prioritization is essential. The Delfino also boasts a fairly affordable development board, though the chip itself is far more expensive than its competitors. Due to its specialized features and rich array of relevant application notes, the Delfino TMS320F28377S will be used in PHATCAT.

Table 3.16. Microcontroller options considered

Device	ATSAME54N20A	LPC4337FET256	TMS320F28377S
Manufacturer	Microchip	NXP	Texas Instruments
Max CLK	120 MHz	204 MHz	200 MHz
Word Size	32-bit	32-bit	32-bit
Program Memory	1 MB Flash, among others	1 MB Flash, among others	1 MB Flash, among others
GPIO	81 I/O pins	164 GPIO	169 GPIO
Floating Point Unit?	Yes, 32-bit	Yes	Yes, also Trigonomic and Complex Units
DMA?	Yes, 32-channel	Yes, 8-channel	Yes, 6-channel
Dev. Board*	SAM E54 Xplained Pro, $84	OM13088: LPCXpresso4367 Development Board, $27	C2000 Delfino MCU F28379D LaunchPad™ development kit, $33.79
Communications	8 Interfaces, supports I2C, SPI, RS485, USB 2.0	USB 2.0, 1 SPI, Quad SPI, LCD controller	USB 2.0, 3 SPI, 2 I2C
Onboard Debugger?	In development board. External required otherwise.	In development board. External required otherwise.	In development board. External required otherwise.
Chip Cost	$5	$9.24	$25.36

3.3.13 POWER ELECTRONICS

With the core hardware components selected, a plan must be made to provide power for them. PHATCAT is specified as receiving power from a standard 120 VAC source. This makes it easy to power the device. Its active components have power varying power demands, requiring several different voltage levels. These requirements are tabulated in table 3.17. The listed powers are the total peak operating power for each component. Note that, in the real world, not every device will be operating at full power concurrently.

Table 3.17. PHATCAT Approximate Power Needs

Device	Nominal Voltage (V)	Peak Power (W)	Special Considerations
X2 **ADS8588S**	5V (Analog), 3.3V (Digital)	0.24W (Analog), 0.02W (Digital)	Low-noise Linear Regulator for Analog
X3 **EE2-12NU**	12V	0.42W	
MAX6979	5V	0.41W	
X6 **AV1610R112R04**	12V	1.44W	
TMS320F28377S	3.3V	1.6W	

There are additional power needs for the power lost to resistors, the optocouplers, and that which leaks through the protection diodes, but this can be accommodated for by keeping resistor current and optocoupler current small. Adding a 25% margin for these losses, we see PHATCAT needs 2.4W @ 12V, 0.82W @ 5V, and 2.1W @ 3.3V. Additionally, the power for the ADC analog portion should come from a linear regulator with a low ripple. The other devices are not as sensitive to ripple and can be powered from switching regulators.

With PHATCAT's power needs established, proper components are now selected. The general philosophy of the power design is to provide the highest voltage level needed (12V) and to use buck (as opposed to boost) regulators to supply the 5V and 3.3V needs. Switching voltage regulators, which take in a DC signal and chop it up into a square wave to be smoothed into a lower average voltage, can be used for the 12V and 3.3V needs. However, a linear regulator is needed for the 5V supply. The ADC requires low voltage ripple to ensure a stable internal voltage reference for accurate conversion. The selected 5V regulator will be loaded and tested with the selected 120VAC/12VDC supply to ensure adequate conditions for the ADC. See table 3.18 for initial component selections.

Table 3.18. PHATCAT Power Electronics

Device	Input Voltage (V)	Output Voltage (V)	Output Ripple (V_{p-p})	Output Power (W)	Cost
Meanwell RS-15-12	85-264VAC, 120 – 370 VDC	12V	120mV	15W	$9.55
NJR Corporation/NJRC NJM7805FA	7 – 35 VDC	5V	78dB Ripple Rejection	7.5W	$0.88
Recom Power R-78E3.3-1.0	6 – 24 VDC	3.3V	120mV	3.3W	$3.26

The 7805 is expected to dissipate up to 1.15W of heat in supplying the system's 5V needs. Thus, the larger TO-220 package has been selected. Without a heatsink, it is expected to reach some 75 degrees C above room temperature. Thus, an Aavid HS411-ND clip-on heatsink will be used to reduce this rise.

3.3.14 COMMUNICATIONS PROTOCOLS

The PHATCAT device must use different communication protocols to have the various devices communicate with one another. Their origins are briefly discussed in Section 4 – Related Standards. In this section communication protocols will be elaborated upon and chosen for the intercommunication of the microcontroller and the Printed Circuit Boards (PCB) as well as its communication to the Personal Computer (PC). All these protocols follow the oscillations of a clock cycle. These cycles will vary in speed depending on how computationally powerful the CPU is. In general, the CPU can perform actions within a certain number of cycles. Some operations can take a single cycle and are usually called atomic operations while others can take several cycles to perform. And in current more powerful CPUs many operations can take place simultaneously due to having multiple cores that can each operate independently of one another. As these cycles rise and fall the action can be performed on the rising edge which is the change from low to high, or the falling edge which, is from high to low.

The protocols may operate synchronously by using the clock of a master device the microcontroller. They may also operate asynchronously which would make them operate independently from the main clock and can sometimes make it difficult to send data back and forth between them [3.19].

SPI: Serial Peripheral Interface (SPI) is a common communication protocol used in embedded devices. It is a synchronous data bus using separate lines between the data and clock so that it can easily keep both in sync with the clock of the microcontroller. It is a full duplex data bus meaning that it can communicate in both directions. It generally has one master device that can be used to control the many slave devices (Fig. 3.31). In PHATCAT the master device would be the microcontroller that will communicate to the LCD and other slave devices. It uses four wires to connect to devices and transmit the data and clock signals. SPI has four logic signals SCLK is the serial clock from the master. Master Output Slave Input (MOSI) which, is the data output taken in from the master device. Master Input Slave Output (MISO) which, is the data output from the slave device. Finally, Slave Select (SS) which, is used to select which slave is going to be used at a certain time output from the master device [3.20]. SPI has four different modes based off Clock Polarity (CPOL) and (Clock Phase) which can be specified as a one or zero to form the unique modes. Mode0 is when CPOL and CPHA are both zero and the data will be sampled at the leading rising edge of the clock. Mode0 is the most common mode used in slave communication SPI. Mode1 is when CPOL is zero and CPHA is one. Will result in the data being sampled on the trailing falling edge. In Mode2 CPOL is one and CPHA is zero and in this case, data is sampled on the leading falling edge of the clock. The final mod3 is done when both are one. In this instance, the data is sampled on the trailing rising edge. For the master and slave to communicate correctly they must both be in the same mode.

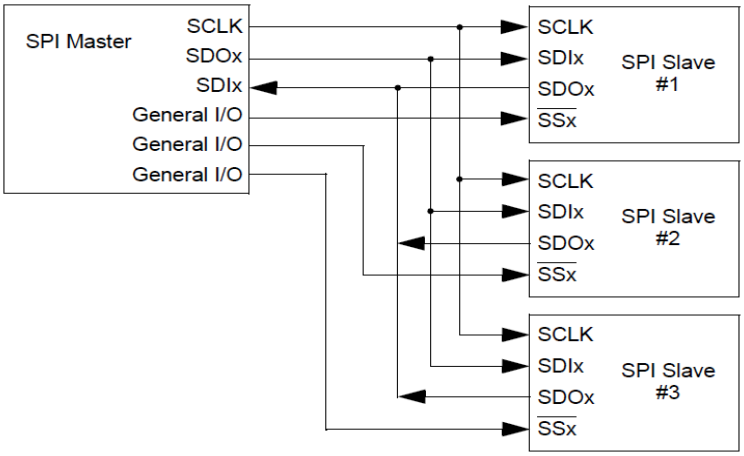


Fig 3.31. Master Slave SPI. Reproduction Permission obtained from electroSome.

There are many advantages to using SPI. For one it is much faster than the other communication protocols and is only limited by the speed of the clock and how fast the slave can react. It is also incredibly easy to implement SPI in both hardware and software because it is very simple to access the slave devices. The slave and master use an eight-bit shift register to send data back and forth and after eight clock cycles, the data has been completely sent and received. It's also not limited to 8-bit data and can continuously send data. The master can have many SS lines and be able to send and receive data at the same time due to its multiple lines and full duplex communication.

Those multiple lines can also be a disadvantage because it requires four lines, unlike its counterparts that only require two or three. There is also no common standard for SPI so each manufacturer can do it however they like, and it can sometimes make it difficult to communicate between devices based off the mode they are in [3.20]. The device must also have a specific SPI interface in order to use the protocol. If there is not interface built into the device, it cannot be used. It also has difficulty communicating over long distances due to the many wires it requires and the interference between them There is also no built-in error checking in SPI so that must be implemented by the developer if it is required for the application.

I²C: Inter-Integrated Circuit (I²C) is a common communication protocol used in embedded devices. It uses two wires a serial clock (SCL) and a serial data (SDA) to communicate between devices (Fig. 3.32). The SDA line is bidirectional, so it can do both MISO and MOSI. It supports multiple master and slave devices. Because of its design if you have two open pins between devices you can implement it without any special interface. It is usually used to communicate between slower devices such as ICs and the microcontroller. Everything in I²C is either a master or slave. The master device is generally the microcontroller and will handle reading and writing to the slave peripherals. The slave devices will only do what the master tells them and start any communication themselves. Each slave device will have a unique address to identify itself with the master device to not confuse slaves. I²C will always have a start condition in which the master will tell the slave devices that communication is about to start. After that an address frame is sent to the slaves to identify what devices it wants to communicate with. The standard address size is 7 bits so there is a maximum of 128 slaves. Then the data frames are sent in either direction. Finally, a stop condition is sent to tell the slave devices that communication is over. When the slave receives the data, it will compare it to its address if it does not match it will simply wait for a stop condition. If the addresses do match, then the master and slave will communicate serially. When data is sent and received the there is an acknowledgment sent before the next byte of data can be sent. Sometimes a repeated start condition is used to keep the slaves listening to one master so that another master can't take control in the middle of operation [3.21].

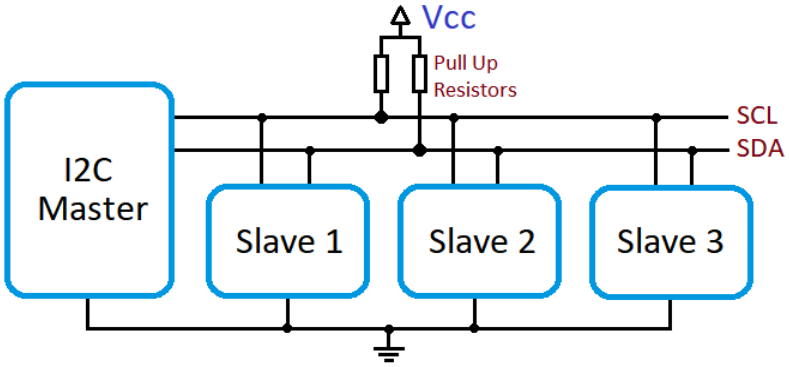


Fig 3.32 Master Slave I2C. Reproduction permission obtained from electroSome

I²C also has features to try and make up for some of its shortcomings. Extended addressing makes it ten bits. Meaning that up to 1024 slave devices can be used. In this mode, the master will send larger double words to the slave to let it know that extended addressing will be used. There is also clock stretching that can be used if the master clock is much faster than the slave device it can hold the SCLK low, so the slave has enough time to send and receive data. And finally, there is a high-speed mode that can up the data transmission rate to 3.4 Mbps.

I^2C has its advantages. The ability to be used in any device that has two wires that can be used for communication is very handy. The fact that it only uses two wires also limits the number of wires needed to implement the protocol. It can also support multiple master devices making it a good solution when many clock producing devices are present. Because of its ability to know who is sending what and keep data from colliding with one another. The checking of the data being sent and received with acknowledgments make it much easier to correct errors quickly.

Although I^2C has many advantages and tries to add functionality to make up its shortcomings. It also has some disadvantages as well. Even with the high-speed mode, it cannot reach speeds as fast as SPI. The built-in error checking can also slow down the transmission too. The constant need for starting and stopping can take a toll on the speed. Due to its many features that must be implemented like addressing the start and stop signals as well as the acknowledgments that must be sent between devices. Make it a little harder to implement.

UART: Universal Asynchronous Transmitter / Receiver (UART) is not a communication protocol like I^2C and SPI. It is a physical circuit that is built into a device to take in parallel data and convert it to serial data then send and receive it. UART is a full duplex communication that is asynchronous. It only uses two wires to transmit the data between two devices. Tx for transmitting data and Rx for receiving data. The transmission is composed of the start bit the data frame the parity bit and the stop bit. Instead of using a clock to send data it uses a start and stop bit, along with the baud rate to determine how fast the data will be transmitted [3.22].

UART has its advantages. It only needs two wires helps with the number of wires and the interference they produce. The fact that there is no clock signal that has been used for transmission is also a boon. It also has a built-in parity bit that can be used in error checking t determine if any bits got messed up in transmission. It is also possible to change just how the data is being transferred between the devices. The fact that it has been used in the industry for so long and mean It has been widely used and heavily documented.

While it has advantages it is not perfect. The maximum size of 9 bits limits the amount of data that can be sent. There is no support for multiple slave and master devices because it is only communication between two devices. Also, the Baud rate between the devices must match or the data cannot be transmitted between them.

After examining the standard means of communication. They all have their advantages and disadvantages. However, SPI's simplicity to implement as well as the speeds that can be achieved. In conjunction with the fact, the single master model fits our PHATCAT design. Where the microcontroller will be the master device that will communicate with all the slaves. And the relatively short distances that will be traveled between the components. Make SPI the preferred method of communication.

3.3.15 PROGRAMMING LANGUAGES

A programming language is how developers can get computers to behave in the way we want. There is certain terminology that is required in the discussion of programming languages. A program can be compiled or interpreted and in many current languages they do both depending on what is necessary. Compilation is when one language of code is translated into another language. Generally, from a high-level language to a lower one. This is done by a compiler which is a specific program to perform that function. Happening at compile time which is before the start of the program called runtime. Thus, making it impossible for the code to change the way it will be executed. Meaning any changes to the program will have to be recompiled before taking effect. An interpreted language stays in the same format that it was written but will execute specific subroutines. Which is a set of instructions the computer will perform based on the commands received. This makes it possible for the program to modify itself by adding or removing functionality before it is executed at runtime. And enable changes to be made to the program without the need for recompilation. There is also a linking step between compile time and run time where libraries which, is just code written in a different file is pulled in and compiled too. These libraries which, are

generally written by professionals in the field can be used to make it incredibly easy to implement functionality on a computer. Readability is another important concern of a programming language. This is determined by how close the language is to human language and how easy it is to read and understand without special training. Programming languages have different levels that determine how close they are to bare metal components of the device. As you go lower you get closer to communicating directly with the chip. These levels will be explained below and after certain languages will be considered for the embedded applications and the desktop application that will be used with PHATCAT.

Binary/Machine Language: The lowest level is binary called machine language and is a series of ones and zeroes that the processor understands and uses to perform the tasks based on their patterns. The processor can understand them but it's very difficult for a human to understand what is happening by examining the code. Only very specific low-level applications are written in machine language and require special training.

Assembly: The next level up is assembly language which is the lowest language that works with a processor that a human can understand with some training. Assembly language is specific to the chip that the device uses so the people working with it must know that language and its instruction set. Which is a command that makes the processor perform a task. It also requires several more lines of code to achieve the same effect in higher level languages. Being the closest programming language to binary makes it perform incredibly fast in terms of execution time compared to other languages that must be read and translated by the compiler. However, with today's optimized compilers, many languages can come very close to the speeds achieved by assembly. Resulting in quicker production time due to its ease of writing and understand compared to assembly language.

Low-Level: Taking another step up is low-level languages. These languages can be used on many different chips and use a compiler to translate the code to the machine language that the chip can understand. This is where most programs for embedded systems operate. Being much more readable than assembly language and not having to learn a certain chips instruction set can be very beneficial. Low-level languages are generally compiled before run time. So, they cannot modify the way they operate within themselves.

High-Level: The final level of programming languages is high-level. These languages are generally very easy to understand and designed for simplicity to use. Having high readability makes production time shorter than lower level languages. In high-level languages, it is difficult to access specific addresses in memory if not impossible. The compiler/interpreter will decide what memory locations will be used and the programmer has no say. The compiler/interpreter also takes care of memory management and will use garbage collection to clean it up properly to avoid memory leaks and segmentation faults. This can slow down the program and can be called at any point in time. So high-level languages are generally not used for mission-critical programs due to this fact.

Embedded Application: There are approximately two hundred and fifty-six different types of programming languages that are used throughout the world. However, for embedded systems and their constraints, it limits the number of usable languages considerably. Of the languages discussed above more than 90% of embedded applications are written in low-level languages [3.23]. The important features to consider when working with an embedded application are. The ability to access memory addresses necessary to interreact with the microcontroller and connected devices. The ability to quickly respond to interrupts that will be activated when the device detects a fault in the system. The ability to take in the data sent to it through serial communication sent from the desktop application and configure the PHATCAT.

Embedded Language Options: C is a low-level language and is the main programing language used in embedded software. In C it is possible to access any address of memory the developer states. Which can be difficult to work with because they may accidentally access memory that is system critical and crash the device. The ability to dynamically create memory as needed is a boon and a curse because if the memory is not properly cleaned up it can leak and cause performance issues on the device. There are also a lot of libraries written to be used in many different embedded devices.

Rust is an open source low-level language that was developed by the Mozilla, the same organization that created Firefox browser. It is becoming a very popular language to use because it has been designed to alleviate a lot of the problems associated with C/C++. As well as its ability to make the memory management easier and safer make it one of the top-rated newer languages. By having guards in place in the language to make it impossible to access memory you are not supposed to as well as reminders to clean up memory allocation [3.24].

High-level languages are generally not used in embedded processes due to their larger size and inability to directly control memory access. Which are both incredibly important in embedded devices due to their limited memory and requiring memory management to control parts of the device. There is, however, a high-level interpreted language that works in embedded systems Python. A special version of python called MicroPython built on C so it can be used in embedded devices [3.25].

Choice of language: The various languages considered, along with their features, are compared in table 3.19.

Table 3.19 Embedded Application Language Comparison

Language	**Rust**	**C**	**MicroPython**	**Assembly**
Level	Low	Low	High	Low
Compiled/Interpreted	Compiled	Compiled	Interpreted	Compiled
Execution Time	Fast	Fast	Slowest	Fastest
Production Time	Short	Long	Shortest	Longest
IDE on Microcontroller	No	Yes	No	No
Readability	Low	Low	High	Very Low
Experience	No	Yes	No	Yes

VHSIC Hardware Description Language (VHDL) and Verification of Logic (Verilog) are also low-level languages which, are hardware languages designed to be used with Field Programmable Gate Arrays (FPGA). Since the PHATCAT will not be using FPGA it is not necessary to explore VHDL and Verilog Several different options were considered for the embedded portion of the programming language. The machine language assembly is the fastest choice of all the languages. However, due to the difficulty to program and understand. It has been removed from consideration. The high-level language MicroPython is designed to make the life of the developer easier. By having superior readability and high-level features such as garbage collection. Which will periodically check if certain parts of memory are being used and clean it up properly if it's gone unused for a certain period. This will remove the fear of segmentation faults. Which is an error raised when trying to access memory that is not supposed to be accessed. As well as avoiding memory leaks. However, since MicroPython is interpreted to C and the PHATCAT requires very fast interrupts to function properly in the event of a fault. And the fact that MicroPython is only supported on certain chipsets and the chip on the microcontroller we will be using is not supported. Making it unable to be used in the desktop application. The low lever Rust language is growing in popularity rapidly because it is avoiding pitfalls that C encountered. It's built-in protections for common memory errors make it a good candidate. But due to it being a newer language and not widely used means it may be difficult to find help if we have difficulty implementing it. The fact that the developer board has an Integrated Development Environment (IDE) designed to be used in C. And C's ability to dynamically create and access any memory

location required. As well as the experience among group members with the language. Make C the language of choice to be used in embedded development in the PHATCAT as a language to use.

Desktop Application Language Choices: The desktop application does not have the same constraints imposed as working in an embedded environment. The application will be built on a computer with a full Operating System (OS) and IDEs available to assist in writing the program. Making for a plethora of choices that could be used for the application. Important features of the desktop application include: having an easy to use graphical user interface (GUI), sending data to the microcontroller via communications, and the ability to take in user input and logic and control the microcontroller and its connected devices. These languages will be discussed below and compared with one another until a single choice is determined.

C is the language of choice for the embedded application. It is also possible to make a graphical user interface (GUI) in C using specialized libraries. And its ability to directly control memory access make it a powerful tool.

C++ is an Object-Oriented Programming (OOP) language. Meaning the language is designed to build objects that will have properties that can be acted upon. Built on C framework making it still possible to access memory locations and keep the speed of the C language. But has special features implemented to make it easier to handle the memory allocation. To avoid memory leaks and segmentation faults.

Rust, as stated before, is a low-level language that has been built to alleviate a lot of the problems that can be encountered when working in C/C++. Its built-in protections make it easier to work with memory than C/C++.

Java is a high-level language designed by Sun Microsystems and later acquired by Oracle. It is an OOP class-based language. The beauty of Java is that the code is run in a Java Virtual Machine (JVM) and converted to byte code that can be read by the processor. Making it possible for Java to run on anything that can support the JVM. Java will handle all memory allocation and clean up after itself with a garbage collector.

Python is a very popular open source high-level interpreted language. Its ease of implementation and readability make it an ideal language for beginners. Python has made it grow in popularity quickly since its inception in the 1980s. If it exists in computer science, there is probably a python library and a community that supports it ready to assist. As stated above in the paper there is even a special Python created for embedded applications. Where high-level languages are generally never used.

The various languages considered are compared in table 3.20.

Table 3.20 Desktop Application Language Comparison

Language	**C/C++**	**Java**	**Python**
Compiled/Interpreted	Compiled	Compiled	Interpreted
Experience	Moderate	High	Low
Readability	Low	High	High

All the examined languages have their uses, and most could be used to write the desktop application. One language must be chosen as the preferred choice and that will be discussed here. C while being the number one language for embedded design and having a way to make a GUI relatively easy. Is not the language of choice because the application will not be required to access specific memory addresses and the ability to ignore memory allocation errors will make this application easier to develop. C++ could help with its easier to manage memory allocation. It also has built-in libraries to assist in GUI design. However, the application does not need to be the fastest part of the device and waiting for garbage collection and being able to edit

code at runtime will make interpreted languages more useful. Rust is an impressive new language that is getting a lot of followers due to its great design and ability to guard against many memory errors. But the fact that it is a newer language and has no built-in tools to help with GUI design remove it from the candidate list. Java is an easy to use language and has a built-in tool to assist with assembling GUIs. This, as well as the fact that it is the language with the most experience, make it an excellent choice. Python's popularity in the computer science community and its vast library set make it an excellent choice for the application. Though the team does not have experience in Python. It is an important language to learn and senior design is an excellent platform to learn new skills. Thus, Python has been selected as the language of choice to use in the desktop application.

3.3.16 DESKTOP APPLICATION

The PHATCAT desktop application is one of the most important parts of the device. It is going to be one of the main sources of interaction with the user. It will have a Graphical User Interface (GUI) that the user will interact with the do various things with the PHARCAT. A use case diagram is useful tool in understanding how the desktop application will operate and interact with the other components of the PHATCAT.

Use Case Diagram: In fig. 3.33, it can be seen that desktop application is the central part of the device and handles all communication between the user and the microcontroller. The desktop application will be written in python, which has several libraries that can be used to make it easier to create a great User Experience (UX). It also has libraries that will make it easier to communicate with the microcontroller.

Upon initial connection to the device the application will send a request to the MCU to pull the settings it currently has stored. After it has those settings it will display the current settings the device is using. The user can then decide if they want to change the settings and modify the configuration of the device. The settings can be modified by using key labels that are user defined and can be used in conjunction to configure the device. These configurations can be parsed by the application and translated to data that can be sent to the microcontroller and configure the PHATCAT.

Mock Up: A mockup of the application is a great way to visualize how the application will look when it is running and being interacted with by the user. When the application is first run there will be an initial opening screen with the PHATCAT logo in all its glory (fig. 3.34). After connecting the device, it will import the settings that are stored on the MCU and allow the user to navigate those settings in the GUI (fig. 3.35). There will also be a text editor pane where the user can enter their own logic expressions that can be parsed by the application and sent to the MCU. There will also be an option to save and load the user defined settings so that progress is not lost each time the application in started up.

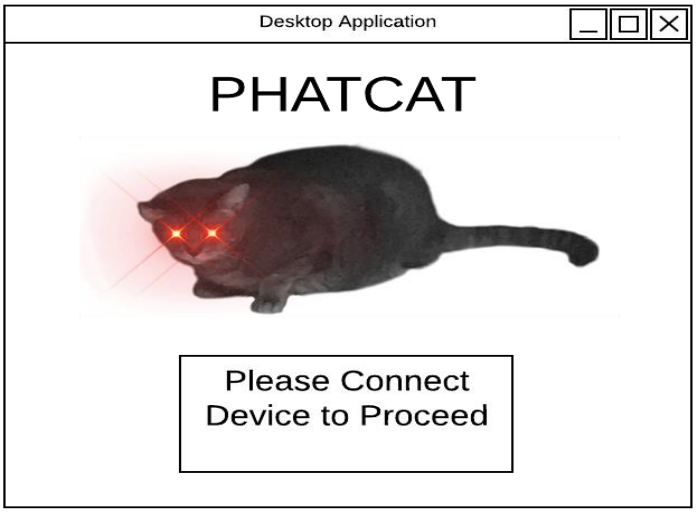


Fig 3.34 Desktop Initial Open Mockup

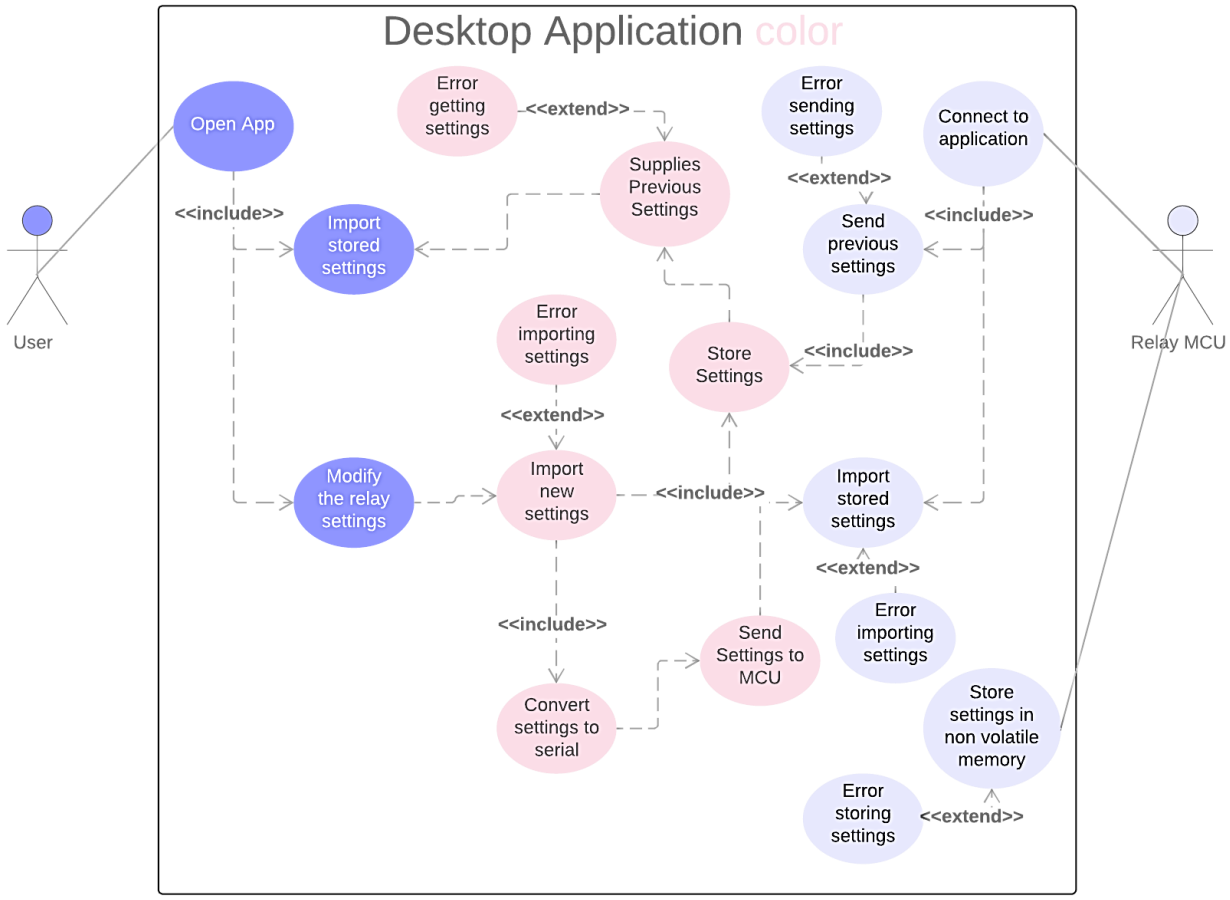


Fig 3.33. Desktop Use Case Diagram

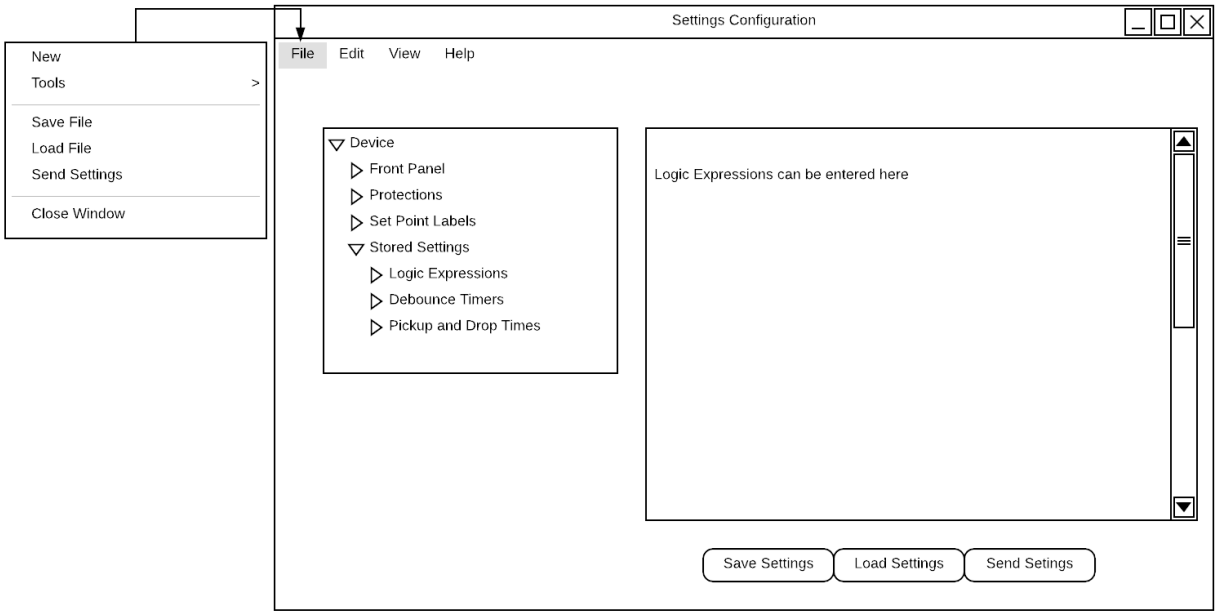


Fig 3.35 Desktop Config Settings Mockup

3.3.17 System Frequency and Phase Angle Determination

Since phasor representations presume a certain sinusoidal frequency, the system frequency must be determined before frequency components can be extracted for the purpose of constructing phasors or quantifying harmonic content. Because this algorithm will be tied to detecting periodicities, it is also convenient to use this algorithm to determine the phase angles between inputs. This algorithm, rather than focusing on being accurate for a wide range of frequencies, should be as accurate as possible for a small range—power system frequency is regulated within $\pm$.05 Hz, so even a small standing error will cause problems. If a discrete Fourier transform with little spectral leakage is used, this can result in the retrieval of wildly inaccurate magnitude results when pulling the fundamental frequency component from the array of DFT results.

Zero-Crossing Detection: A zero-crossing detection (ZCD) algorithm determines the frequency of a signal by detecting when a sinusoid crosses a zero value and counting the elapsed time between zero crossings. A comparator-type device, such as a Schmitt trigger, can be used to create a bi-stable circuit that will clamp to V_{cc}+ for positive voltages and V_{cc}- for negative voltages. The output can be sent to a microcontroller and the time between changes can be counted to determine the frequency. However, this is made inaccurate by DC and harmonic content, requiring additional hardware. Because an ADC is already necessitated for other device features, it is more sensible to implement ZCD in software.

The odds of ever actually sampling a value of zero are very low, so it is not used to detect zero crossings. Instead, the sign of the next value in the series is compared with the sign of the previous. This is computationally very fast, as only the most significant bits need to be logically AND-ed. DC components can be subtracted from the signal by keeping a running average and subtracting it from a sample before checking the sign. A digital bandpass filter can be used to remove harmonics; since the lowest possible considered harmonic frequency (90Hz, 2nd harmonic of 45Hz) is higher than the highest considered system frequency (65Hz), a single passband can eliminate all possible harmonics without eliminating any possible fundamental frequencies. The small jitters introduced by noise may cause false crosses near the zero threshold, triggering multiple, rapid zero crosses in a short window. To avoid this issue, hysteresis can be implemented. That is, not only must the sign change, but the value must be above a certain threshold.

A preliminary Matlab program demonstrations the function of this algorithm. The 60Hz sinusoid shown in figure 3.36 is sampled at 8kHz for a 0.1 second window before being passed as an array for processing by the ZCD algorithm.

The algorithm tracks the frequency almost immediately but oscillates about the true value indefinitely. Due to the discrete timesteps used, this algorithm's accuracy is limited by the sampling frequency. In the example given, the output alternates between 60.6Hz and 59.7Hz. In many applications, an error of +1% / -0.5% would be sufficient. However, due to the tightly regulated nature of power system frequency, a frequency error of 0.6Hz may be unacceptable. It can be further improved with two averaging methods. The first is making the currently detected frequency the average of the last two frequencies detected (i.e. the midpoint of the oscillation). This process can be nested several times (i.e. find the midpoint of the last two midpoints, and so on) to converge the oscillations somewhat. Then, a running average of the last five determinations of the midpoints determined can be kept. This greatly smooths the oscillations, giving an output of 60Hz exactly, with occasional momentary forays into 60.01Hz. There will be a slight delay in the tracking ability of the algorithm due to the averaging, but this will not greatly affect PHATCATs algorithms. What appreciable error is present in this method will likely arise from imperfections in the digital filtering required to remove harmonics.

However, it has the additional benefit of allowing for easy calculation of phase angles—the time between zero crosses between different channels with respect to a constant reference channel can be used. The algorithm must distinguish between positive-to-negative and negative-to-positive crosses, but this is easily implemented.

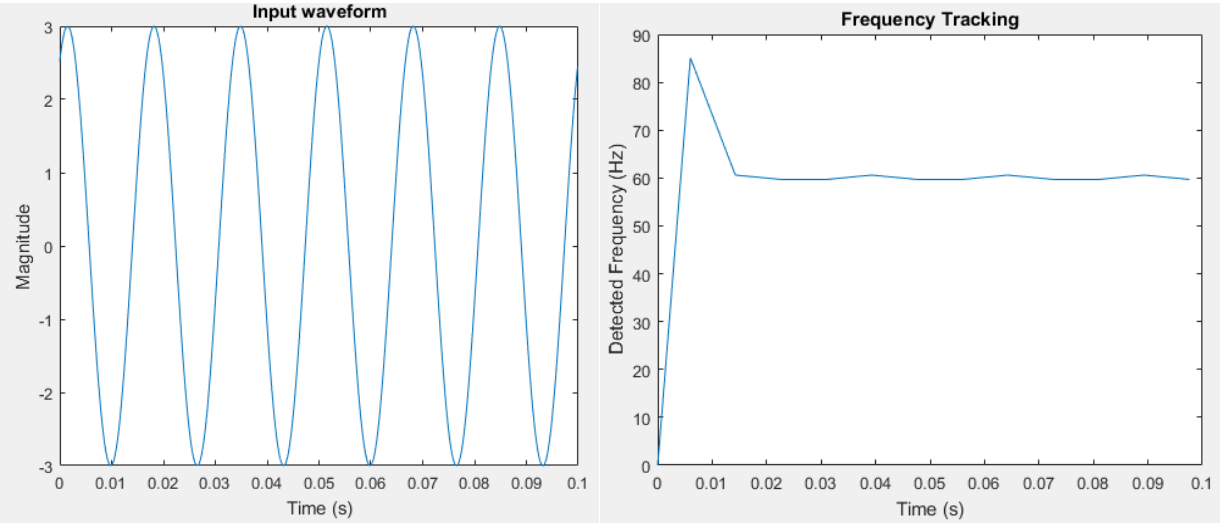


Fig. 3.36. Input waveform for ZCD algorithm (left) and algorithm results (right). Produced with Matlab by B. Ross

Machine Learning: Machine learning is a process of giving a computer a data set and having it learn from the data and begin to be able to predict what the future of that data will be. It was believed that machine learning might be a good approach for trying to predict the sine wave frequencies if it was properly trained with enough points early on to be able to predict the rest of the sine wave. Recurrent Neural Network (RNN) was examine which can use previous data to try and predict future data. The specific RNN used was Long Short-Term Memory (LSTM) that is generally used to predict time series data. After finding out the LSTM algorithms did not predict the sine function well outside of the initial data set other forms of machine learning were examined [3.27]. Feedforward Neural Networks (FNN) is a network that has no cycles. It will only continue in one direction after the input data. The fact that the network did not cycle to investigate previous data made it very bad at predicting periodic sine waves [3.28]. After doing the research it appeared that most training methods in machine learning were unable to generate a periodic sine wave with enough accuracy for the PHATCAT to function correctly [3.29]. So, utilizing machine learning in the PHATCAT was abandoned.

Fast-Fourier Transform: The FFT is a modified version of the Discrete Fourier Transform (DFT) that exploits some of the symmetry inherent in exponential functions with imaginary exponents to simplify the number of operations required. A 1-Dimensional array of samples fed into an FFT function and multiplied by 2 divided by the number of samples will give another array of complex numbers, with each number corresponding to the magnitude and phase of a frequency component. However, there is one serious challenge to be overcome. It is required that instantaneous protections be able to trip with no more than two power system cycles of delay (33.3ms). Leaving some time for computations and a safety margin, it's desirable that we only take one power system cycle to sample the input values to be transformed. Care must be taken when trying to obtain accurate FFT results from such a brief sampling period.

For determining the fundamental frequency, the absolute accuracy of the magnitude measurements is of little concern. Instead, it is the relative magnitude that is of most import. Because harmonics are, by their very nature, lower in amplitude than the fundamental frequency component, accurately locating the highest-magnitude frequency component in the signal means locating the signal's fundamental frequency component. This criteria is further secured by considering that, since we only design for system frequencies between 45 and 65 Hz, the lowest possible 2nd harmonic frequency (90 Hz) is still lower than the highest possible fundamental frequency. So we can bound our search to avoid picking any harmonics as the fundamental frequency. One challenge with this approach is the limited number of samples contained within a one-power-system-cycle of time. It is likely to be only on the order of hundreds. This means that there

will be relatively few discrete frequency bins. Zero-padding (adding samples with a magnitude of 0 to the end of an array of samples) can be used to improve the binning, providing a very precise frequency measurement. Compare the following frequency response plots of a FFT resulting from a 65Hz signal with large harmonic content sampled at 6.25kHz for 22.2ms (Fig. 3.37).

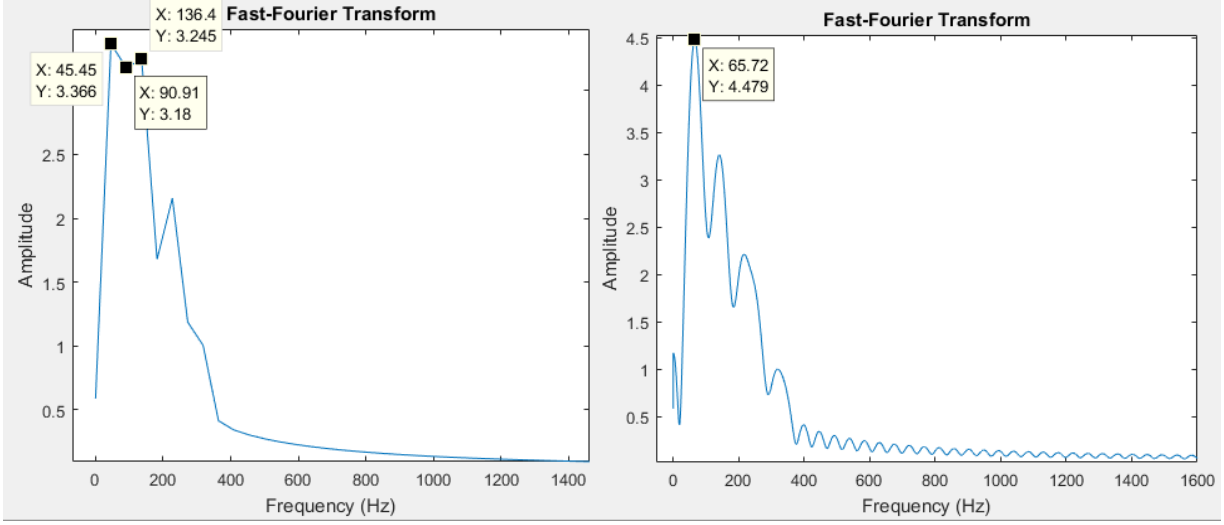


Fig. 3.37. Fundamental frequency detection without (left) and with (right) zero padding. Produced with Matlab by B. Ross

With no zero padding, the maximum (3.366) is nowhere near the real value. However, once a large amount of zeros are added to the time-domain samples, the frequency resolution increases greatly. The maximum value occurs within 1.1% of the real frequency. Initial Matlab simulations estimate this to be the most accurate this method can be – it will be impossible to differentiate more precisely between points near the maxima with single-point precision and the estimated value seems to vary nonintuitively based on both the fundamental frequency and sampling frequency.

This method brings with it an easy method for obtaining the system phase angles. Because the chosen ADC performs truly simultaneous sampling of all input channels, all 14 FFTs will output complex numbers with the same reference – the beginning of the sampling window. Thus, a simple arctangent calculation will allow for all phase angles to be obtained. A channel can be chosen to serve as a reference from the others, and the phase difference between it and the beginning of the FFT window can be subtracted from all signals.

Of the above methods, the ZCD method offers the highest accuracy and arguably the lowest computational burden. Even the averaging improvements will be light computationally; they only require floating point addition and division by 2. The downside to this method will be the need to design a digital Butterworth filter to remove any harmonic content before processing the data stream. However, this will be achievable fairly easily by creating the desired analog transfer function and mapping it to the z-domain.

3.3.18 Phasor and Harmonic Magnitude Estimation

With the fundamental frequency known, the magnitude of the fundamental frequency and the second, fourth, and fifth harmonics should be obtained. The phase angle should then be calculated with a reference that is common to all current and voltage measurements. Two methods for extracting individual frequency components are considered.

Digital Filtering: One methodology is to use digital filters to isolate individual frequency components in a sample set. For instance, a raised cosine filter is a digital filter with a frequency response characterized by a cosine function. Its impulse response takes the form of a sine cardinal function that passes through zero for adjacent sample values. This means that the impulse response to a symbol at time T will be zero at *2T*,

3T, …. *kT*. Consequently, the only signal present at sample *kT* will be a symbol received at that instant. This can be used to band-limit an incoming signal. A sampled data set can then be broken up into separate bands, one for each frequency component desired. Once a single frequency component is isolated, it is not necessary to perform a computationally-expensive RMS calculation. Instead, one can simply calculate the hypotenuse defined by two sampled values taken at 90 degrees delay. In other words:

$$\text{Asin}\left(\omega t + \frac{\pi}{2}\right) = Acos(\omega t) \;\; ; \;\; \cos^2 x + \sin^2 x = 1 \;\; => A = \sqrt{[Asin(\omega t + \frac{\pi}{2})]^2 + [Asin(\omega t)]^2}$$

Two samples are taken from a pre-sampled and cosine-filtered window, one at *t* and another at $t - \frac{\pi}{2\omega}$. The Pythagorean theorem is then used to calculate the magnitude of the phasor.

Fast-Fourier Transform (FFT): Because the FFT produces complex numbers with a magnitude equal to the input peak, it is well-suited for obtaining the various magnitudes needed. However, the challenge presented by the brief sampling time affects its proper application. Consider the following function:

*5sin(2pi*60*t+1) + 4sin(2pi*120*t+2) + 3sin(2pi*180*t+3) + 2sin(2pi*240*t-1) + sin(2*pi*300*t+1)*

The function is sampled at 8kHz for 50ms. Matlab is used to perform the FFT and generate the plots (3.38). We see that the FFT has successfully determined the frequency components of the original signal with a high degree of accuracy. However, in our application, 50ms is far too long a delay for sample acquisition. If we reduce the sampled time to only 20ms, our magnitudes become very inaccurate (Fig. 3.39). Not only are our binned frequencies not lining up with the frequencies we are interested in, but the linear interpolation between frequencies gives very inaccurate magnitudes. The source of this issue can be seen by looking at the input waveform. The FFT is designed for periodic waveforms. Repeating the input waveform periodically shows a big discontinuity at the end of each period (Fig 3.40).

In many applications, this would be difficult to overcome. But, since we have a knowledge of our system frequency from our frequency tracking algorithm, and our other signals of interest are harmonics of this frequency, we can avoid these discontinuities. For instance, in this case, our frequency tracking algorithm will look at the sampled values and determine the fundamental frequency to be 60Hz. Any sample set passed to the FFT that is a multiple of 1/60 = 16.67 ms will not have a discontinuity at the end. Consider the FFT results obtained for a sampling window of 16.67ms (one cycle, Fig. 3.41).

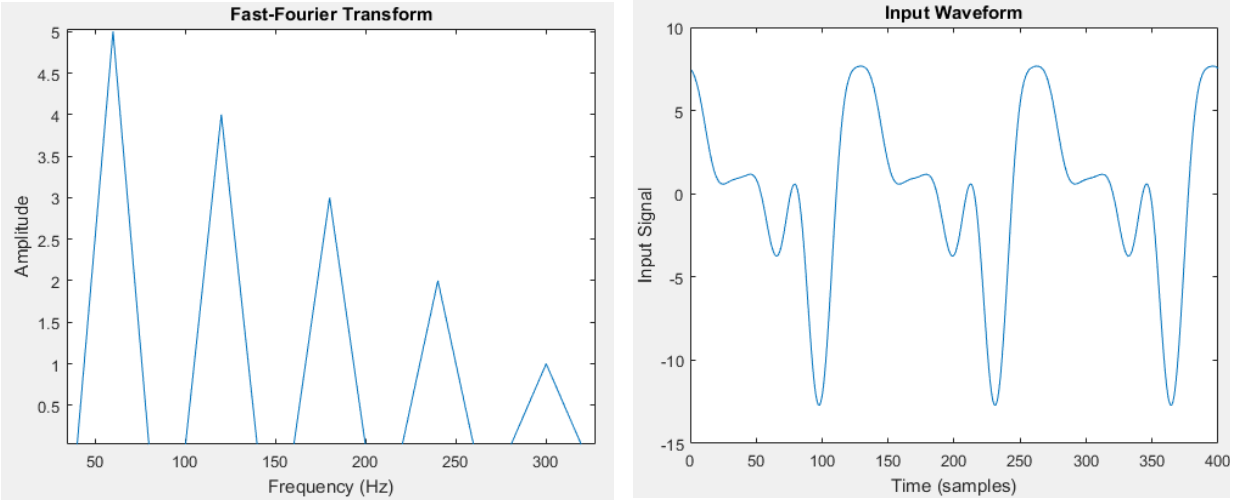


Fig. 3.38. FFT Magnitude Components and Input Waveform – 50ms window. Produced with Matlab by B. Ross

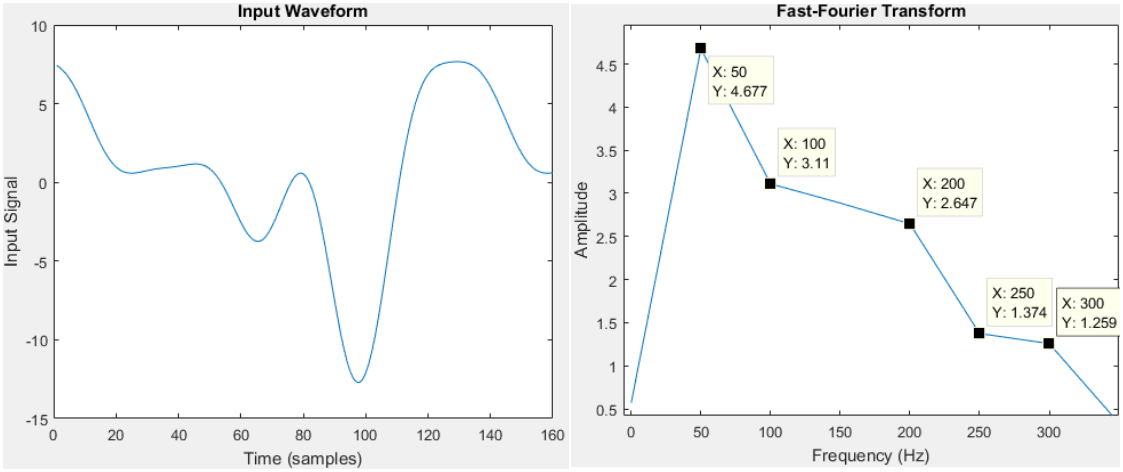


Fig. 3.39. FFT Magnitude Components and Input Waveform – 20ms window. Produced with Matlab by B. Ross

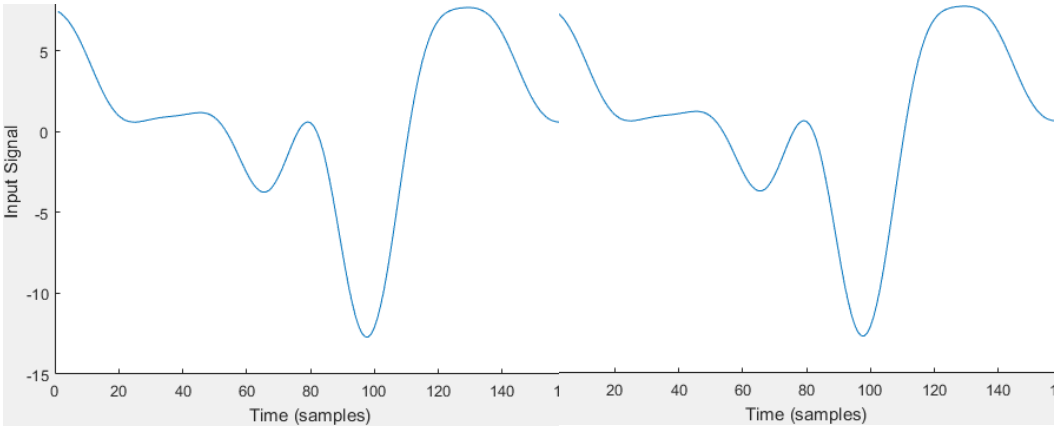


Fig. 3.40. Discontinuity between periods of sampled signal. Produced with Matlab by B. Ross

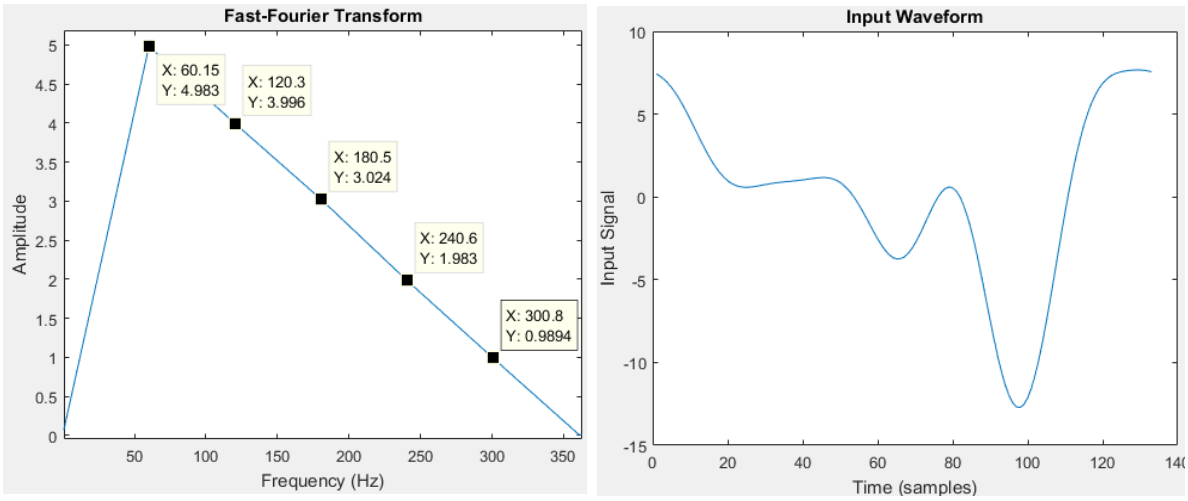


Fig. 3.41. FFT Magnitude Components and Input Waveform – 20ms window trimmed to 16.67ms. Produced with Matlab by B. Ross

While there is a large amount of spectral leakage, our frequencies are binned very near the system frequency and the magnitudes are very (~1%) accurate. Because we know the frequencies we are looking for, this spectral leakage does not degrade performance. In fact, it helps by keeping the measured magnitude very similar for close frequencies. In other words, even though our 3rd harmonic is binned by the FFT at 180.5 Hz, this frequency component has basically the same magnitude as 180Hz. So, we can just pull the 180.5Hz data point from the outputted FFT array and have accurate results without needing interpolation. From this we conclude that, as long as the input data set is trimmed to consist of one power system cycle of data, our FFT will provide accurate magnitude data for all signals and their 2nd to 5th harmonics.

During this study, the effects of zero-padding and windowing functions on the FFT were also analyzed. Zero padding aided in resolving the exact frequency more clearly but did not improve amplitude accuracy. Due to the shortness of the dataset, windowing functions, while reducing the discontinuity at the end of the signal, leave too little unattenuated content in the middle of the sample set for accurate magnitude determinations.

Phasor and Harmonic Methodology to be Used: Both the cosine filter and FFT methods will work for our needs, but the FFT is preferable for multiple reasons. The first is ease of application. For the digital filtering method, a filter will have to be designed for each frequency component. Each frequency component's magnitude must then be individually calculated. For FFT, many libraries are available. A preliminary study of these has revealed that the FFT for all fourteen data sets can be performed in a single function call. The second, more compelling reason, is the much lighter computational burden of the FFT. It produces all the needed magnitudes with no extra processing required. It only needs to process one data set, as opposed to breaking the data stream into five filtered sets. It does not need to perform the many slow square-root computations that the digital filtering method does.[6] All that must be done is the trimming of sampled values that are in excess of one power system period. This can be easily done by comparing the number of samples read in to the number of samples in one period at the current system frequency. For PHATCAT, the lowest frequency to be tracked is 45 Hz, which gives a period of 22.22ms. The number of samples read in can be fixed based on this number, as more samples than this will never be needed. In conclusion, PHATCAT will use the Fast-Fourier Transform on a dataset consisting of one power system cycle's worth of samples to determine the magnitudes of the fundamental, second, fourth, and fifth harmonics.

3.3.19 ENCLOSURE

For the design of the enclosure of the PHATCAT is to follow the industry standard speciation's towards a means of being able to integrate with the equipment already used in practice. By adapting to these standards, it offers a set of powerful business and marketing tools to be utilized for the project design. The power industry already has a set of standards in which they operate within to reduce the waste of resources and inventory of items that economically, don't make sense to purchase. Adapting the standards of the enclosure PHATCAT can become an efficient and sustainable device which can be integrated to tools that most power industry users already own. This will improve the market in which demand for this device will be in and provide an advantage for this transformer relay.

The standard dimensions used for a relay box has a width of 19" with a height of 3.45" commonly known as 1U and a depth of 14.25". It is important to follow mainly the width as these enclosures are often mounted on a relay rack. The fig. 3.42 shows a relay rack which is commonly used by the power industry and has a standard width of 19". For the design of PHATCAT, the height is initially going to be selected to be 3U or 5.20", a width of 19" and a depth of 14.25".

[6] Some relay manufacturers utilize the digital filtering method and use approximations of the Pythagorean theorem in conjunction with look-up tables of pre-calculated values to reduce the computational burden

This will provide an estimated $1400 inches^3$ enclosed for the components. This space will be to ensure that the all the components selected for transformer relay will fit inside and provide enough ambient space to allow sufficient heat dissipation. If necessary, small cooling fans can be installed to provide cross-sectional cooling to the enclosure. These are often used in relay designs to provide a controlled temperature environment where the components operate at recommended temperatures. By controlling the heat dissipation, the components will operate in optimal conditions and reduce the risk of overheating.

Fig. 3.42. Standard Relay Rack. Reproduction permission requested from Rack Solutions

Fig. 3.43 is the back panel of the ALP-4100 protection relay and has the design aspects that will be applied to PHATCAT. The sections #13, #17 & #19 will be adapted into the design and will correlate as follows: #13 has the current analog inputs which will be connected to the test device which will simulate the current and fault conditions as needed. #17 is the voltage analog inputs which, similar to the current inputs will be connected to the test device. #19 is the outputs for the relay which will "disconnect" the corresponding zone when a fault is detected. It is important to note that, PHATCAT is not a full-scale relay which is why only part of the ALP-4100 back panel outputs will be implemented. The figure chosen still provides a great illustration on how the back panel of the relay will be designed and built.

Now that the outside of the enclosure has been discussed, just as equally important is the logistics on the inside. Each component must be mounted in a way that keeps wires from shorting or loosely moving around in the enclosure. This can lead to damaged PCB and other sensitive components that are in the enclosure. The PCB can be designed with mounting through-hole options to ensure that the PCB will be secure. Additionally, with eight current transformers and six voltage transformers, each with wires that must be inserted through the back of the enclosure. To visualize the initial set up without the test unit connected, figure 3.43 is the backside of the relay. Each input will be connected to transformer which will lead to the transformers being placed towards the back of the enclosure. This will allow for shorter wires to be used and an overall more organized relay.

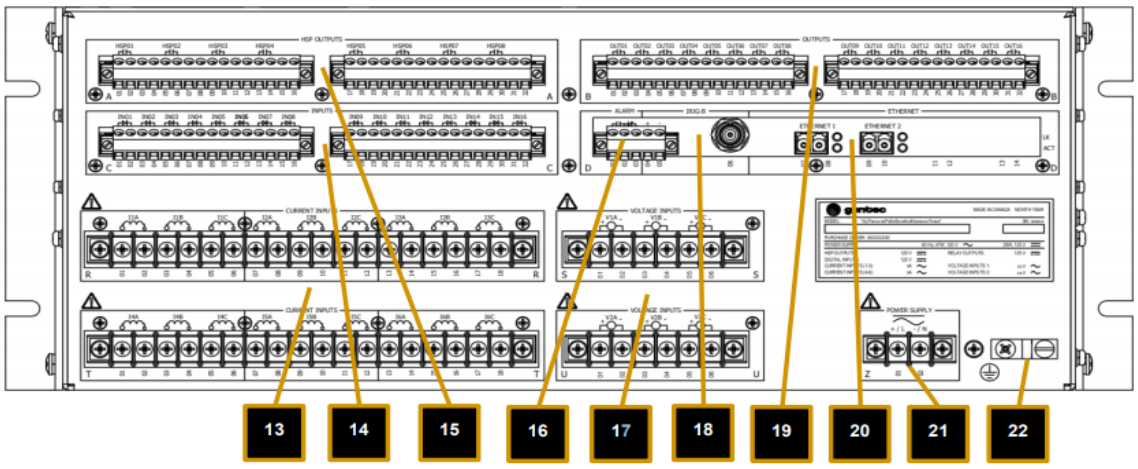


Fig. 3.43. ALP-4100 Back side of the enclosure. Reproduction Permission requested from Gentec.

The transformers will be mounted on the inside of the enclosure on a removable slab which can be removed in case of damaged transformers. The slab will be mounted to the enclosure while the transformers then mounted on top. If need be, the slab can be designed to have two different levels stacked on each other to provide more room to place the transformers. By stacking the transformers on a single removable pad, the whole pad could be removed allowing for access to vital components which will experience the highest power dissipation in the relay.

Diving into the front panel of the PHATCAT, the relay must also provide a way to interact with the engineer or technician and provide an output for information. The initial design of the front panel will be chosen after the comparison of material seen in table 3.21. This table will go to the extent of materials considered in building the enclosure and the advantages each provides.

On the front panel of the relay, a display will be used to provide information as to what is happening regarding the current and voltage measurements.

There will be LEDs to inform the user if there is a fault and which phase the fault is on. There will also be LEDs for the protective functions. Each state will have a corresponding code shown on the front panel which will relate to an industry standard known by the user.

For illustration of the front panel, fig. 3.44 is used which is taken from a professionally used microprocessor relay, the ALP-4100. The front panel is shown with an LCD (#1), a slot for a code identifier (#2) and customizable push buttons (#3). These three items which are part of the ALP-4100 will be integrated into the PHATCAT design. Some items discussed below are not shown in figure 8.X but will be included for the convenience and simplicity of the project.

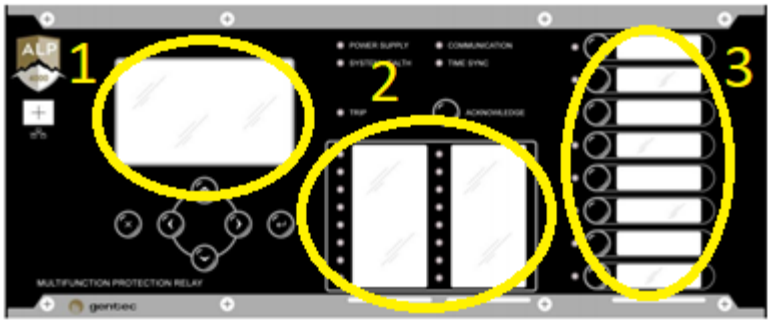


Fig. 3.44. ALP4100 Front Panel View. Reproduction Permission requested from Gentec.

The front panel will also include a mounted main power switch controlling the main power supply to the relay. This switch will be covered to ensure a double step process must be taken to reduce the possibility of turning the relay off during testing or on while in storage. For the consideration of the user, a computer port will also be mounted which will allow for a cable to connect. There will also be push-buttons with a double step process for the same reason mentioned above. The push-buttons will have hard coded actions addressed to each one but can also be programmed to have customizable options. This will provide an open source like option to the relay and allow for dynamic customization. The front panel will have a code engraved on the front which will correspond to each individual push button.

The wires running from the items listed above will have to be organized in a manner in which they will not interfere with other components. Placement of the PCB will be selected later as the design of the PCB evolves and the components are placed.

After considering the layout of the enclosure, the material that the enclosure will be made from can be considered (Table 3.19). The importance of the material chosen will contribute to the weight, physical & electrical protection and tools required to build. Microprocessor relays are found in laboratories but can also be brought out to the field to test protection systems. In the latter case, they can be exposed to a dirty environment and additionally could have physical damage caused to them in the chance they are dropped or knocked over. The components inside the relay will be required to stay undamaged in the event that the

box is knocked over. By choosing a material that will be resilient to the being dropped or the rugged environment, it will provide protection and increased resilience to the internal and items.

Additionally, the weight of the box will be important. Since it will be a testing device, it would be convenient for the relay to be relativity lightweight. This will factor into the material chosen so the relay is more readily available to be moved to the location of the power systems equipment location. Next, the thermal conductivity is considered for the factor of keeping components operating at an acceptable thermal level. By having a low thermal conductivity, the components the ability for heat dissipation will reduce. The ability to radiate heat to the enclosure provides another way for the thermal heat generated by the components to be removed. The exposure to the ambient temperature of the case, the heat inside can be transferred to outside of the enclosure. This will result in a lower internal temperature of the enclosure and a controlled environment inside.

Table 3.19 – Comparison of materials for enclosure

	Material			
Characteristic ↓	**Wood (Pine)**	**Plexiglass**	**Aluminum**	**Steel**
Thermal Conductivity ($\frac{W}{m-k}$)	~0.113	~0.17	~225.94	~13.38
Aesthetics	Simple to paint, easily changed	Clear aspect shows internal components	Special paint required, naturally bright metallic color	Special paint required,
Customizable	No special tools required	Can be cut with laser	Special tools required to cut/bind	Special tools required to cut/bind
ESD Protection	No way to be grounded.	Can be layered with static dissipative surface	Can be coated or grounded	Can be coated or grounded
Density ($\frac{Kg}{m^3}$)	~400.0	~935.0	~2650.0	~8030.0
Tensile Strength (MPa)	40	70	110	860
Dimensions (inches) & Estimated Cost	.20x23.74x48 $20.94	.125x12x12 $8.99	.375x6x6 $24.84	.375x6x6 $61.42

Another way to control the possibility of overheating, a cooling fan can be used to circulate the air. The circulation of air with a fan on an intake and an exhaust port, the immediate heat inside of the relay will be reduced as the it is taken out of the system. Without introducing the use of a heat sync for the components, cooling fans are a viable solution to controlling the internal temperature of the relay box.

Furthermore, the electrostatic discharge (ESD) is the sudden flow of usually high voltage from the build-up of charges. These voltages can discharge across sensitive components, compromising the integrity of the unit. ESD cannot be fully eliminated in electronics design but there are ways to reduce the chances the discharge will affect sensitive components. By selecting a material for the enclosure that can be grounded, the static charge that builds up is more likely to be discharged to the ground source instead of being discharged across the sensitive components.

By selecting wood for the enclosure, the advantages would include the easy manipulation of the material and by using pine, it would be light weight. By using the precision of a laser cutting tool provided by the Innovation Lab would, the enclosure could easily be crafted. But this comes also comes with the downfall of thermal heat. With a low thermal conductivity rating, there could be more heat inside of the enclosure and this would have to be either solved with a heat sync or adding additional cooling fans.

Next, plexiglass would provide a great advantage of also being cut by the laser cutter and also has the addition of having transparent. The transparent aspect would be a great way to display the internal workings of a microprocessor relay. This relay is built with the idea of teaching future power engineers on how the equipment they use every day and the impact it has. The plexiglass is relatively cheap but does not have a way of being grounded. Fortunately, there is materials on the market that provide a way to reduce ESD risk by providing a way to reduce any charge buildup on the enclosure. The material is similar to a laminate but still provides the feature of being transparent.

The aluminum enclosure has great thermal conductivity and provides a lightweight aspect if this material was chosen. The material requires a few tools to put together the enclosure which adds some difficulty to using aluminum. Aluminum can be grounded to provide the reduced ESD risk and is rather cheap when compared to other materials. Steel has the greatest protection to physical risks by providing strong resilience to any falling or being knocked. This material can also be grounded for ESD risks but does require a bit more consideration when altering. Steel is the most resilient out of the materials considered which means the tools required to alter the enclosure will be required to be more robust then the tools for the pine wood. The cost is also a more expensive but is often cheaper when bought in shapes pre-built. These pre-built boxes are often found for networking applications which are readily available. Another benefit is that these boxes are shaped for a relay rack and follow the standards in place for them.

Because most relay boxes are made from steel and are often mass produced, the cost of these pre-built boxes are lower than purchasing stock material. Since steel can also be thinner and still provide the resilience of aluminum, steel is a strong competitor for the enclosure. More consideration will be in place till further knowledge is acquired but for now, a steel enclosure will be chosen for the initial design selection.

Cooling: The cooling fans compared in table 3.22 would be utilized to circulate the air inside the enclosure providing a controlled environment for the components. Using the method of convection, the heat inside the case is carried outside by the circulating air. The advantage of adding a fan to the enclosure will ensure that the components do not overheat and operate at nominal temperatures. When components start to overheat, the accuracy of the output becomes skewed producing undesirable results. As a result of keeping the components at a reasonable temperature level, the relay is able to sustain the reliability of the device. Since most of these components are similar in the characteristics they provide, the power required, airflow and cost will be the major considerations.

The Eluteng brand offers one of more expensive fan options at the average air-flow and lowest power demand. This makes this cooling fan a viable option for the enclosure. One thing that must be considered is running the fan off a stepped down 5V power supply unlike the other brands demanding a 12V connection. This would require minimal changes for the power supply but would need to be considered when the power supply component is chosen. Next one brand to be addressed is the Artic Cooling fan. This fan comes with a small decrease in cost but comes with only 0.3W increase in power demand. The speed of the fan is a higher but still allows for a lesser noise level. This fan also comes with a steel enclosure for an added safety feature over the other fans.

After considering four different cooling fans that were possible solutions to the heating problem, one must be chosen for the initial design. When the Artic Cooling brand was compared it satisfied a lot of the criteria and provided the best economical choice. For these reasons and the reasons above, the Artic Cooling AF12PRO will be chosen for the initial design selection.

Table 3.20 – Comparison of cooling fans

	Component			
Characteristic ↓	Eluteng B075XGP994	Cooler Master R4-L2R-20AR-R1	Apevia CF312S-BK	Artic Cooling AF12PRO
Speed (RPM)	1000	2000	1500	1500
Voltage	5	12	12	12
Amperage	0.30	0.37	0.33	0.15
Power (W)	1.5	4.44	3.96	1.8
Size ($\boldsymbol{mm^3}$)	120x120x25	120x120x25	120x120x25	120x120x25
Noise Level (dBA)	27.0	19.0	24.7	22.0
Air-Flow (CFM)	54.56	69.69	57.67	54
Estimated Cost ($)	8.99	8.34	6.44	8.69

4. RELATED STANDARDS

The following standards have been identified as having relevance to the project at hand. Core component selection is still underway, making more a more precise discussion impossible at this time. As more exact methodologies are chosen, standards discussions will be expanded as necessary. For many standards, such as those for safety and electromagnetic capabilities, the practices are noted but not worked into the design specifications. This is due to the expensive and specialized equipment and environments required for actually demonstrating many specifications (e.g. high voltage impulse withstand). Instead, efforts have been made to create specifications that capture the spirit of the standards but are more easily verifiable (e.g. withstand a 150% overvoltage for 15 ms).

IEC 60255: Electrical Relays

Maintained by the IEC, the 60255 series of standards address many aspects of power system relay performance. They cover topics such as voltage, current, and frequency ratings. They also address accuracy requirements under normal operations as well as dynamic and transient conditions. It also contains test guidelines for evaluating many of these functions. Because of the breadth of topics covered under this standard, it can serve as an excellent of guidelines.

Impact of IEC 60255 on Design

Efforts are still ongoing to obtain access to this standard. However, once this access is obtained, many useful details regarding all aspects of PHATCAT's design will be available for extraction. It will be unlikely that the authors will have the resources necessary to provide feasibly demonstratable compliance with these standards, but they can serve as excellent guidelines for ensuring good engineering practice.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is a communication protocol, first developed by Motorola in the 1980s, that is frequently used for communications in embedded systems. Rather than being enforced by IEC or IEEE, it is a 'de factor standard'. In other words, it is so widely used and accepted that it is, for all intents and purposes, an enforced standard. An SPI consists of a master device and many slave devices. For our project, the microcontroller would act as the master, providing the clock that regulates the timing of information exchange. All peripheral devices would be slaves.

Impact of SPI on Design

For this project, SPI enables more than it constrains. It constrains electronics manufacturers to certain guidelines to allow designers to easily interface different devices. We are then downstream of the enforcement, so to speak, and reap the benefits of the standardized interface. We are constrained in the sense that we must abide by the pin mappings, etc. defined by the standard and ensure that devices we wish to interface using SPI are in fact designed to support such an interface.

Inter-integrated Circuit (I^2C) Bus

Like SPI, Inter-integrated Circuit Bus is a widely-used protocol for communication in embedded systems. It was invented in 1982 by Phillips Semiconductor, which is known as NXP Semiconductors today. As such, NXP maintains the specifications for the protocol. It is free to implement, but devices using it must pay a fee to obtain a slave address. Unlike SPI, it supports multiple master devices.

Impact of I^2C on Design

Similar to SPI, I^2C will enable us to interface our various integrated devices. The two will be compared in the 'Core Components and Parts Selection' portion of the paper, and a choice will be made. It would be used similarly to SPI, but multiple master devices (such as the ADC) may be included.

TIA-232 (RS-232)

TIA-232, commonly referred to by its original name of RS-232, is a standard for serial communications. It originated in 1960 with the Electronic Industries Association (EIA) and is currently maintained by the Telecommunications Industry Association (TIA). This may be used to facilitate communications between the microcontroller and the PC for PHATCAT's configuration functionality.

Impact of TIA-232 on Design

Using serial communications may constrain the design somewhat as many computers (e.g. slim form-factor laptops) no longer support serial connections. A chosen microcontroller must support serial communications (i.e. it must have a UART). It will be desirable to make the communication work with a commercially available serial-to-USB solution such as the many converter cables available online today, so as to make PHATCAT compatible with a wide range of PCs.

Universal Serial Bus (USB)

Universal Serial Bus is a communications protocol that was first supported by Intel in 1996, though many other companies such as Microsoft, Apple, Hewlett-Packard, Nokia, and Phillips have all played a role in its development. It is currently maintained by the USB Implementers Forum (USB IF). It is intended for communications between a PC and its peripheral devices. In our project, PHATCAT would be a peripheral of the user's PC.

Impact of USB on Design

The biggest impact of using USB is the requirement that the microcontroller in fact supports USB; this is not always the case. Overall, this would serve to enable more compatibility with many modern devices, and enables more than it constrains.

5. Real-World Design Constraints

There are some constraints placed upon the development of PHATCAT that do not pertain to those resulting from physical laws or the project's main objectives. Stemming from real-world causes, these constraints are detailed below.

5.1 Economic Constraints

First, the economic constraints present in the microprocessor relay industry are discussed and related to the constraints present on the project. Microprocessor relays are typically much cheaper than the assets they protect and the scenarios they prevent. An older, simpler model of a transformer protection relay might cost a little over $2000. A new, state-of-the art relay might cost as much as $10,000. But this is dwarfed when compared to the costs of major equipment and outages. A 30MVA distribution transformer, for instance, costs on the order of $600,000, sixty times of the cost of even the most advanced transformer relay. The risk total asset loss is not the only cost factor. In order to justify its cost, the transformer must aid in the delivery of power for a certain service lifetime. Each fault the transformer is exposed to decreases its life. As such, the speed of the protection system also plays a vital role in decreasing the costs associated with fault occurrences.

Much of Florida's distribution takes place at 13kV on equipment rated for 600A, giving its distribution lines a rule-of-thumb capacity of 13 MVA. Allowing for a poor power factor, a distribution line might be said to deliver 10 MW. In Florida, electric energy costs ~12 cents per kWhr. If improper protection causes one of these lines to go out of service for even an hour, $1200 in revenue alone is lost, without even mentioning the costs associated with the location and repair of the faulted equipment. A distribution transformer might supply four or five such distribution lines, further increasing this cost. Even these costs can be dwarfed by those imposed by regulating bodies when utilities have serious mis-operations or fail to meet certain standards for quality of service.

Furthermore, the cost of the relay itself only represents a portion of the cost associated with deploying it for protection. Engineers must be paid to create the wiring schematics and perform fault studies to customize the relaying functions for the application. Skilled technicians must be paid to wire up and test the complete designs. System operations must make and execute arrangements to sustain the equipment outages required for the construction and commissioning process.

With all of these concerns under consideration, it is clear that the economics of using microprocessor relays for protection and control are not primarily driven by the costs associated with the relays themselves. If a $10,000 relay is chosen instead of a $2000 relay for use on 75 distribution transformers and preserves even one transformer from a situation that the $2000 could not, money will be saved. The savings realized by faster trip times and reduced mis-operations are more distributed throughout the system, but the economics are easily justified. It is common practice among utilities to use two or even three simultaneous protective relays operating in parallel to further reduce the chance of a protection failure.

Due to these factors, our project does not focus so much on selecting the cheapest components that can perform the task. Rather, we focus on selecting components that are robust and unlikely to limit the performance of other components. However, note that, due to the time, labor, and experience available to the project team, a reliability and robustness comparable to market offerings will not be feasible. Current market offerings are the result of top experts spending millions of dollars honing platforms for decades. These offerings are hardened against temperature, ESD, EMI, and seismic conditions and feature robust self-test features that continually monitor functions and report failures. Instead of trying to meet industrial standards of performance, specifications have been appropriately curtailed to be achievable within the team's constraints.

5.2 TIME CONSTRAINTS

The time constraints placed upon this project affect the specifications more than perhaps any other realistic design constraint. It is essential for the authors to meet the milestones for project documentation and prototyping. If these milestones are missed, the course may be failed. This would result in utter termination of the project—a new project and team would have to be selected for the next attempt. Not only does this jeopardize the author's GPA and graduation date, but it may impact their future career. All authors have plans to enter the workforce full-time upon graduation, and failure to graduate by the planned date may result in the destruction of these plans. While failure is a highly improbable scenario, its seriousness should be stated and considered heavily in the scoping process.

There are several options for mitigating the risk of violating time constraints. The first is the procurement of skilled guidance. Dr. Chung Yong Chan has agreed to serve as a mentor throughout the project process. With his extensive technical background and experience guiding students through senior design, his counsel, if followed, will prevent serious missteps and serve to keep authors on the proper path. The second is the setting of aggressive early milestones and the utilization of all spare time. One of the biggest challenges in senior design is that of the unknown—what works in a Matlab simulation may be unreproducible in a laboratory setting. Practical milestones should be set earlier than the required so as to allow for such contingencies. This deviation between the theoretical and practical highlights the third option: the thorough research and technical understanding of the implementations used. There are many professional-grade ICs and reference designs available for the project's various components. These will streamline the design process, but they hold a hidden trap. If the authors do not properly understand what it is they are selecting, how it functions, how to modify it, and how it interacts with other components, integration will be difficult and perhaps even impossible. It is key for authors to have the proper knowledge so as to avoid lengthy troubleshooting and time-consuming redesign.

5.3 SAFETY CONSTRAINTS

Safety is a paramount virtue at electric utilities. While protection and controls engineers spend much of their time in a relatively safe office environment, they occasionally venture out to visit generation plants and substations where even a few careless moments can result in a life-altering injury. This risk is heightened by the fact that a site visit is a break in the usual routine. Protective relays can mitigate the dangers present in these types of locations in several ways.

The first and most obvious way relays protect personnel is by rapidly clearing power system faults. During a ground fault in a substation, a large amount of current is injected into the earth. As a result, large voltages develop. This presents a serious shock hazard for any personnel who might be located in the yard at the time of the fault. To reduce this risk, a comprehensive grounding study is conducted for every substation that is built and a network of underground conductors is used to reduce the voltages that develop. But these voltages can never be reduced to absolutely zero; it is still vital that protective relays operate quickly to reduce the harm sustained by anyone who may be shocked. This further supports the speed-related specifications of our relay.

Another way a well-designed relay will protect personnel is by its hardening against human performance error. This achieved in two ways. The first is the requirement of two-factor action for activating any buttons on the front of the relay. This prevents accidental operation if someone were to bump into or lean against the relay. Accidental operations bear significant hazard not only for system reliability, but for personnel safety. Due to the tremendous amount of energy at play, when power systems equipment fails, it typically does so in spectacular fashion, with shards of metal and ceramic cutting chunks out of solid concrete. As such, an accidental operation might take place when personnel are very near this equipment, presenting awful risk. The second method of combating human performance is through flexibility of the relay interfacing. A utility might use dozens of different relay models across its various applications. The greater the uniformity in the way relay technicians interact with these relays, the less likely it is for them to make

a mistake. Since a relay manufacturer has many different customers, each with their own preferences and practices, they need to make the way the technicians interact with the relays customizable. This drives our LED and pushbutton functionalities to be user-programmable.

5.4 Environmental, Sustainability, and Sociopolitical Constraints

Many of the challenges surrounding modern day power systems are embroiled in sociopolitical issues with environmental and sustainability as their focus. This controversy mostly revolves around the way in which power is generated. Some believe a rapid change over to fully renewable sources such as wind and solar is key to preserving the health of our environment. Many at utilities believe this technology to be insufficiently reliable. In countries with the proper natural resources, such as the US, natural gas has been increasingly looked to as a replacement for coal. Other European countries, such as Germany, that rely heavily on other countries for natural gas reserves, are investing heavily in renewables. Others, such as France, are doubling down on nuclear energy, which, despite its representation in popular culture, is both carbon neutral and the second safest form of energy (per MWh), following hydroelectric [5.1]. All over the world, intense discussions are ongoing with regards to the proper balance between environmentalism and pragmatism. It is not uncommon for either side of the issue to misunderstand limitations of their position from a technical standpoint.

The most relevant aspect of these challenges to the field of protection and control are those presented by the integration of renewables. Due to both their complex fault responses and distributed nature, renewable generation requires vastly more robust schemes in portions of the grid (e.g. distribution) where, previously, very simply schemes sufficed. Much research is ongoing in the field of microgrids and more distributed methods of system control that can tackle these emerging issues. UCF has developed a microgrid control laboratory and many of its graduate students and faculty are researching the various challenges associated with a power grid driven by distributed resources. One hallmark of these solutions is their reliance on modern communications systems. As we saw in the market analysis, modern relay manufacturers see this reliance and are moving forward to provide ever more robust devices capable of functioning in such applications. But with the inclusion of these new communications systems, another sociopolitical constraint reveals itself.

Utilities have been facing a growing cyber threat, with malicious entities regularly striving to penetrate and disrupt their systems. Even the power grid, as it is today, is not impervious to these attacks [5.2] and increasing the system's dependence on modern communications is sure to only increase the potential impact of a serious compromise. So, while a need for sustainable, renewable energy is driving more complex and robust protection and controls systems, a growing threat of cyber-terrorism is heightening the risks associated with implementing the required technology.

It is very common for senior design projects to include Bluetooth or Wi-Fi interactivity in their projects, in keeping with current industry trends (e.g. 'Internet of Things'). However, the sociopolitical constraints associated with this project illustrate that such features should not be present in microprocessor relays. Even a hard-wired connectivity with any LAN would have to be extremely secure, and its proper implementation would expand the scope of the project so as to violate the time constraints.

One other sustainability constraint worth noting is that of part availability. In a professional setting, those in charge of procurement should work with parts manufacturers to ensure the lifetime availability of chosen components is not shorter than the desired product life cycle or, at the very least, that future offerings will be compatible with the product. For this project, the key is to avoid purchasing parts early on in the Senior Design process that may be unobtainable later on. In the worst-case scenario, issues might manifest themselves in the form of last-minute redesign required after a now unavailable part malfunctions. As such, this project will avoid using parts that are obsolete or marked as 'not for new design' by manufacturers or suppliers.

6. System Hardware Design

In the System Hardware Design section, the core components and approaches developed for PHATCAT are implemented in fully-functional schematics. Their operation is briefly explained as necessary and bills of material for each schematic are provided.

6.1 Overvoltage Protection Design

The baseline design for PHATCAT's overvoltage protection circuitry is given in fig. 6.1. D1 is a bi-directional TVS diode that is chosen to limit V_{out}^{+} - V_{out}^{-} to below the absolute maximum rating of the protected circuit (e.g. ADC inputs, GPIO). This protects against high differential-mode input voltages. However, it is feasible that there may be a large common-mode input voltage, in which case D1 will not turn on. D2 and D4 protect V_{out}^{+} and V_{out}^{-} respectively by limiting them to $V+_{MAX}$ + V_D. D3 and D5 function similarly, instead providing the lower bound. R1 and R2 limit the current flowing through the diodes during an overvoltage. Note that the use of D2-D5 limits the ability to use diodes designed to work in the reverse-breakdown region. They would become forward biased for normal operation if applied here (the diodes would be flipped in orientation). Furthermore, these limits are typically something along the lines of V_{cc} + 0.3V, so a small breakdown voltage will be desirable.

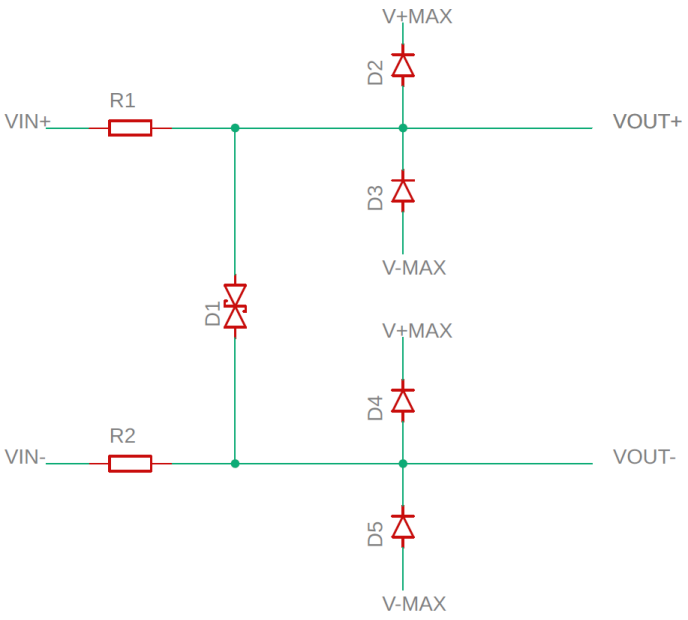


Fig. 6.1 Baseline overvoltage protection design. Produced with EAGLE by B. Ross.

There is one important thing to note regarding the application of this design to PHATCAT's input and outputs. The use of R1 and R2 is only acceptable for protected devices having a high input impedance, if any current flows through R1 and R2 during normal operation, there will be undesirable voltage drop. Because the voltage limits vary throughout the project, the exact diodes will be chosen on an individual basis and the selected components captured in the BOMs for those portions of the design.

6.2 Current-Sensing Design

In fig. 6.2, the layout of the analog current inputs is shown. There will be two Zener diodes used for the differential over voltage protection and one for the common mode over voltage. The capacitors cascaded after the sense resistor will provide denoising before the signal is transmitted to the analog-to-digital converter. L1-L8 are the current transformers which will be mounted inside the enclosure but in to conserve cost and space, they will not be mounted on the PCB. Therefore, L1-L8 are just place holders for the schematic for clarification of design. Table 6.1 provides the bill of materials (BOM) which will be utilized to build the current sensing schematics.

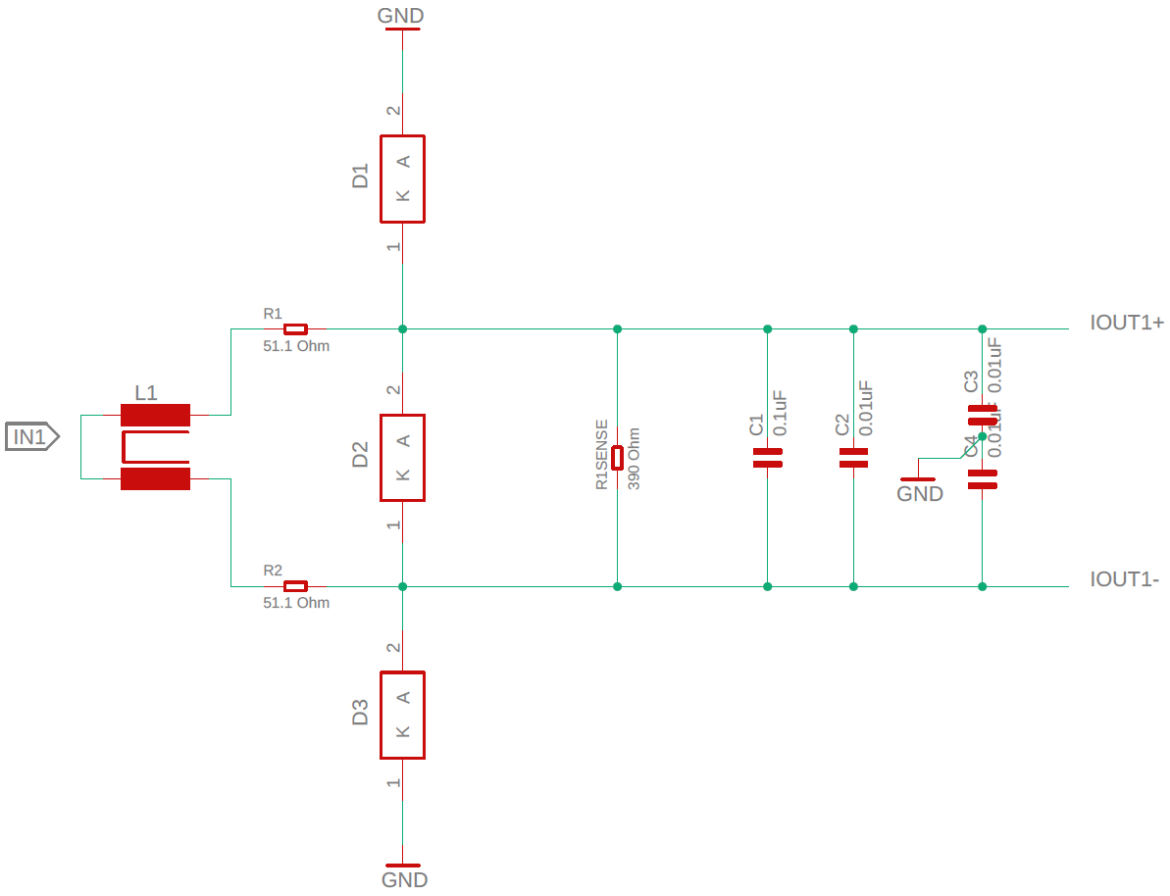


Fig. 6.2 Current Sensing Schematic

Table 6.1 - Current Sensing BOM

Manufacturer Part #	Qty	Manufac.	Description	Cost
SMAJ10CA-E3/61	24	Vishay	ESD Suppressor, TVS Diode 400W 10V	$6.43
SFR2500005119FR500	16	Yageo	RES 51 OHM 1% 2/5W 1206	$1.96
CRCW0805390RFKEAHP	8	Vishay	RES SMD 390 OHM 1% 1/2W 0805	$3.60
AC0603KRX7R9BB104	8	Yageo	MLCC - SMD/SMT 0.1uF 50V 10%	$2.30
AC0603KPX7R9BB103	24	Yageo	MLCC - SMD/SMT 0.01uF 10% 50V	$1.20
CR8350-2500-N	x8	CR Magnetics	100A Current Sense Transformer	$133.60
			Total Cost:	$152.66

6.3 VOLTAGE-SENSING DESIGN

In fig. 6.3, the layout of the analog voltage inputs is shown. There will be two Zener diodes used for the differential over voltage protection and one for the common mode over voltage. The capacitors cascaded after the load resistor will provide denoising before the signal is transmitted to the analog-to-digital converter. TR1-TR6 are the voltage transformers which will be mounted inside the enclosure but in to conserve cost and space, they will not be mounted on the PCB. Therefore, TR1-TR6 are just place holders for the schematic for clarification of design. Table 6.2 provides the bill of materials (BOM) which will be utilized to build the voltage sensing schematics.

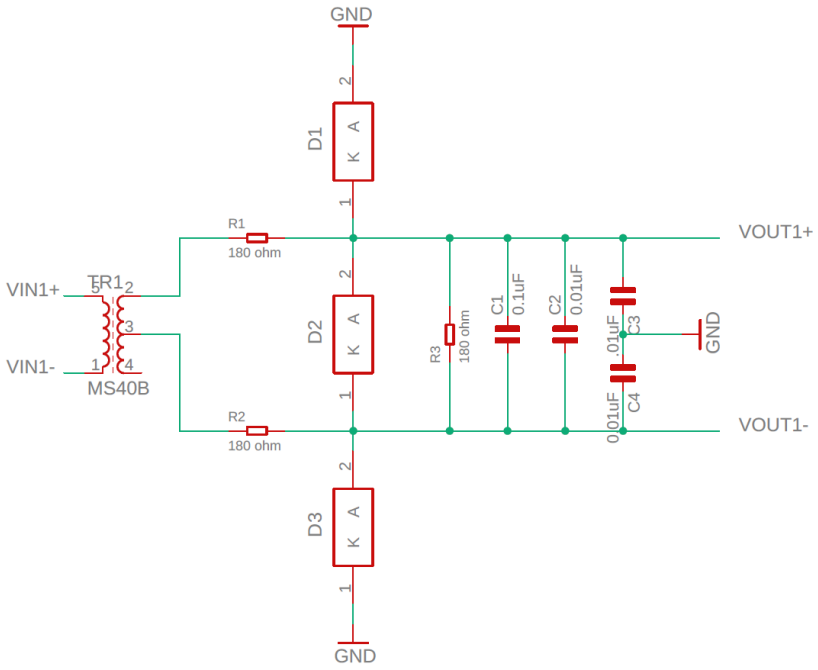


Fig. 6.3 Voltage Sensing Schematic

Table 6.2 - Voltage Sensing BOM

Manufacturer Part #	Qty	Manufac.	Description	Cost
SMAJ10CA-E3/61	24	Vishay	ESD Suppressors / TVS Diodes 400W 10V	$6.43
ERJ-8GEYJ181V	24	Panasonic	RES SMD 180 OHM 5% 1/4W 1206	$3.01
AC0603KRX7R9BB104	8	Yageo	MLCC - SMD/SMT 0.1uF 50V 10%	$2.30
AC0603KPX7R9BB103	24	Yageo	MLCC - SMD/SMT 0.01uF 10% 50V	$1.20
F20-055-C2	x6	Triad Magnetics	115V Voltage transformer	$38.93
			Total Cost:	$55.44

6.4 ADC DESIGN

In the fig. 6.4, the layout for the analog to digital converter is shown. This layout includes the components and schematic that is going to be implemented for the ADC. The 16 analog inputs are shown on the left side with noise decoupling capacitors and current restricting resistors. The digital outputs are on the right side with breakout pins to be connected to the developer board. This schematic will be duplicated to include all 14 inputs from the analog and eventually included in the main PCB layout. Table 6.3 includes the BOM for the ADC schematic and the components that will be used for the design.

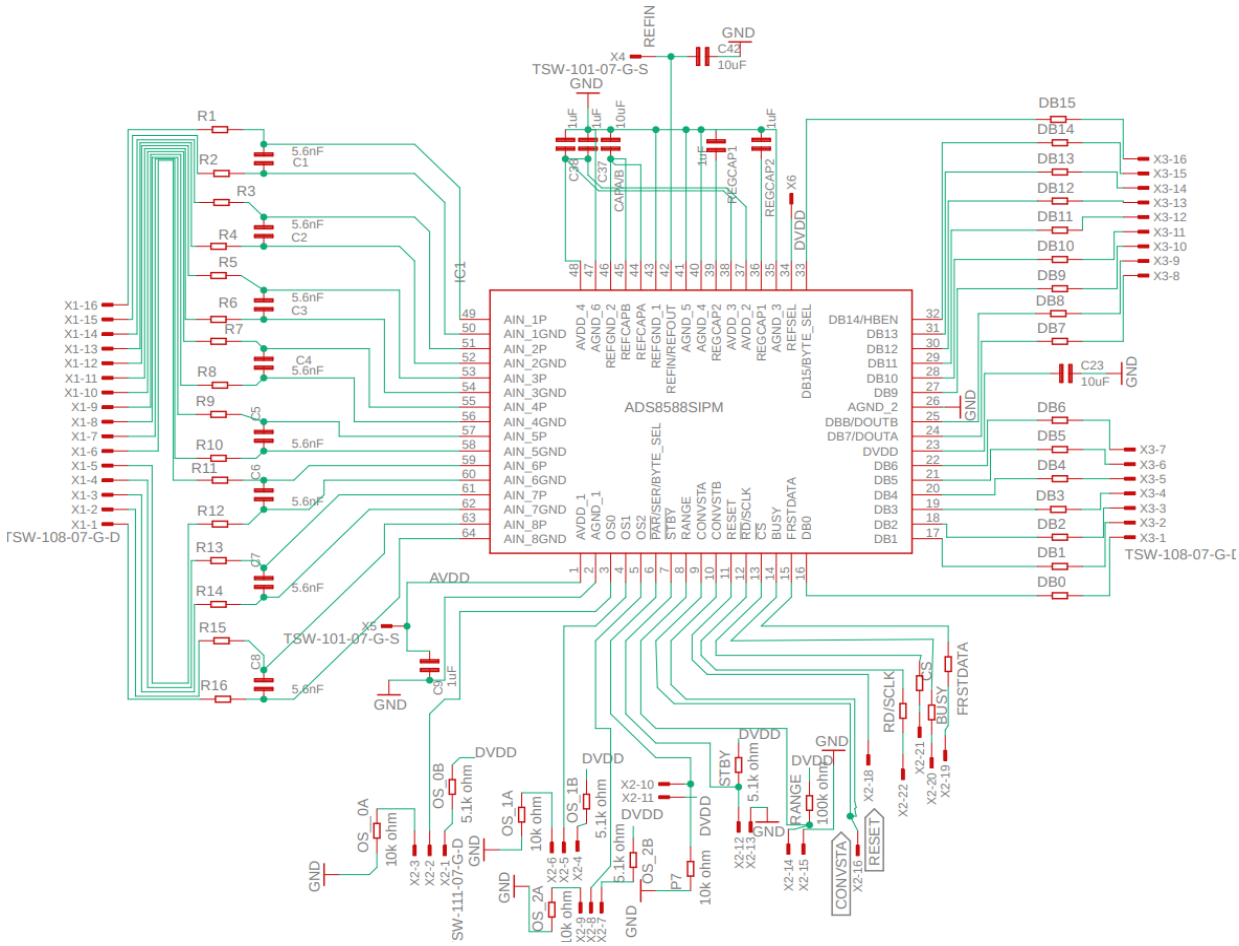


Fig. 6.4 ADC schematic

Table 6.3 – Analog to Digital BOM

Mfr #	Qty	Manufac.	Description	Cost
SDR03EZPF4301	16	ROHM Semi.	Resistors, SMD 0603 4.3Kohm 1%	$1.82
RCS060310K0JNEA	3	Vishay	Resistors, SMD 0.25W 10Kohms 5%	$0.42
RCS0603100KJNEA	1	Vishay	Resistors, SMD 0.25W 100Kohms 5%	$0.14
RCS060349R9FKEA	20	Vishay	Resistors, SMD 0.25Wt 49.9ohms 1%	$2.28
RCS06035K10FKEA	4	Vishay	Resistors, SMD 0.25W 5.1Kohms 1%	$0.56
C1608C0G2A562J080AE	8	TDK	Ceramic Capacitors MLCC - SMD/SMT 0603 100V 5.6nF 5%	$2.40
CL10A105KB8NNNC	5	Samsung	1µF ±10% 50V Ceramic Cap X5R 0603	$3.40
GRM188R6YA106MA73D	3	Murata Elec.	Ceramic Capacitors MLCC - SMD/SMT 0603 10uF	$1.47
ADS8588SIPMR	3	Texas Inst.	ADC 16-Bit High-Speed 8-Channel	$22.08
			Total:	$27.68

6.5 Output Contact Design

The schematic shown in fig. 6.5 is designed such that if the protective algorithms pertaining to the output contacts within the relay read “NOT TRUE”, then the microcontroller would output a low voltage signal of 3.3V through a 806 ohm resistor into the optocoupler. The optocoupler would then switch on the circuit controlling voltage across and current through the coil of the EE2-12NUH-L Relay. The magnetic field generated by the current passing through the coil would cause the armature of the relay to open the normally closed contacts and close the normally open contacts. The relay circuit is connected across the normally open contacts so that when the contacts are closed, current would begin to flow through the relay contact circuit and accomplish what is designed to, which typically would be to activate the coil of a breaker in a substation to break the contacts of a high voltage circuit.

The output contact schematic also included some protective measures that were taken. A protection diode was placed in parallel with the coil of the relay to help dissipate the energy of the sudden collapse of the magnetic field that was initially generated by the current through the coil. A RC snubber circuit was placed in parallel with the relay contacts in order store the energy from the sudden collapse of the inductive circuit using a capacitor to extend the life of the relay contacts and do away with arcing that could occur across the contacts. The Output Contact Circuit material is listed below in the BOM (Table 6.4).

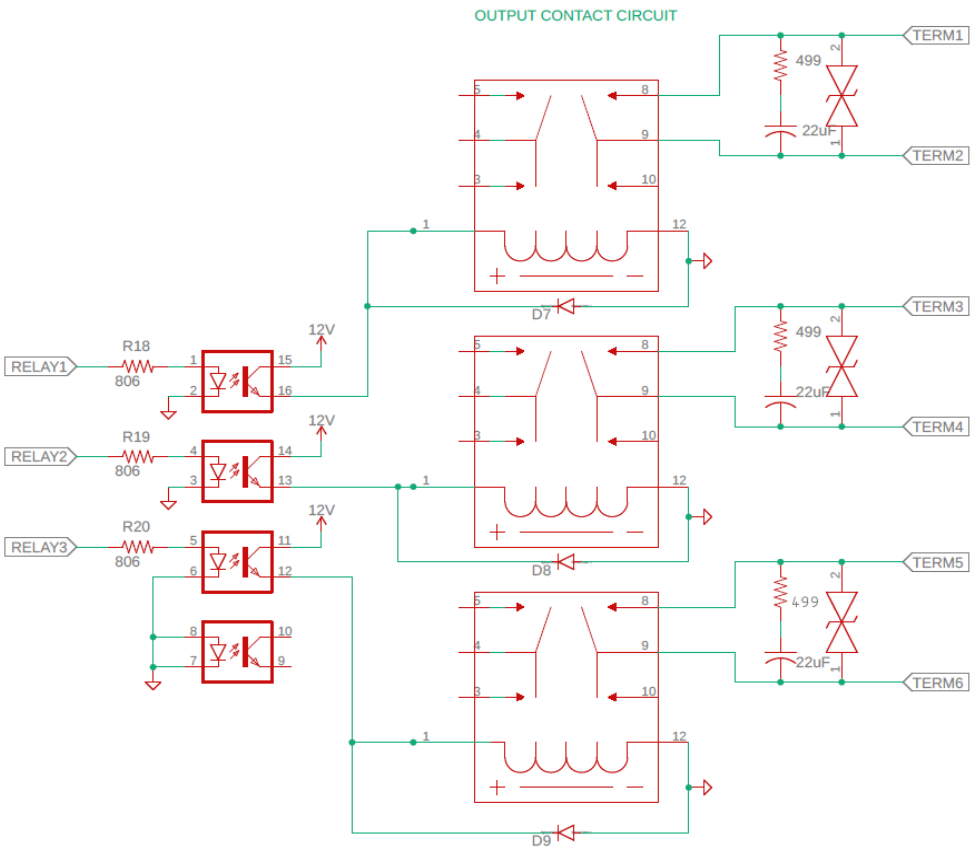


Fig. 6.5 Output Contacts Circuit Schematics. Created by Ed Millet with Eagle.

Table 6.4. BOM – Output Contact Circuits

QTY	ITEM	MFR#	COST
3	RELAY GEN PURPOSE DPDT 2A 12VDC	80-EE2-12NUH-L	$13.32
1	TRANSISTOR OUTPUT OPTOCOUPLERS	ILQ2-X009T	$6.44
2	TERM BLOCK PLUG 24POS	TE-1658621-5	$4.68
2	TERM BLOCK HDR 24POS	TE-5499910-5	$9.66
1	CBL RIBN 24COND 0.050 GRAY 1’		$3.40
3	RES 806 OHM 1% 1/4W 1206	ERA-8AEB8060V	$1.98
3	RES 499 OHM 1% 1/4W 1206	ERA-8AEB4990V	$3.30
3	CAP CER 22 UF 50V C0G/NP0 1206	GRT31CC81C226KE01L	$1.89
3	TVS DIODE 136V 219V DO214AA	P6SMB160CA-E3/52	$1.59
3	DIODE GEN PURP 1KV 1A	CGRKM4007-HF	$1.59
		TOTAL COST:	$47.85

6.6 LED INDICATOR DESIGN

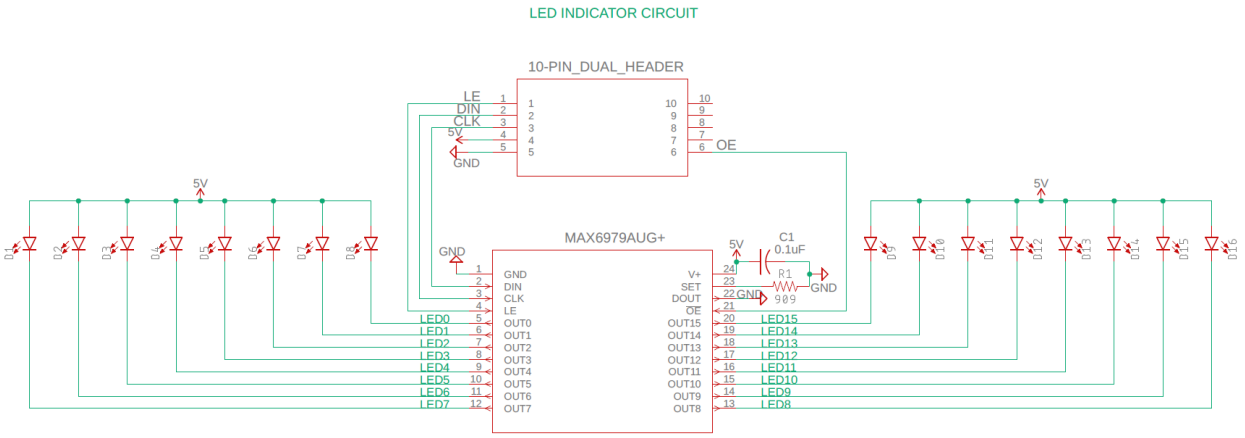


Fig. 6.6 LED Indicator Circuit Schematic

The LED Indicator circuits (fig. 6.6) are designed using the MAX6979AUG LED Driver. The LED Indicator circuit will be mounted to the front panel of the relay on its own PCB board. Using a 10-Pin Dual Header, the serial communication will be established to the microcontroller on the main board. The power and ground for the LED board will be supplied by the microcontroller. The microcontroller will send 16 bits of data to the LED driver that will be shifted in and latched using a clock signal. The data will be output using an output enable pin. The data that is output will determine which LED is turned on or not. A single 909 ohm resistor is used to keep constant current close to 20mA. A 0.1 uF bypass capacitor is used from the source to ground of the LED Driver to minimize the effects of noise or interference from other elements or circuits in the relay. The LED Indicator Circuits will be used to indicate the type of fault that occurred, protection algorithms that were deployed, and breaker statuses. The components required to build the circuit is given in Table 6.5

Table 6.5 BOM – LED Indicator Circuits

QTY	ITEM	MFR#	COST
1	LED Lighting Drivers 16Port 5.5V Constant Current	MAX6979AUG+	$7.35
16	Standard Red LEDs - SMD	SML-S13VTT68	7.84
1	RES SMD 909 OHM 0.1% 1/4W 1206	ERA-8AEB9090V	$0.66
1	Multilayer Ceramic Capacitors MLCC - SMD/SMT .1UF 50V 5% 1206	CC1206JRX7R9BB104	$0.25
1	TERM BLOCK PLUG 10POS	TE-1658621-1	$1.17
1	TERM BLOCK HDR 10POS	TE-5499910-1	$2.12
		TOTAL COST:	$19.39

6.7 SENSE INPUT DESIGN

The Sense Input Circuits (fig. 6.7) were designed in such a way to reduce the voltage of the circuit to 5V by going through a 56k ohm resistor. The resistor power rating was increased to 1/2W to be able to handle the heat dissipation that will occur. The 5V will then go through 2.8k ohm resistor into the optocoupler which is isolating the higher voltage circuit from the microcontroller. When the optocoupler is switched on, using a pull-down 3.3k ohm resistor the microcontroller will then read “HIGH”, thus sensing the input across Terminals 1 & 2. The required components are given in table 6.6.

Table 6.6 BOM – Sense Input Circuits

QTY	ITEM	MFR#	COST
1	TRANSISTOR OUTPUT OPTOCOUPLERS	ILQ2-X009T	$6.44
3	RES 3.3K OHM 1% 1/4W 1206	ERA-8AEB332V	$1.98
3	RES 2.8K OHM 1% 1/4W 1206	ERA-8AEB2801V	$1.98
3	RES 7.1K OHM 5% 1/4W 1206	ERA-8AEB7151V	$1.98
3	CRGP 1206 56K 1%	CRGP1206F56K	$0.99
3	TVS DIODES 10V 500W 44A	SMBSAC5.0-TP	$3.03
		TOTAL COST:	$16.04

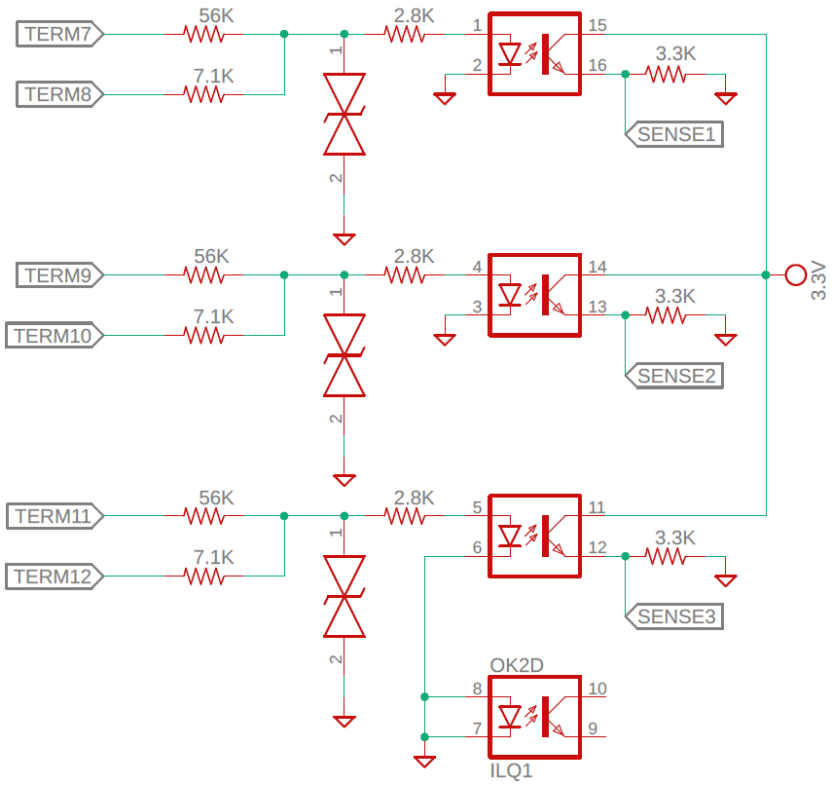


Fig. 6.7 Sense Input Circuit Schematic. Created by Ed Millet with Eagle.

6.8 PUSH-BUTTON DESIGN

The push button schematic (fig. 6.8) is designed to power on the circular white LED ring of the push button all the time by using a 12V source in series with a 422 Ohm resistor. The push button circuit uses the charging of a capacitor to read into the microcontroller whether the push button has been pressed or not. The resistors of 36k and 24k ohms, plus the capacitor of 0.01 uF were selected so that when the push button was pressed and released the capacitor would discharge in 1.5ms through R2 and charge through both R1 and R2 in 3ms. The total time for discharge and charge equaling 4.5ms. Understanding and knowing the total time for the capacitor to discharge and charge back up again allows for accurate programming of the microcontroller to read in the status of the push button.

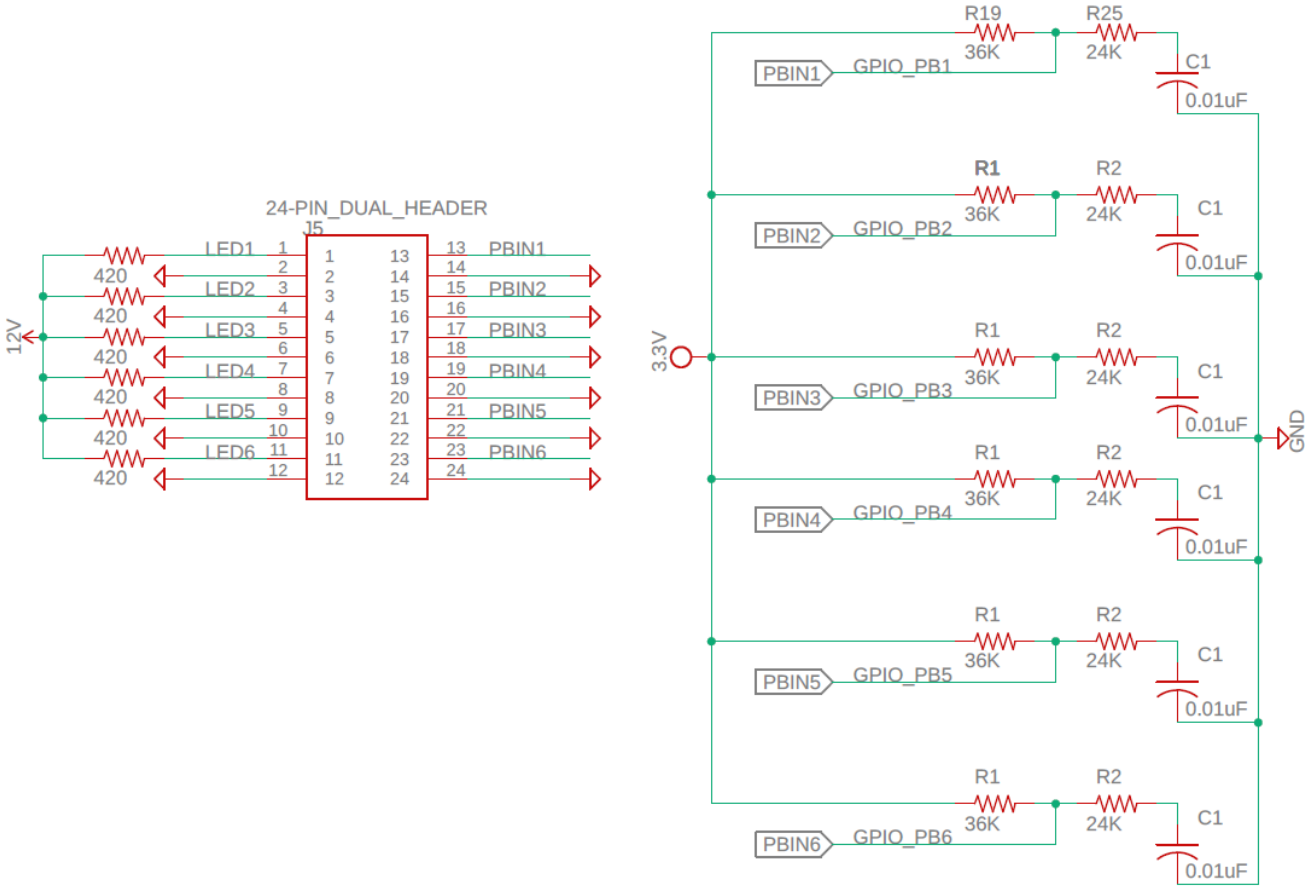


Fig. 6.8 Push Button Circuit Schematic

Table 6.7 BOM – Push Button Circuits

QTY	ITEM	MFR#	COST
6	PVA6LRE21241 SWITCH PUSHBUTTON	PVA6LRE21241	$73.50
2	TERM BLOCK PLUG 24POS	TE-1658621-5	$4.68
2	TERM BLOCK HDR 24POS	TE-5499910-5	$9.66
1	CBL RIBN 24COND 0.050 GRAY 1’		$3.40
6	RES SMD 422 OHM 0.1% 1/4W 1206	ERA-8AEB4220V	$3.96
6	RES 24K OHM 1% 1/4W 1206	ERA-8AEB243V	$3.96
6	RES 36K OHM 1% 1/4W 1206	ERA-8AEB363V	$3.96
6	CAP CER 0.011UF 50V C0G/NP0 1206	CC1206JKNPO9BN103	$3.00
		TOTAL COST:	$106.12

6.9 MICROCONTROLLER DESIGN

The Texas Instruments C2000 Delfino MCU F28379D LaunchPad development kit is used in order to initially test and set up hardware and software applications for the PHATCAT Project. The schematic and board layout CAD files have been requested and obtained from Texas Instruments (fig 6.9). The CAD files have been uploaded into Eagle in order to modify the following design to better fit and meet the needs of the project. The modification to the following design will include the removal of all unnecessary circuits and components that will not benefit or contribute to PHATCAT. The schematics that were designed for PHATCAT will be implemented into the following schematic design and updated using the same block diagram organization with new sheets referencing the incorporated schematics.

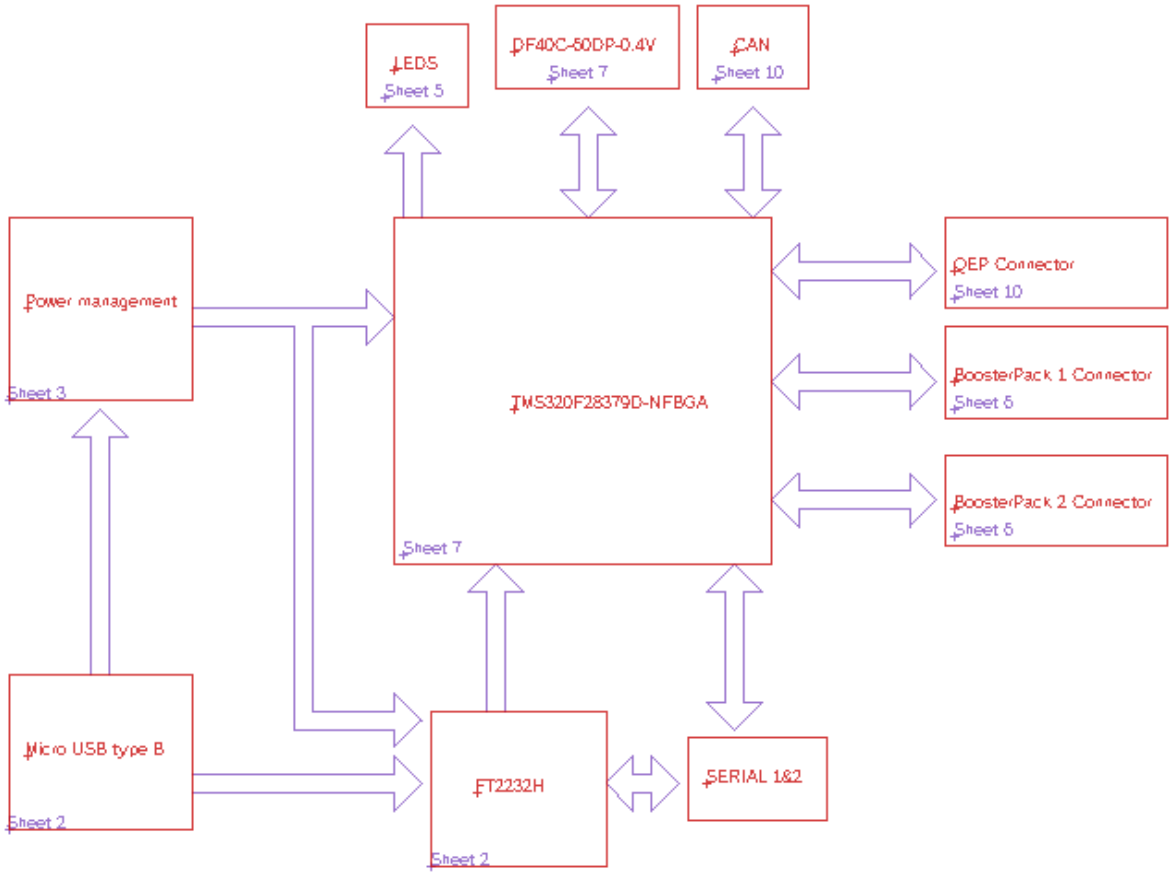


Fig. 6.9 TMS320F2837xD Dual-Core Delfino Microcontroller Block Diagram. Reproduction permission requested from Texas Instruments.

6.10 Power Electronics Design

The design in fig 6.10 is used to take the 12V output from the RS-15-12 and use it to provide +12V, +5V, and +3.3V for PHATCAT's hardware. A flyback diode, denoising capacitors, and a heatsink (not shown) are used for the 5V linear regulator. An EMC filter is used with the switching regulator. The 2-pin header is connected to the +12V output of the RS-15-12. This is the point where PHATCAT connects to earth (the RS-15-12 provides grounding continuity to the 120VAC receptacle). Table 6.8 provides a bill of materials for the design.

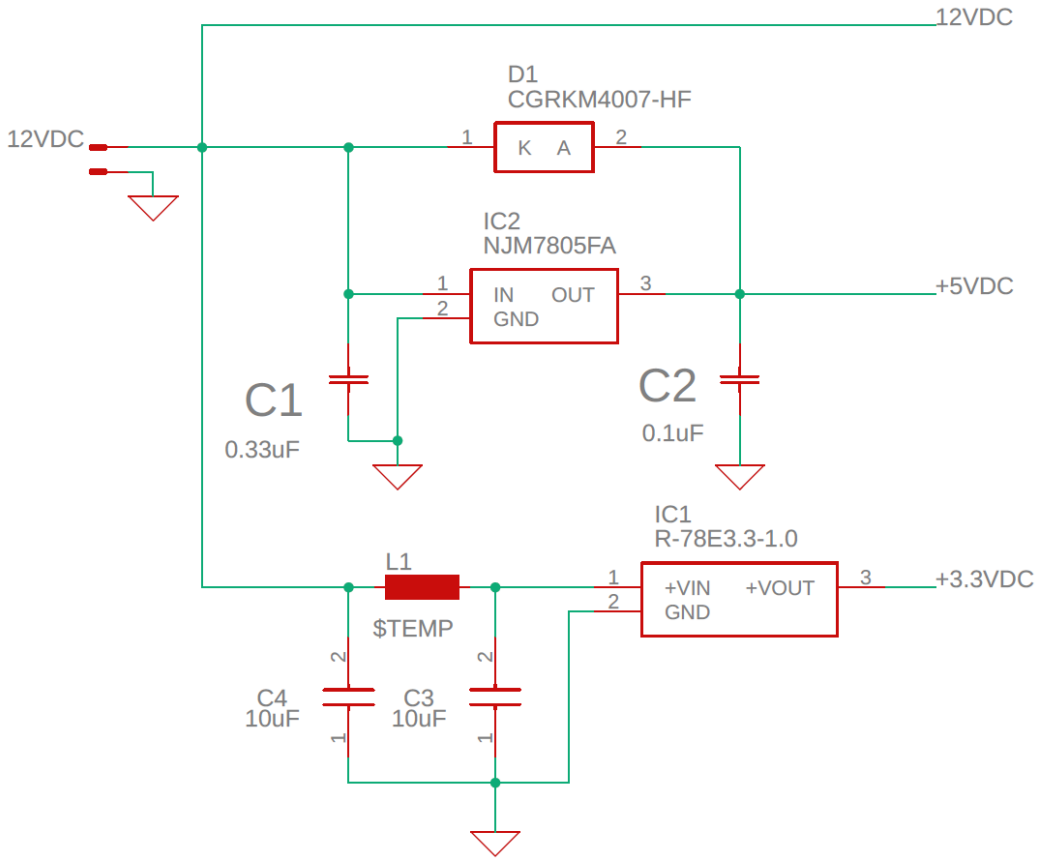


Fig. 6.10. Power Electronics Design

Table 6.8. BOM – Power Electronics

Item	Quantity	Cost
Meanwell RS-15-12 Power Supply	x1	$9.55
KK® 254 Solid Header 22-23-2021	x1	$0.17
NJR Corporation/NJRC NJM7805FA	x1	$0.88
Aavid 6237BG Heatsink	x1	$1.28
Samsung CL21B334KBFNNNE, 0.33uF, 50V, Ceramic Capacitor	x1	$0.19
Samsung CL10B104KB8NNNC, 0.1uF, 50V, Ceramic Capacitor	x1	$0.10
DIODE GEN PURP 1KV 1A CGRKM4007-HF	x1	$0.36
Recom Power R-78E3.3-1.0	x1	$3.26
TDK Corporation C5750X7S2A106K230KB, 10uF, 100V Ceramic Cap	x2	$2.11
Recom Power RLS-126, 12uH Choke	x1	$0.61
	TOTAL COST:	$18.51

7. SYSTEM SOFTWARE DESIGN

In the System Software Design section, the signal processing and software tools chosen in the core components portion of the paper are used to realize PHATCAT's software. The functionality and behavior software is detailed.

7.1 PHILOSOPHY AND DEVELOPMENT ENVIRONMENT

Design Methodology: The software design methodology is used to structure plan and control how the software will be created. There are several different design methodologies. Some of these methodologies will be discussed and one will be selected after examining their pros and cons. This methodology will be used in all aspects of software creation done for the PHATCAT device.

One such methodology is Waterfall which is the traditional method of software development and was one of the original methods of doing it. In this method the process is rigid and follows a linear path that is very difficult to back track on. Once one step is complete it will not be returned to again. In theory this deign should make it easy to set time deadlines on goals and should make it easier for managerial roles to keep track of progress. In practice however, the waterfall method generally has problems due to its inability to go back and correct issues experienced earlier in development [7.1].

Spiral methodology is a methodology that functions by continually going through a circular process. In the circular life cycle the identifications of risks that will be involved is paramount. It requires a lot of up-front time to develop the plan and special management to implement it. This design is generally used for very large-scale projects with large teams. Making it less than ideal choice for the project [7.2].

Agile development focuses on breaking the project into smaller chunks called iterations. These can vary in length from a week to several weeks. After each of these iterations a small working part of the project is completed and then evaluated. After evaluation it can be modified to better suit the need or move forward with another chunk of the project.

There are sub methodologies that are derived from Agile. These are called Crystal Method, Dynamic Systems Development Model (DSDM), and Scrum. The Crystal Method is an Agile development that will split groups into team that have a lot of communication between them but are self-contained. The idea behind this method is that each team has its own set of talents and are better left to their own devices. The small size of our team makes it difficult to split into fragmented teams, so this methodology is unusable [7.3]. The team does, however, have a diverse set of skills that will be called upon as the project progresses. DSDM is built on the idea that development is an exploratory endeavor. It builds rapid chunks of the project and has a lot of user involvement in fine tuning the product. The methodology is for large scale productions and is not easily to implement in small teams. Making this methodology is unusable as well. The Scrum process is an Agile process that has a log of tasks to complete. It also uses brief routine meetings that will be used to discuss the project and decide how to proceed.

There are many more methodologies that could be discussed. However, the small scale of our project and the size of the team make most of the methodologies non-ideal. After examining the methodologies, the best fit for the PHATCAT is Agile Scrum development. The brief scrum meetings will be useful in making sure the group is on track to complete the tasks assigned to each member. These meetings will happen weekly with our Mentor and routinely amongst the team. This process will be used in software development as well as designing hardware and writing the documentation. A web-based software application Asana will be used to keep track of the team and their progress.

IDE: The integrated development environment is a crucial part of all software development. It is a special program that is designed to be a platform to build and test software that has been written. There are many ways to write program from a simple text editor program like notepad++ that has built in features like color

to make it easier to visually organize the program. To full on IDE that has code completion and intellesense that will assist with code completion by recommending what it believes is the code you want to use.
Embedded

After selecting the TMS320F28377S as the microcontroller of choice. The IDE of choice becomes relatively easy to make. Since it is a Texas Instruments (TI) chip there is a special IDE called Code Composer Studio that is used in developing applications to use with TI chips. Code Composer Studio will simplify the process of connecting the microcontroller dev board to the computer considerably. There are special packages and libraries built in to handle communication to the device. Making it much easier to communicate with the device and start writing code to work with the microcontroller. There is also a large set of example projects that can be examined and modified to assist in development [7.4].

Desktop Application: After deciding upon Python as the desktop language of choice there are a few options that could be used as a development environment. After further research there are various tools that can be used for development. There are bare bones text editors that will simply save your code in a text like document like notepad. There are more advanced text editors that have text highlighting and code completion. Some can even execute the code and debug it with installed plugins like Atom, Sublime, VS Code. There are also IDEs that can support multiple languages and with certain plug ins installed make Python development possible. This includes Visual Studio with Python Tools for Visual Studio or Eclipse with PyDev. These full feature IDEs require special experience with the tool to be able to use well. There are also Python specific editors that have full features and can be used to execute and debug the code. This includes PyCharm, Thonny, and Spyder [7.5].

Table 7.1 Comparison of Python Development Environments

IDE	PyCharm	Eclipse w/ PyDev	VS Code	Notepad
Syntax Highlight	Yes	Yes	Yes	No
Code Completion	Yes	Yes	Yes	No
Execute Code	Yes	Yes	No (Yes w/ plugin)	No
Debug Code	Yes	Yes	No (Yes w/ plugin)	No
Save Code	Yes	Yes	Yes	Yes

Because of their lack of features and tooling to assist in development normal text editors will not be considered like notepad. The unfamiliarity with the language makes it necessary to use a full feature IDE to assist with development. Thonny for its beginner friendly objective will help with the skill level of our team with Python but it is lacking in features. And Spyder while being a powerful tool is designed with data science and machine learning in mind and has been built for those applications. Of the development environments examined PyCharm has been chosen as the development environment of choice. It is a full featured development tool that has all the important features like syntax highlighting and code completion. It is also possible to run and debug the code making it easier to write and test the code as it is being written.

7.2 Software Version Control

Version control is an important feature in any project involving many people. The ability to have a saved set of code that can be kept in multiple places avoid any unforeseen circumstances like computer failure. There are many different applications that can be used for version control and they will be discussed below.

Local Version Control: Local version control is the first form of version control. In which the user would make separate folders to hold a different version of the files and keep track of the differences that way. This form of version control was easy to implement but incredibly prone to errors that would cause irreversible

damage. To avoid the errors that responsibility was removed from human users and placed on local databases that had revision control built in to keep track of the stuff they put on the database. This was fine to use with a single user but made it incredibly difficult to work in teams and keep track of changes [7.6].

Centralized Version Control: Centralized version control came after local version control. This version control was created to make it easy to coordinate code changes between teams of developers. In this version control system, there is a central server that houses the main files. These files can be checked out by individuals and modified and then later checked back into the server. This was the standard version control for many years in early development. Some of the popular forms of this type of version control are CVS and SVN. This type of version control has one fatal flaw. If the central server goes down or is broken it makes it impossible for the team to collaborate and if the data is lost the entire project is gone unless proper backups have been implemented. Let's examine a few version control systems that use centralized version control.

Concurrent Versions System (CVS) was the first form of version control. It is an open source software that can be used for version control. A server hosts the files and they can be checked out and later check in the changes they made. It will only allow changes to be checked in if the most recent version of the file is being used. So, the developers must make sure that they have the newest file set before they modify it and check it in. CVS was a great start to version control, but it has been outdated and surpassed by the newer tools that were created after its inception.

Subversion (SVN) is another version control application. It is also an open source software and is the successor to CVS. It operates much in the same way as CVS in that a server will host the files and they can be checked out modified and checked in after the changes have been made. SVN is very popular and widely used. It is even the version control used at Johnathon's current internship with Leidos.

Distributed Version Control: Finally, Distributed Version Control Systems was created to make up for the shortcomings of the version control that came before it. There is still a central server that houses the code. However, the local machine will also house and mirror of the server repository. If the server fails and the content is lost it can easily be restored by any of the other machines that have a mirrored repository. This system is also designed to work well with remote repositories making it easy to work with different groups in different ways easily which was not possible with the older forms of version control. Some of the most popular forms of this version control are Mercurial, Bazaar and Git, these tools will be examined below.

Mercurial is a newer open source version control system. Mercurial was designed to be very fast and easy to use. Making it an ideal candidate for teams that are worried about speed and simplicity. It is usually used for very large-scale projects and has a lot of tooling to assist keep teams on track. There is a web application dashboard to help with controlling the project and very few commands to learn and execute to perform tasks.

Git is another form of version control. It is radically different than the other forms of version control because there is not a central code repository that is housed on a server. In many other forms of version control, the information stored on the server is a file system and the changes that happen to those files over time. In Git it is different because it thinks of the data as a snapshot of a filesystem. If changes are made to the filesystem or its structure it will take a picture of it and use it as a reference to keep track of what the state of the whole file system is. It is also more difficult to use than other forms of version control.

Bazaar is a distributed version control system, which provides a very user-friendly experience. It can be used with a central code base or a distributed code base. Making it a very versatile form of version control. It has a lot of plugins and tools to help make it better. One feature it has that Git and Mercurial do not is bound branches. Bound branches will check and make sure your local copy is the same as the server copy before allowing you to commit and avoid version errors. It also makes the changes on the server before allowing the local commit to succeed, this is another form of error prevention [7.7].

Selection: There are a plethora of version control tools on the market and many of them would work just fine in development of PHATCAT. Since we are a small team and will only have a maximum of four different people contributing to the code. As well as the small scale of the code we will be managing. Make a lot of the tools with all the bells and whistles unnecessary. Keeping local copies of our code would be enough. However, having an online backup of all the files is incredibly useful to prevent unforeseen circumstances. Git has been selected as the preferred method of version control. It allows the team to have a public repository that is on the cloud and can be sent to and received from. This is an ideal solution so that the team does not have to set up a server to house the repository. As well as the familiarity of using Git in other projects, while attending school.

7.3 PHASOR CONSTRUCTION

Preparation of Phasors for Protection Functions: There are several things that must be done to provide a reliable stream of phasors to the protection functions. The first is the calibration of PHATCAT to adjust for its standing error. Ideally, the internal values obtained for voltage and current will be identical to those inputted into PHATCAT. That is:

$$V = V_{in}\,; I = I_{in}$$

Where V and I are the obtained results and V_{in} and I_{in} are the inputs. However, there are several hardware and software steps in-between these two quantities. The final values in the ADC must be properly scaled and calibration should be done to minimize the impact of non-ideal effects and component imperfections.

Current Sense Scaling and Calibration: For the current sense, the current is stepped down by a ratio factor two thousand then turned into a voltage through the use of a sense resistor. This may be inaccurate. The CT has some internal impedance that can be modeled as a series impedance with both a resistive and reactive component. This effectively creates a voltage divider. The sense resistor will have some inaccuracy, which will make the real R_{sense} different from the selected. The protection diodes have some nonzero leakage current, which robs current from the sense resistor. We assume nonideal capacitance to play a small role because our frequency spectrum of interest is so low (325 Hz max). These two nonidealities allow for the input voltage into the ADC to be approximately expressed as:

$$V_{ADC} = \frac{R_{sense}}{R_{sense} + Z_{CT}}\left(\frac{I_{in}}{CTR} - I_{Diode}\right)R_{sense}$$

Where R_{sense} is the sense resistor value, Z_{CT} is the CT and current limiting resistor impedance, I_{Diode} is the leakage current into the diodes, and CTR is the CT turns ratio. This is approximate, of course, as the diode current leaves after passing through the CT impedance. In reality, these effects are more also intercoupled as well as voltage and temperature dependent. But a detailed model is not necessary, the calibration will be done experimentally. The goal here is to show, generally, how the nonidealities effect performance of the linear analog measurement. V_{ADC} should be measured for a wide range of input currents and a calibration function developed. If a single coefficient, A_{cal}, can be used to bring the whole input range within spec, it will be used. Otherwise, a more complicated expression will have to be developed. The most important factor for making this approximation good is keeping the diode leakage current low. This coefficient allows us to reobtain I_{in} as follows:

$$I_{in} = CTR * A_{cal}\frac{V_{ADC}}{R_{sense}}$$

The ADC is expected to introduce little error. The internal Butterworth filter and oversampling modes will reduce high frequency noise but are chosen to have a unity gain for frequencies of interest. Common-mode noise will be canceled using differential inputs. True simultaneous sampling for all channels and a parallel-interface means that the skew between channels will be small. Still, the 2's compliment value it produces

will have to be scaled. When operated in the ±10V range, an output of 2^{15}-1 corresponds to +10 and an output of -2^{15} corresponds to -10V. Since 2^{15}-1 ≈ 2^{15} we can use this with the above equation to determine the input current from the 2's compliment value received from the ADC:

$$I_{in} = CTR * A_{cal} \frac{1}{R_{sense}} \frac{10}{2^{15}} O_{ADC}$$

Where O_{ADC} is the 16-bit 2's compliment value stored in the microcontroller's memory from the ADC. This value can be multiplied by the user-set CT ratio (for primary equipment CTs, not those within PHATCAT) to present metered data. However, it will be convenient to leave it in this form for many protection functions.

Voltage Sense Scaling and Calibration: A very similar process is used to yield the following expression, which relates the input voltage to the 2's compliment number output by the ADC.

$$V_{in} = PTR * A_{cal} \frac{1}{R_{sense}} \frac{10}{2^{15}} O_{ADC}$$

Sample Set: One of PHATCAT's principle limiting factors when it comes to speed is the low frequency of power systems. It does not use any form of fractional cycle estimation, so at least one power system cycle's worth of data must be read in order to obtain accurate FFT results. Since the frequency is not known until the ZCD algorithm runs, the window must be wide enough to ensure enough samples are acquired to track the lowest frequency PHATCAT is designed for – 45Hz. So, upon startup, PHATCAT begins by maintaining a 22.2ms sample set (139 samples @ 6250 Hz). However, once a frequency is acquired, a sample set of `ceiling(1.1*f)` is used for the next window. This reduces the required waiting time and allows for some margin in case the system frequency declines within the current window and the next. Furthermore, the sample set is maintained on a sliding basis – not a sequential one. PHATCAT generates an interrupt to build its phasors and evaluate protective functions every 16th of a power system cycle. This means that, once the relay has run for several cycles, protective elements will begin to see the disturbance within 1/16th of a cycle.

Frequency Tracking: PHATCAT uses a software-implemented ZCD algorithm with hysteresis and 5-cycle averaging to determine the system frequency. PHATCAT supports the selection of either the W or X winding as the source-side winding. The A-phase voltage of this winding is used as the primary source for the frequency tracking and zero reference phase angle. The selected side should be that which is typically energized before load is connected. For instance, for a generator step-up transformer, the low voltage side would be the source side. For a distribution transformer, the high voltage side would be selected.

During a close-in fault involving A-phase, the local voltage may become very depressed. A voltage near zero may be a poor reference for frequency and phase. If the voltage is less than 10% of the transformer's nominal voltage, the A-phase current of the source side is then selected as the frequency tracking and phase angle source. If PHATCAT is protecting a transformer in a radial network, it may see little fault current on the non-source side of the transformer. This should not be selected as the primary source side in PHATCAT's settings. Nevertheless, PHATCAT will try to use the A-phase current on the other (set non-source) winding of the transformer in the event that the other two sources are of insufficient magnitude. Fig. 7.1 illustrates this control logic implemented in Simulink.

Fast-Fourier Transform: In order to achieve an accurate FFT for one cycle of data, it is very important that the passed sample set consists of one cycle exactly. The sample set program ensures that there are always a sufficient number of samples in the array of read values. The frequency tracking allows for the number of samples to be processed, `floor(1/f)`, to be determined. The array to be processed is copied elsewhere so it is not modified by the sampling processes and trimmed to fit this length. The FFT functionality provided in TI's Control Suite is applied.

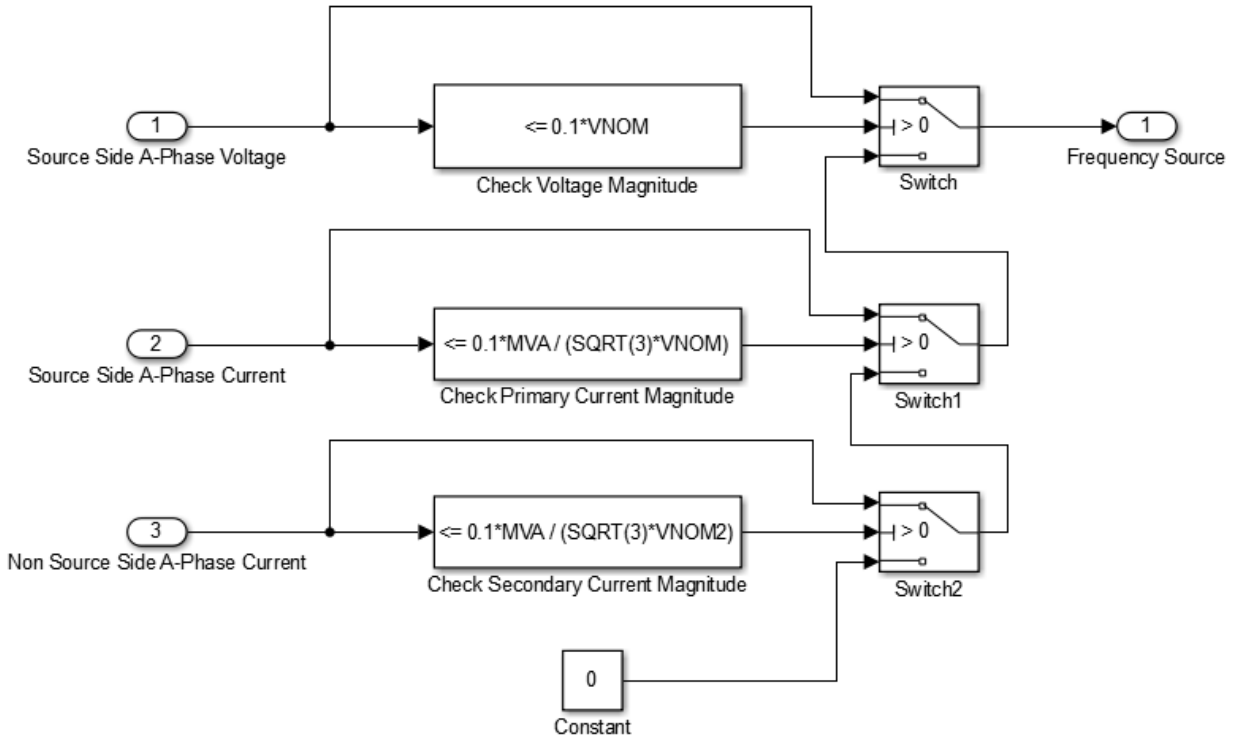


Fig. 7.1. Frequency Source Selection. Produced with Simulink by B. Ross

Connection Compensation: Due to the phase shift introduced by the mixing of delta and wye connected windings, the current and voltage phase angles must be modified. PHATCAT will support Y-Y, DAB-Y, DAC-Y, Y-DAC, and Y-DAB connections. A 30 degrees phase shift is added to the various phasors as appropriate based on the connection selected by the user.

PHATCAT assumes that its current and voltage inputs come from wye-connected instrument transformers. The CT and PT circuits should be grounded in one place and as close to PHATCAT as possible. Instrument transformer cables that pass through extra-high voltage yards on their way to the control house should be shielded. These practices prevent ground loops and minimize noise.

Sequence Component Extraction: Both positive-sequence and zero-sequence currents should be calculated for use in protection subroutines. They are obtained using:

$$I_1 = \frac{1}{3}(I_a + I_b\angle 120° + I_c\angle 240°) \qquad 3I_0 = (I_a + I_b + I_c)$$

Note that the zero-sequence is not divided by 3 so as to leave it in a form convenient for use in residual overcurrents.

7.4 Protection Algorithm Design

In this section, the designed behavior of PHATCAT's protective algorithms is discussed.

Overcurrent Algorithms: PHATCAT provides phase, neutral, and residual overcurrent elements for both the W and X winding with both instantaneous and time-inverse functionality. Each instantaneous element has a configurable pickup with definite time setting. Each time-inverse element has a configurable pickup, time dial, and curve setting. The phase overcurrent operates based on the currents measured on the phase (ABC) current inputs, the neutral overcurrent operates based on the currents measured on the neutral (N)

current inputs, and the residual overcurrent operates based on the vector sum of the phase currents. PHATCAT allows the user to select from the standard U.S. relay curves, which utilize a characteristic governed by two general equations:

$$t_{trip} = TD * \left(\frac{A}{M^D - 1} + B\right) \quad ; \quad t_{reset} = TD * \left(\frac{C}{1 - M^2}\right)$$

't_{trip}' is the time to trip for a given fault current. *M* is the fault current, expressed as a multiple of the user-defined pickup current. *TD* is the user-defined time dial setting. The coefficients *A, B, C,* and *D* are defined by the user-selected curve. They are given in table 7.2. The meaning of 't_{reset}' requires a more detailed explanation, which is given in the discussion below.

Table 7.2 Coefficients of U.S. Relay Curves

Curve Name	Curve Code	A	B	C	D
Moderately Inverse	U1	0.0104	0.2256	1.08	0.02
Inverse	U2	5.95	0.180	5.95	2.00
Very Inverse	U3	3.88	0.0963	3.88	2.00
Extremely Inverse	U4	5.67	0.352	5.67	2.00
Short-time Inverse	U5	0.00342	0.00262	0.323	0.02

These curves are applied with some caveats. The operating time curve is only used when *M* is greater than 1. If *M* is greater than 30, an *M* of 30 is used. Notice that these curves provide an 'electromechanical reset' option that simulates the dynamics of a traditional electromechanical device. This curve is used when $M < 1$, after the relay has begun to time ($M > 1$ for some time period previously). In the event that the current briefly drops below the pickup value (e.g. due to a conductor making poor and intermittent contact with the ground), the element does not reset its timing. Rather, it begins to re-accrue time delay by slowly 'traveling' back towards its reset position. The t_{reset} value given above is the time it would take for the relay to fully reset its timing if it has fully traveled to the point of tripping. The behavior of this function will be clearer with a brief description of the overcurrent algorithm's real-time behavior.

The timed elements in PHATCAT operate based on the analog of a physical induction disk traveling towards the closure of a contact. Rather than calculating a certain operating time and waiting, the virtual position of the disk is tracked. For while time-inverse curves provide an operation time for a given fault current, real-world fault currents are time-varying. A 10kA fault current may have an operating time of 1.0 seconds, but what is the operating time for a fault current that is 10kA for 0.3 seconds then increases to 12kA?

For each overcurrent element, there is a travel distance to operate, *x*, which varies from 0 to 1.0. Every time PHATCAT evaluates the measured currents (every ~1 ms) and checks its protection logic, it does not simply compute an operating time (t_{op}). Instead, it computes a velocity, *v*, of travel towards operation. This obtained by taking the reciprocal of the instantaneous operating time (computed using the equations above). The known time-step between calculations, t_{step}, is then multiplied by this reciprocal to compute a change in travel distance. In other words, $\Delta x = \frac{t_{step}}{t_{op}}$. Once *x* is greater than or equal to one, we have traveled to the point of operation. If *x* is not zero and $M < 1$, then a negative travel distance is calculated, based on the given electromechanical reset curves.

Current Differential Algorithms: The current differential algorithm starts by normalizing the currents on the high side and low side of the transformer. Two normalizing factors, historically referred to as 'TAPS' due to their originally being physically set transformer taps in electromechanical devices, are used to normalize the currents on each winding so as to make them comparable. Based on the equation for three-phase power, the scaling factors are designed to both normalize the measured currents and ensure reasonable magnitudes for comparison (i.e. not too large or small to exacerbate the impact of inaccuracies). For both sides of the transformer, the TAPS values are calculated according to the following formula:

$$TAP_n = \frac{MVA * 1000}{\sqrt{3} * KV_n * CTR_n}$$

Where TAP_n is the TAP value for winding *n*, MVA is the highest nameplate rating of the transformer, KV_n is the line-to-line voltage of the *n* winding, and CTR is the CT ratio of the (wye-connected) CTs for winding *n*. Notice that this is actually the equation for the secondary side relay current at the transformer's rated load. The measured currents are divided by their associated TAPS before further use. At rated load, then, the measured currents will be normalize to a value of 1. The remaining differential settings are then cast in terms of multiples of their TAPS value. For example, an unrestrained pickup value of 10 would mean that the current differential has to be ten times the transformer's rated load to operate the unrestrained differential.

With the currents normalized, I_R is calculated by taking the greater of the two means of the three phase current magnitudes. For example, if the normalized current magnitudes are 1.2A, 1.1A, and 1.25A for the high side of the transformer and 0.3A, 0.2A, and 0.2A on the low side, I_R would be 1.18A. This provides a relatively stable indicator of the transformer's current loading condition. It also prevents the restraint from being reduced to a low-side CT saturation event, in which case a properly set restraint would be essential. Before I_{op} can be determined, connection compensation and zero-sequence remove must occur. If the user has selected a delta-wye transformer, 30 degrees is either added or subtracted to the phase angles to compensate. To prevent unintentional operation for external ground faults on a delta-wye, the zero-sequence component is calculated and subtracted from the currents. I_{op} is then determined by taking the vectorial sum of the normalized currents for each phase.

With the currents obtained, I_{op} is then compared to the unrestrained pickup value, it being the most extreme case. I_R is then analyzed to determine if I_{op} is in the minimum pickup region, the slope 1 region, or slope 2 region. The user-defined curve parameters are used to obtain the corresponding tripping threshold for the relevant region and a tripping decision is made by comparing I_{op} to this threshold.

Harmonic Blocking Algorithms: With the results of the FFT available, the implementation of harmonic blocking is fairly straightforward. The amplitudes of the second, fourth, and fifth harmonics from the FFT of the phase currents are divided by the amplitude of the fundamental frequency. These ratios are compared to the user-defined percentage values. If any of the thresholds are exceeded for any phase, then the differential element is blocked for all phases for one power system cycle. The second and fourth harmonic elements are intended for detecting inrush current events and the fifth harmonic element is intended for detecting saturation. A value of 15% is considered a reliable setpoint for reliable detection.

Overexcitation Algorithms: The overexcitation algorithm operates based on a normalized Volts/Hz quantity. The voltage is normalized based on the user-defined winding voltage and the frequency is normalized based on the user-defined system nominal frequency. The normalized quantities are divided (voltage over frequency) to provide a measure of the transformer's excitation level that can be express as a percentage. At 1 p.u. voltage and 1 p.u. frequency, the excitation level is 100%. PHATCAT will calculate based on the source-side winding. The time delay is based on an increment, which counts every period that the percentage threshold is exceeded until the set time has elapsed.

7.5 LCD DISPLAY DESIGN

The LCD is a critical part of the PHATCAT device because it will be relaying a lot of the information about what is happening with the device to the user (fig. 7.2). The display is a forty-by-four character display so, it can show forty different characters on four different rows. Meaning that there is only so many things that can be displayed on the screen at a time. This will make it so that there will have to be three separate screen layouts to display all the relevant information to the user.

The first screen will display the three phase current phasors as for each winding well as the neutral current. The left side will be the W-winding and the right side will be the X-winding for each of the rows. It will be able to display the readings in amps or kiloamps depending on the magnitude of the reading. The first part of the number is the magnitude the @ will symbolize the phase of the current which will be found after that. There will be an ASCII art transformer (-><-) between both windings.

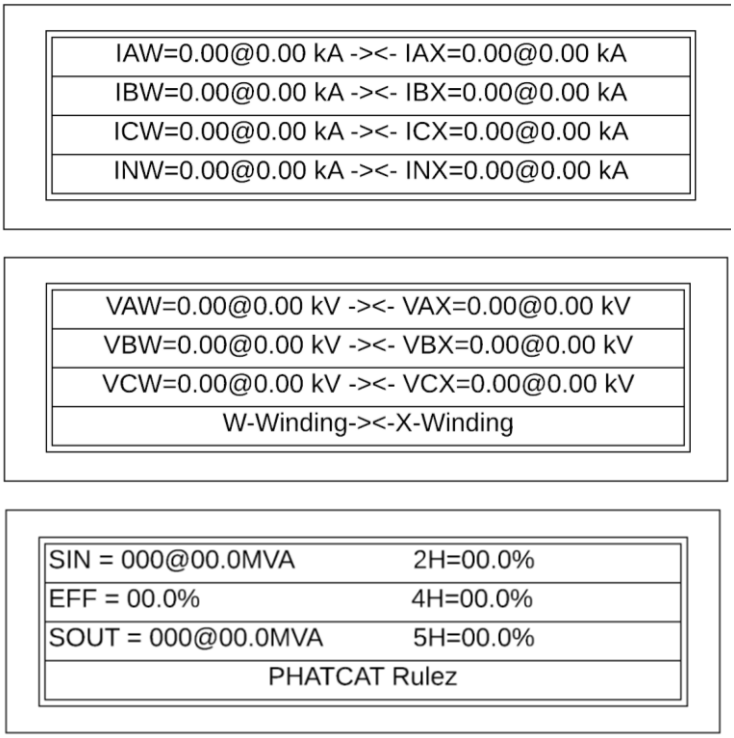


Fig 7.2 Information shown on PHATCAT's display. By John DeFour.

The next screen will be the voltages screen. It will be very similar to the current screen except it will only have three rows because there will be no neutral voltage to display. In the voltage screen, it will display the numbers in volts and kilovolts.

The third and final screen will have several derived quantities that may be of use. The first is the input apparent power magnitude and power factor (SIN). The output apparent power and power factor (SOUT) as well as the transformer efficiency of the device will be displayed as a percent (EFF). It will also display the percentage content of the different harmonics use in the blocking logic (2H, 4H, 5H). There will also be an added phrase for much-needed humor and flair to the project.

7.6 Desktop Application Design

The desktop application must be easy to work with and intuitive to use. For these reasons it will be modeled after the very popular AcSELerator Quickset software that Schweitzer Engineering Laboratories uses with their relays. There will be multiple settings that have to be set on the PHATCAT device and can be configured the way the user wants. There will be main groups of settings that can be opened to configure the settings found within. There will be borders around the settings that are grouped together and they will have a label to describe their use and what can be entered in them. There will also be a tooltip that appears when the user hovers over a setting to describe it too. An example of a settings screen can be found in fig. 7.3 application prototype. A full list of settings can be found documented in the software.

Logic Expressions: There are also special characters that will be recognized when writing logic expressions in the portions of the settings that can be altered by the user. These characters must be parsed by the desktop application and used to configure the settings on the device. An example of a user defined logic expression

can be found in figure 7.3. A complete list of user defined logic expressions can be found documented in the software.

Desktop Prototype: Now that the different components of the desktop application are completed a prototype has been created to represent what the desktop application will look like to the end user. This prototype can be found in fig. 7.4. The white text boxes will be the areas that can be modified by the user and will recognize the logic expressions entered by the user. The grayed out drop-down boxes will have a list of settings that can be selected by the user. Each group of settings will populate a page of settings that can be modified and stored in the desktop application. These settings can also be sent to the PHATCAT device through USB mini connection.

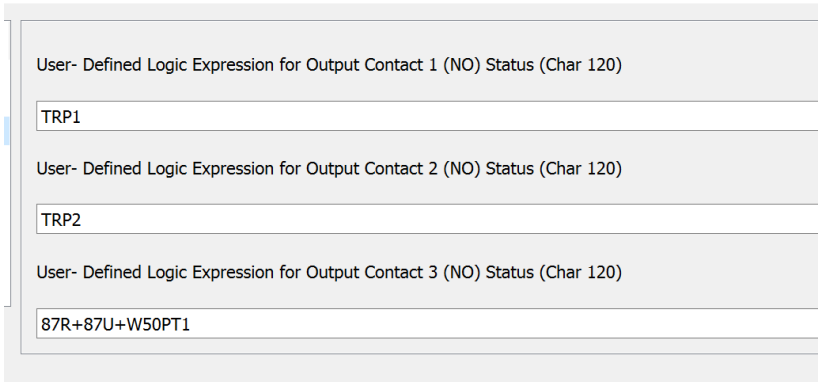


Fig. 7.3 User Entered Logic Expression Example by John DeFour

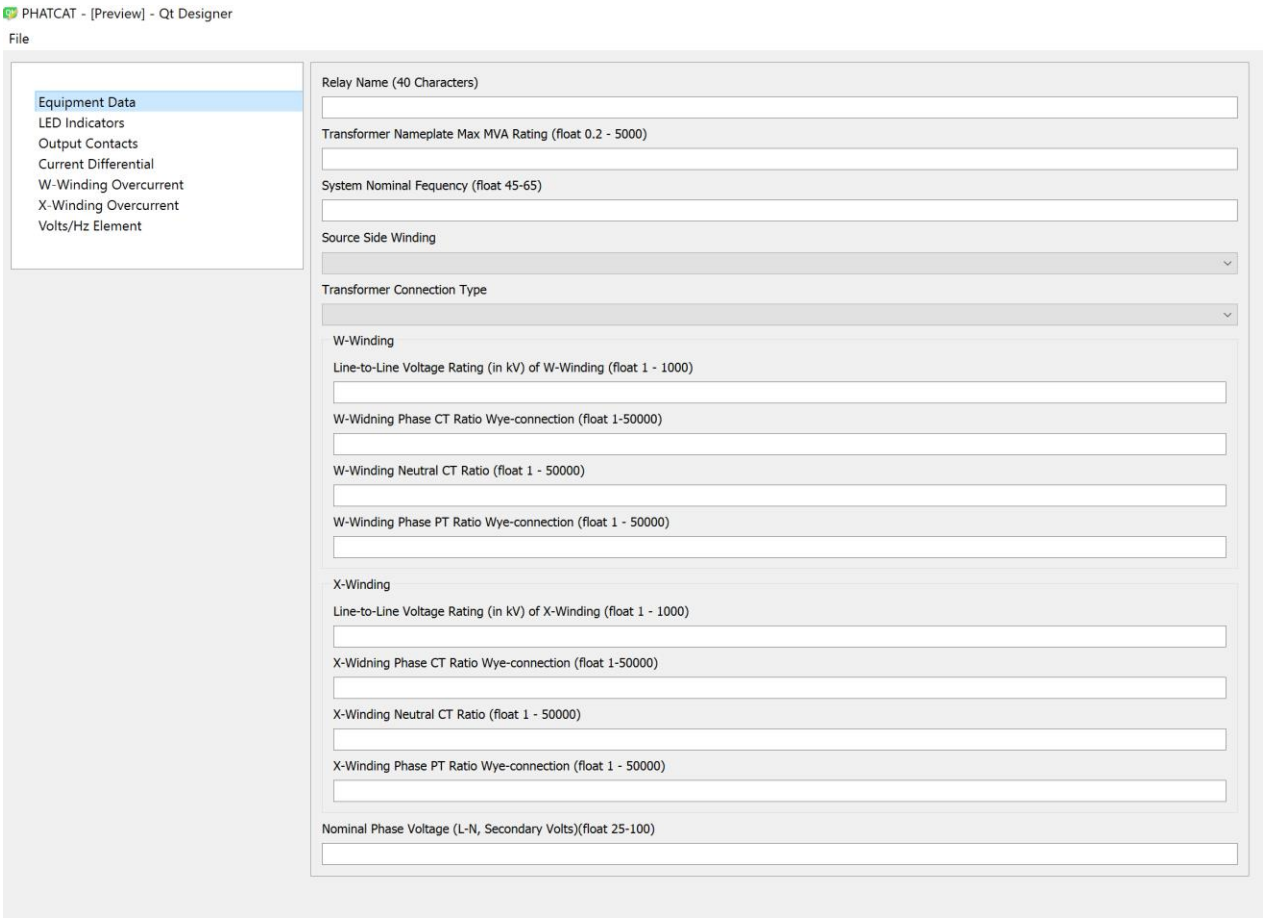


Fig. 7.4 Desktop Application Settings Prototype by John DeFour

8. SYSTEM FABRICATION

With all of PHATCAT's hardware and software functionality realized, a fabrication plan for the device is put forth including both PCB and the device enclosure.

8.1 PCB DESIGN SOFTWARE

Printed Circuit Boards (PCB) were invented in order to minimize the complexity and size of an electric circuit. Designing a circuit on a PCB allows all components to be connected electrically by copper traces on a common board. In order to design a PCB, there are many different types of PCB design software that are considered. The software used to design a PCB is sophisticated and has many different features from the others. The three different types of PCB Design Software that are considered for PHATCAT PCB Boards are EasyEDA, Altium and Eagle.

EasyEDA: EasyEDA is a web-based Electronic Design Automation (EDA) tool. There are many advantages to the web-based tool. The most important feature that EasyEDA has to offer is that it does not need to be downloaded and therefore can be accessed from any computer. The tool is capable of operating using any type of operating system such as MAC, Windows or Linux as long as there is a capable web browser. In order to experience the best performance possible with the web-based tool, it is recommended to use Google Chrome or Firefox web browsers. EasyEDA is well known for the simplicity and the user-friendly features which make it an attractive choice to inexperienced PCB designers. There are over half a million libraries to choose from for schematic symbols and board layout footprints. If the component is not available in one of the available libraries, there is a feature where you can create your own component. The EDA tool is also capable of supporting the component libraries from Eagle and Altium.

Altium: Altium is the more expensive PCB Design Software, however does offer a free trial. The licensed version of the software would cost a company about $7,245.00 dollars. The software is ideal for a corporation with a larger budget and corporate engineers. Altium has a good component management system, where BOMs can incorporate hardware changes with a few clicks instead of having to regenerate all of the information again. The schematic browser is user friendly and has an easy to use feature that allows every pin in the schematic to be easily checked. Altium is very capable of designing very difficult and complex circuits that generate fast and realistic results. The circuit design can be viewed in a 3D Model to help with further understanding and visualizing a specific board design. Due to Senior Design Cost constraints, Altium will not be considered for our PCB Design Software.

EAGLE: Easily Applicable Graphical Layout Editor (Eagle) is widely used and is highly recommended by students and professors at the University of Central Florida. Eagle offers a free student download version of up to 16 layers and up to a size of $4m^2$. The most important feature that Eagle has to offer is the large component library system for component selection. If a component is not available in the one of the libraries, you can design the symbol and footprint yourself or get a site like 'Digikey' or 'Mouser' to do it for you. The libraries of the components can then be imported into Eagle using a Library Uploader or Ultra Librarian. The Schematic and Board Layout Editors are user friendly and very easy to use. Due to Eagle's large library system, user base, the free downloadable version and Senior Design Class Tutorial, the decision was made to use Eagle for our PCB Design Boards.

8.2 PCB DESIGN PHILOSOPHY

The Printed Circuit Board (PCB) is the most popular method for incorporating electronic circuits and components into a design. The electronic components and devices of a circuit are connected together using sheets of copper as traces and pads. The PCB is popular due to its compact and rigid form of routing power and signals to different electronic devices that make up a specific circuit. A typical PCB is made up of multiple layers, the number of layers on a PCB is measured by the number of sheets of copper within the board. The thin copper sheets are laid on top of an insulating material called a substrate (FR4). The Solder

is the metal that connects all of the electronic component and devices to the board, which serves as a strong mechanical adhesive [8.1]. The layers are then laminated together to form one object.

PCB Layers: The PCB is made up of multiple layers where the thin layers of copper are separated by a substrate and these layers continue to make up a multi-layer board that consist up to as much as sixteen layers kind of like a cake with layers of frosting. The composition of the PCB is shown in fig. 8.1.

Substrate (FR4): The most popular major material that a typical PCB consists of is a type of fiberglass called 'FR4'. FR4 is a NEMA grade designation for glass-reinforced epoxy laminate material. FR4 is a composite material composed of woven fiberglass cloth with an epoxy resin binder that is flame resistant. The FR4 is popular due to its electrical and mechanical qualities that remain constant in both dry and humid conditions. The substrate material is what gives the PCB a certain thickness and durability. However, there are some PCBs built on a type of heat resistant plastic that presents a little more flexibility. A lot of the Arduino and Raspberry Pie boards use a thickness of 0.8mm.

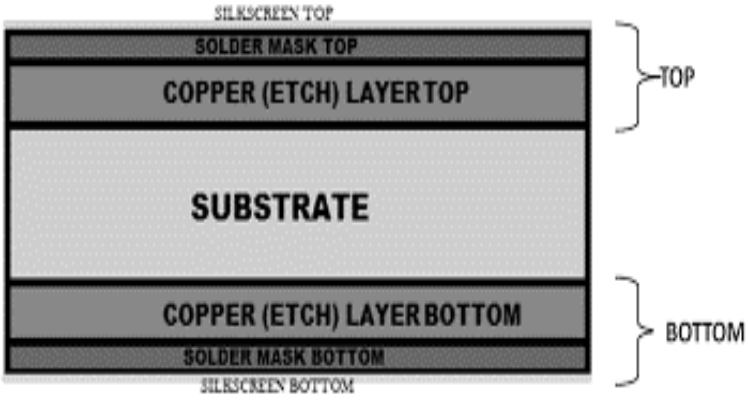


Fig. 8.1. Composition of a PCB. Reproduction permission requested from Technology Uncorked.

Copper: The thin copper layer is applied to the substrate material. For a multiple layer board, the copper layer is applied to both sides and sandwiched together. The typical weight of the copper layer of a PCB is 1 ounce of copper per square foot which is about 1.4 thousandths of an inch in thickness of copper. This measurement of thickness translated to meters would be about 35 micrometers resulting in an extremely thin layer when compared to the substrate insulating material layer. Some PCBs are designed to handle more power and therefore incorporate more sheets of copper per micrometer to account for the increase in voltage and current.

Soldermask: The solder mask is the layer that is applied to the copper layer which gives the PCB a typical green tint, but the solder mask can come in a variety of colors. The following layer provides a type of insulation to all copper traces and connections to prevent the accidental contact that may occur between solder and other metals. The silver rings and surface mounted pads are left uncovered by the solder mask for soldering purposes.

Silkscreen: The silkscreen layer is typically applied to the top or bottom layer of the board. The silkscreen is an important part of the design for identifying the connections, electrical components and specific values pertaining to different sources and elements. Since the top or bottom layer is all that is seen and is the only place to mount through hole or surface mount components, the silkscreen is a good way of identifying these components and certain characteristics about them. Identifying and incorporating as much information as possible into the design is a great way to help a user understand the board and better identify the different functions of the pins. The silkscreen is often used by manufacturing companies to put their company seal on their products. A particular standard has not been developed in regard to placing a company logo on a PCB, but they will generally place them in a location that is not critical. The typical application of a silkscreen is applied using a white color, but other colors can be used, however it would be unusual to see more than one color on any given PCB.

PCB Production Terms [8.2]

- Annular Ring: Conductive material surrounding a hole which creates a pad.

- Breakdown Voltage: The voltage at which an insulator or dielectric ruptures, or at which ionization and conduction take place in a gas or vapor.
- Bridging, Electrical: The formation of a conductive path between two insulated conductors such as adjacent traces on a circuit board.
- Component Hole: A through hole used for the attachment and electrical connection of component terminations, including pins and wires to the printed circuit board.
- Current Carrying Capacity: The maximum current which can be carried continuously, under specified conditions, by a conductor without causing degradation of electrical or mechanical properties of the printed circuit board.
- Design Rule Check: The use of a computer program to perform continuity verification of all conductor routing in accordance with appropriate design rules.
- Ground Plane: A conductor layer, or portion of a conductor layer, used as a common reference point for circuit returns, shielding or heat sinking.
- Hole Density: The quantity of holes in a printed circuit board per unit area.
- Pad: The potion of the conductive pattern on printed circuits designation for the mounting or attachment of components. Also called Land.
- Plated-Through Hole: A hole in a circuit board that has been plated with metal (usually copper) on its sides to provide electrical connections between conductive patterns layers of a printed circuit board.
- Surface Mount Technology: SMT defines the entire body of the process and components that create printed circuit board assembly with leadless components.
- Trace: A common term for the conductors.
- Via: A plated thru-hole is used as an inner-layer connection but doesn't have component lead or other reinforcing material in it. Vias can make an electrical connection between layers on a PCB.

8.2.1 RELIABLE PCB DESIGN PRACTICES

The PCB has proven to be the most modern way of translating electric circuits and utilizing them for a variety of different applications. Since the PCB has come to play such a crucial role in the development of electronics, there is a need for reliable, long lasting designs. Getting started with a new PCB design, it is possible to neglect certain PCB design principles and focus more on developing the circuits and key components for the design. While, developing circuits and choosing key components is important, rendering to certain general rules for PCB design can prove to be very important. If the necessary time is not taken to consider the PCB design, this could translate poorly from the digital domain to physical reality [8.3]. A poorly translated design could mean trouble when it comes to the manufacturing of the PCB. There are five general rules for PCB design that need to be known in order to produce a product PCB that is functional, manufacturable and reliable.

General Rule #1: Strategically Place Components. Strategically laying out the components on the PCB is an important part in the design process. A part that can prove to be quite challenging. One must consider the available space and determine if a multilayer board is needed or if the components and traces can all fit on a one-sided or double-sided board. There are recommendations to mount components in a basic order of types of circuits, such as power circuits or critical circuits, but here are a few guidelines to keep in mind for component placement:

- Orientation: The orientation of like components should be the same in order to help reduce the length of trace lines and make the soldering process more efficient with less errors.
- Placement: When considering where to place the components on the board, avoid areas on the board where the solder side of the plated through-hole components are located.

- Organization: The through-hole components should all be mounted to the top side of the board and the surface mount technology components should all be placed together on the same side of the board. This is done to minimize the number of assembly steps.

One last thing to keep in mind while designing your PCB, the utilization of different component technology may require the manufacturer to have to go through a lengthier process and thus drive up the overall manufacturing cost of the PCB.

General Rule #2: Strategically Map Your Power, Ground and Signal Traces. After all your components are laid out on the board and oriented properly, the next step is to plan how to route the power, ground and signal traces. Strategically mapping out your trace paths is important to be sure that all pathways are free from obstacles. In order to accomplish this task, here are some important things to keep in mind:

- Positioning the power and ground planes: In order to prevent signal noise and ensure the proper positioning of the components by preventing the PCB board from bending, it is recommended to have them internal to the board while maintaining both symmetry and a center position. When distributing power to the ICs, the recommendation is to use common rails for each supply in order to avoid daisy-chaining the power lines and be sure to design your power trace lines to be solid, wide traces.
- Connecting Signal Traces: To connect the signal traces in reference to the schematic, the recommendation is to keep all traces as short and as direct as possible (fig 8.2, 8.3). If the trace lines are routed in such a way that there is a vertical tracing route on one side of the board, then the tracing route should be horizontal on the other side to prevent component rotation and maintain proper positioning.

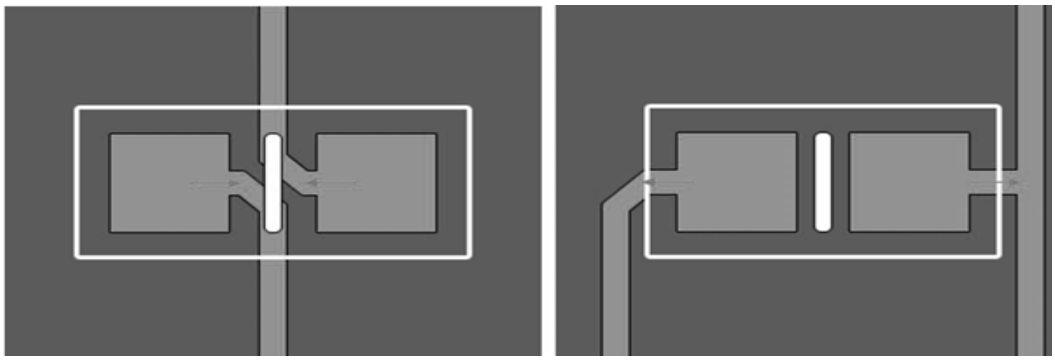


Fig. 8.2. Preferred Routing Trace Lines. Reproduction permission requested from Altium.

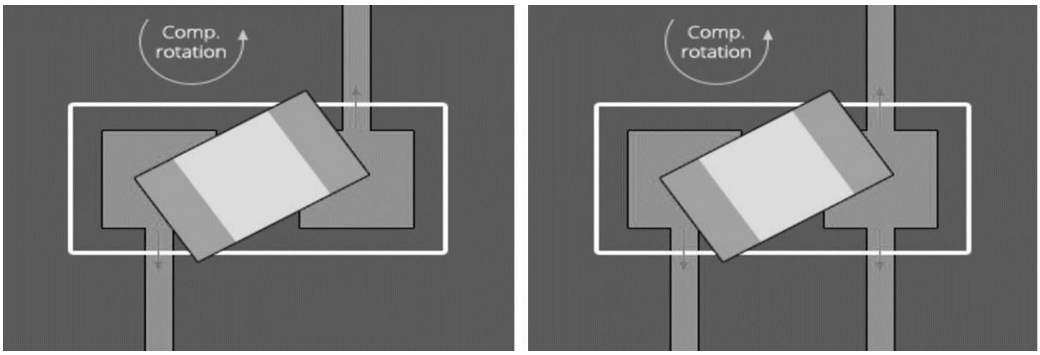


Fig. 8.3. Non-Preferred Routing Trace Lines. Reproduction permission requested from Altium

- Trace Widths: The design will require a variety of different levels of currents which dictates the net width of a trace. For low analog and digital current signals, the recommendation is to use a net width of 0.010". If the signal carries more current than 0.3 Amps, the width of the trace should be wider. To simplify calculating the net width of a trace, use an online trace width calculator.

General Rule #3: Analog and Digital Component Separation. The analog and digital components must be separated in order to minimize noise and the interference of signals (fig 8.4). The higher voltages and currents in power circuits tend to interfere with the lower voltages and currents of the control circuits. There are a few things that can be done to minimize these effects:

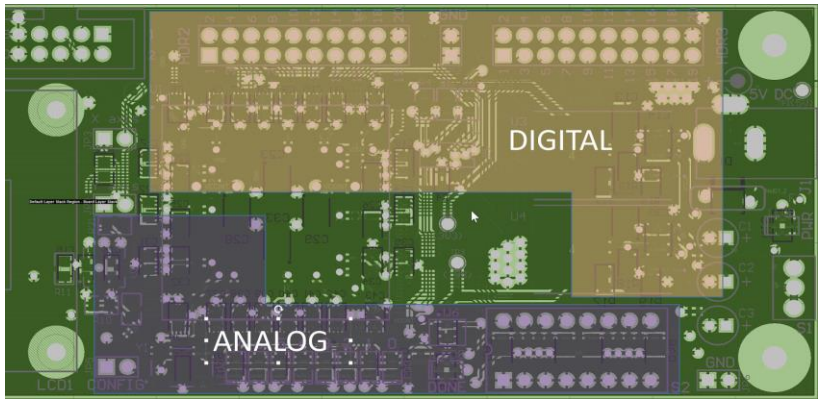


Fig. 8.4 PCB Displaying Separation of Analog and Digital Components. Reproduction permission requested from Altium.

- Separate Planes: The common reference plane for the analog signals and the digital signals must be separated. The power plane, ground plane and traces for the digital signals cannot overlap the analog signals. However, the two must be tied together at the AC to DC converter. The best place to try and bring the two signals together is at the end of the supply path.
- Layer Placement of Planes: Implementing solid power and ground planes into the PCB design will help reduce the amount of EMI emissions, which in turn will improve the quality of the signal present on the copper traces. Considering a two-layer board, then the ground layer should be the bottom layer of the board, where the top layer would be used for component placement and power traces. Considering a four-layer board, then the ground and power planes should be located on the interior layers. The power and ground plane can be accessed through vias connections from the outer layers while keeping the planes and connections symmetrical.
- Capacitive Coupling: The capacitive coupling which can be a product with the placement of a large ground plane can be reduced by routing the analog traces and only allowing such traces to pass over the analog ground plane.

General Rule #4: Keep PCB Temperature in Mind. Temperature can have an effect and play a big role in how a PCB performs. A PCB designer should always have temperature in mind to avoid possible future issues with the design. If the PCB does happen to run into some heating issues that is affecting the boards overall performance, here are some recommendations as to how to deal with the temperature issues with the board:

- Identify Major Heating Components*:* To minimize or prevent any type of heating problems on the PCB that could affect the performance, the major heating components within the PCB design should be first identified. The following components can be identified by referring to their datasheets and locating the thermal resistance rating. Follow the recommendations on the datasheet for keeping components at a decent temperature. All critical circuit components should be placed away from any component giving off a large amount of heat.

- Implementing Temperature Relief Strategies: In order to produce a board that is manufacturable, adding to the board to provide relief due to high temperatures is necessary and needed for multilayer boards with a lot of copper when applying the wave soldering application. The recommendation is to always use a thermal relief pattern for any via or hole that is connected to a ground or power plane (fig. 8.5). Also, adding teardrops where traces connect to pads can help with the mechanical and thermal stresses with the additional copper needed at those points.

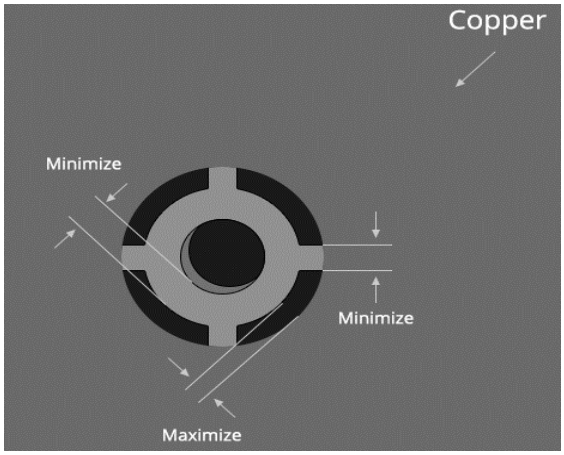


Fig. 8.5. Via Thermal Relief Pattern. Reproduction Permission Requested from Altium

General Rule #5: Reviewing Your Design. The last step in the design process is to review your design thoroughly! Double checking your design at this point is extremely important and could be the difference between manufacturing success or manufacturing failure. There are a series of checks to complete, but it is recommended to start with the Electrical Rules Check (ERC) and the Design Rules Check (DRC).

- *Electrical Rules Check (ERC):* The Electrical Rules check to be sure that proper connections are made to power and ground planes, signal transition times, capacitive loads and fanouts have the appropriate bounds. The ERC determines if there are any unconnected inputs or shorted outputs. Also, checks to make sure that gates are not directly connected to supplies. The Electrical Rule Checks are based upon the normal operating conditions of the application specific integrated circuit.
- *Design Rules Check (DRC)*: The Design Rules Check is a program that automatically checks to determine if a particular design corresponds and is in accordance with a set of predefined technology rules that have been given by the foundry in order to show that a design can be manufactured successfully.
- *Layout Versus Schematic (LVS):* The LVS rule check is a particular method that is used to determine if the functionality of the layout is equivalent to the functionality of the schematic. The schematic is compiled and the Graphical Database System (GDS) devices are recognized along with the specific connectivity which are both extracted to a source netlist and a layout netlist. These netlists are both compared to one another and the results are displayed from the LVS Result Database.
- *XOR Check:* The following check is usually performed after a metal spin, comparing the modified database with the original to verify that the modifications were accurate. The XOR operation is used to compare the layout geometries of both databases. The output is a database of all layout geometries that did not match from both layouts.
- *Antenna Check:* The Antenna is defined as a metal interconnect that is not connected to silicon or grounded. Charges build up on the interconnect during certain fabrication steps at which point there is a rapid discharge that causes permanent damage to the thin transistor gate oxide. The rapid discharge is called the Antenna Effect. The errors that come from antennas can be solved by installing an antenna diode to safely discharge the node.

8.3 PCB SCHEMATICS

There are three separate PCBs designed for PHATCAT. The front panel board holds the LED controller and LEDs. An ADC breakout board is fabricated to allow for standalone software development prior to completion of the main board, it is a development tool not included in the final product. Lastly, there is the main board, which houses most of the remaining components. The current and voltage transformers, due to their bulk, they are housed off board and connected with jumpers. The pushbuttons and LCD are not PCB mount devices, and are mounted on the front panel and connected similarly.

LED Indicator Board: The LED Indicator board mounts to the front panel of the relay (fig 8.6). The board has a 10-Pin Dual Header that will bring power, ground, plus serial communication from the main board's microcontroller to the LED Driver Chip MAX6979AUG. The 16 LED Chips were laid out a half inch apart in two rows. The 1206 packages are used, which are larger than a typical components package in order to simplify soldering the components on the board. A power plane of 5V is generated on the top layer, while a ground plane is generated on the bottom layer. The auto-tracer is a nice feature in Eagle, however, this feature was not used and all traces were individually routed. In order to bypass certain traces a via is used to run the trace on the bottom layer in order to create the shortest path possible to the destination. Another via is used to bring it back up to the top layer after the trace or traces are bypassed. The trace width of 0.12 mils is used since the current seen for the LED circuits will be around only 20mA. The components of the board are labeled using the Silkscreen layer.

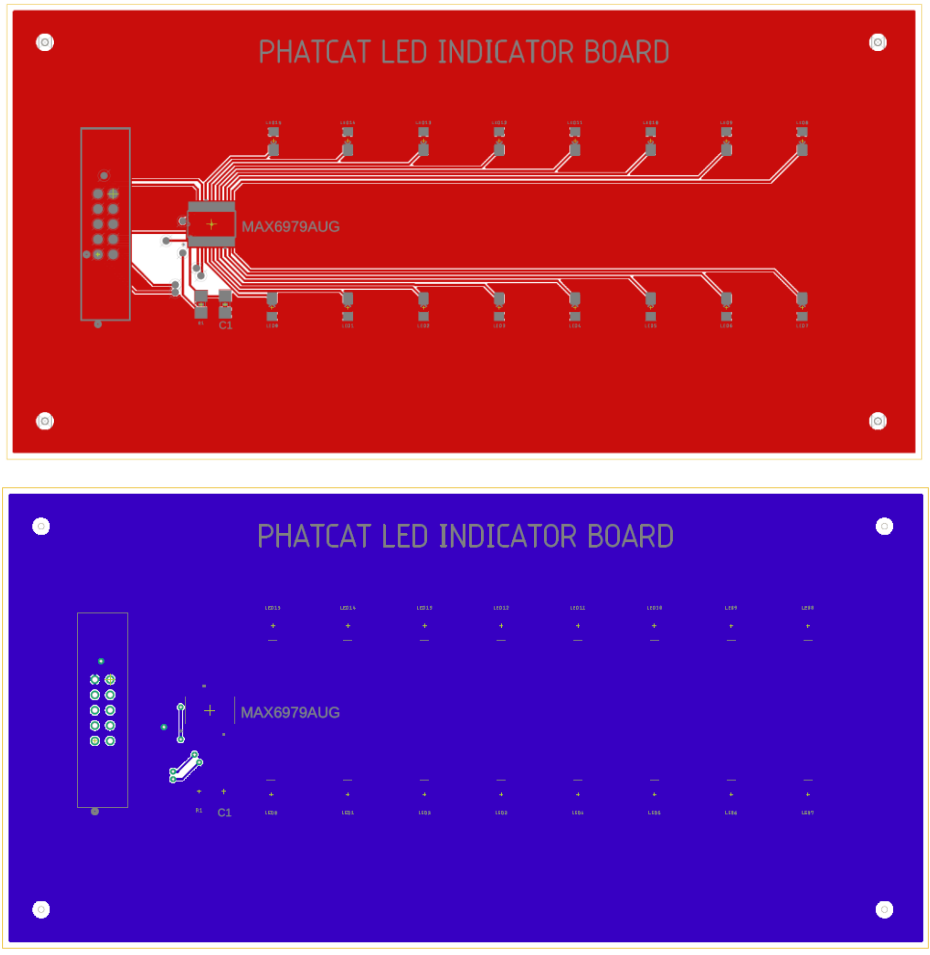


Fig. 8.6 LED Indicator Board Layout – Top (Red) and Bottom (Blue) Layers. Board Layout by Edward Millet.

ADC Breakout Board: The board layout seen in fig. 8.7 is for the TI ADS8588S analog to digital converter. The layout includes 8 input breakout pins to allow for analog signals on the left side and have the 16 digital pins on the output the data to another 16 breakout pins. The resistor and capacitor are 0603 packages which allow for a compact design. This layout will be duplicated and eventually placed in the main PCB board design. This initial layout will be for testing and developing the protection algorithms required for the relay. The main difference between this and the final board design is the removal of breakout pins on the digital side of the IC.

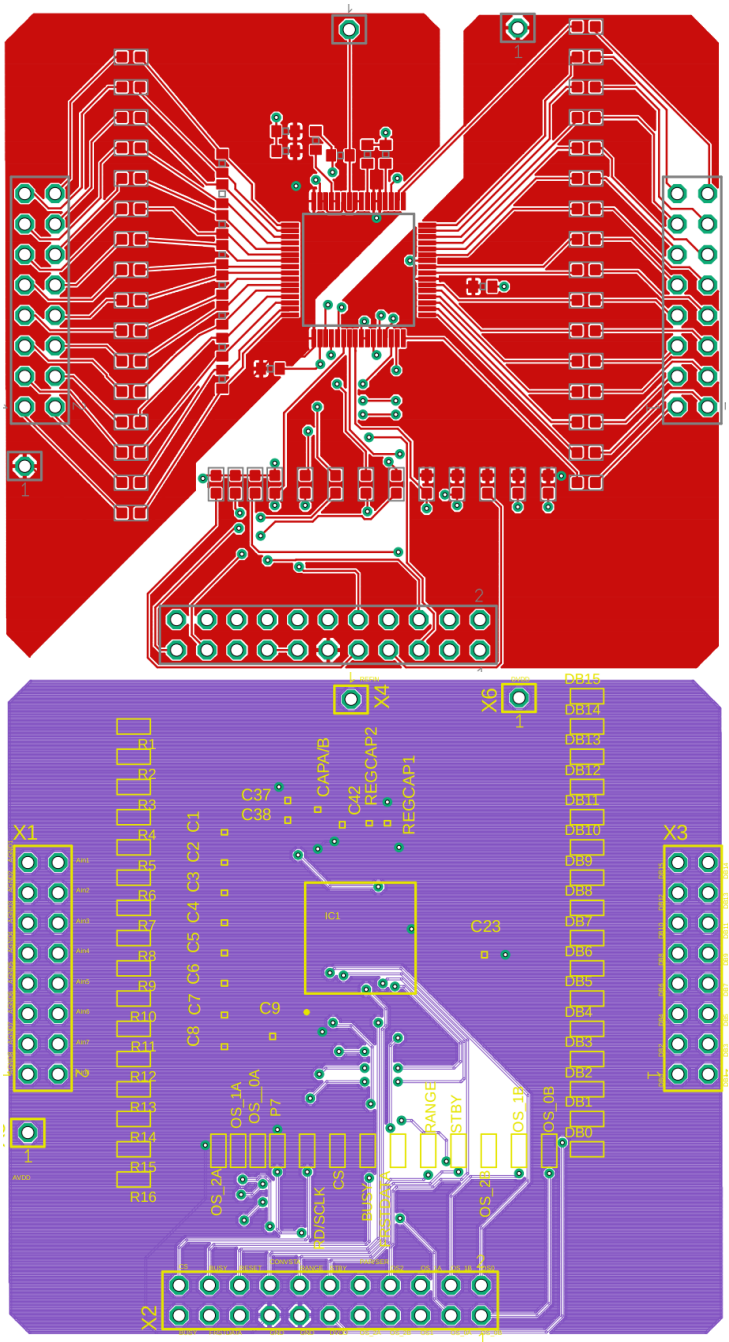


Fig. 8.7 ADS8885S breakout board layout, top (Red) and bottom (purple) layers. Layout by Daniel Hobbs.

There are two planes which separate into the DVDD and AVDD planes. This reduces the size of traces required for the power and the impedance of the plane. The AVDD plane can be seen on the left side of the board in figure 8.X and the DVDD is on the right. The GND plane is the bottom layer in blue. The large continuous GND plane allows for again, lower impedance which allows for the shortest return path. Since there are more traces on the 1st layer, the component names are displayed in fig. 8.7 but, it's worth noting that they are indeed on the top layer of the board.

Main Board: The Texas Instruments C2000 Delfino MCU F28379D LaunchPad development kit design is referenced for modification and implementation into the PHATCAT Main Board Design (fig. 8.8). The following design has a total of six routable layers: A Top Layer, VDD Layer, GND Layer, Route1 Layer, Route2 Layer, and a Bottom Layer. The six-layer board design will be the defining platform for PHATCAT's Main Board Design. The design may seem complicated, but logically it seemed more feasible to modify an existing design that has been tested and works, rather than creating a completely new design from scratch.

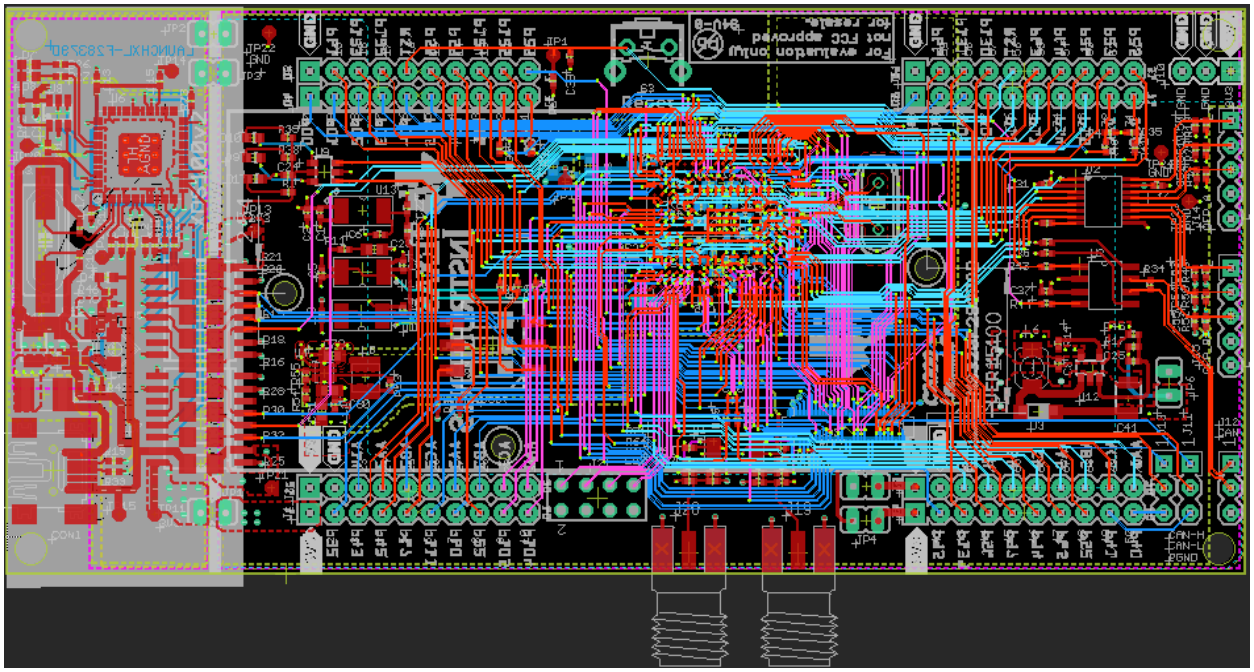


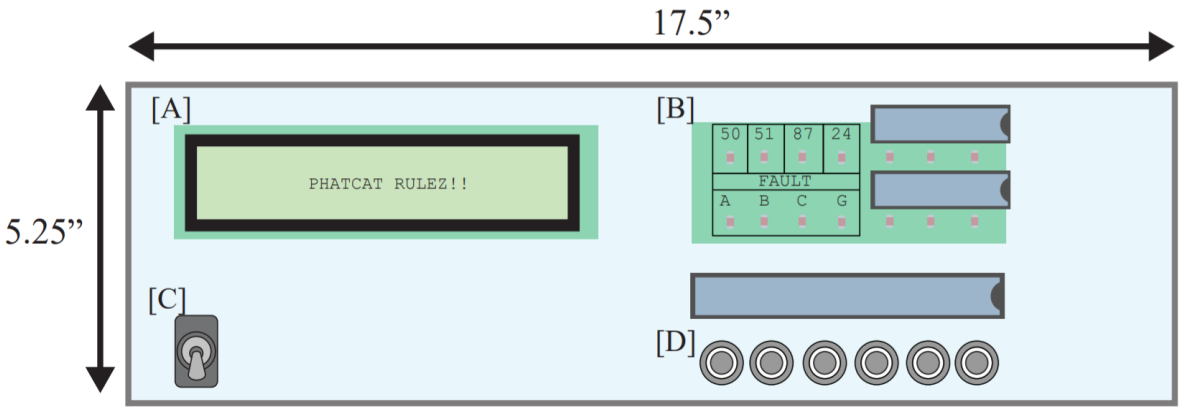
Fig. 8.8 TMS320F2837xD Dual-Core Delfino Microcontroller Board Layout. Reproduction permission requested for Texas Instruments.

8.4 Enclosure Design

The housing of PHATCAT will be design in such a way that is cost effective for the project but allow protection and durability to the relay. The initial housing will be a 3U sized relay box which will be easily mountable in a standing rack if necessary. The relay box will be made from steel and altered to contain the all the components in a manageable way. There is an assortment of vendors who sell standard sized relay boxes which can be expensive. There is a potential vendor who is willing to donate an enclosure box that will become the initial building block of the design.

Plexiglass will be mounted in a manner that allows for easy removal by using four small screws and tabs to secure the glass to the steel box. This will allow for ease of access to the various components in the box as it gets constructed and tested. For the terminal strips, LCD screen and other mounted components, they will have pre-tapped holes drilled into the plexiglass providing an easy way mount each component. The LCD will have a drop-in slot cut into the plexiglass which provides access to the screen and a clear view for the user. The plexiglass can be cut by utilizing the laser in the Innovation Lab located on campus which

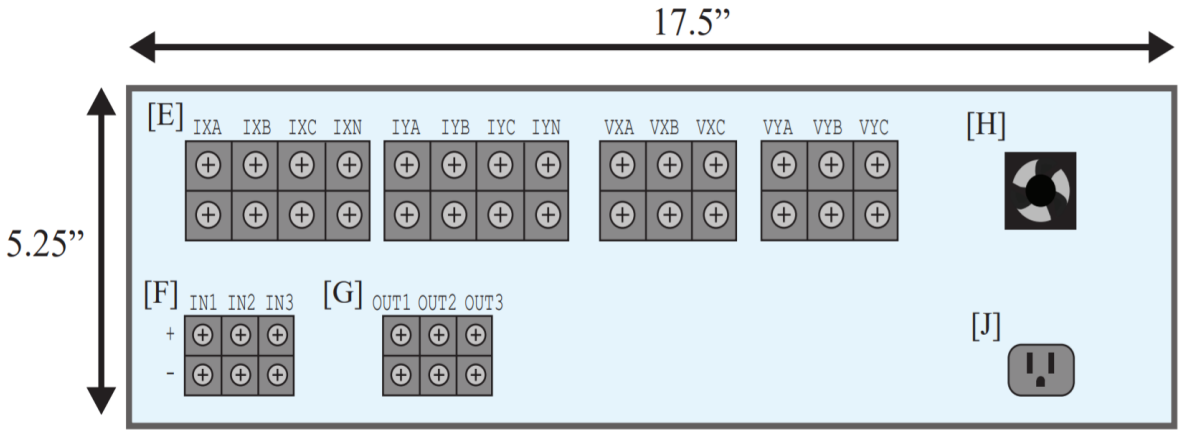
will be accurate and clean. Fig. 8.9 is providing an illustration of how the layout of the front panel will look after assembly.



[A] – LCD, [B] – LEDs & description strip, [C] – Power switch (cover not shown), [D] –Push buttons

Fig. 8.9 PHATCAT Front Panel Illustration by B. Ross

The back of the steel box will be removed and replaced with transparent plexiglass to provide a unique element for presentation. The same will be replicated on the front panel where plexiglass will be used, and the LCD mounted to it. On the back side of the relay, an assortment of terminal strip connectors will be mounted to the plexiglass. They will ensure safe and secure connection between the test equipment and the inside components. To design the PCB in a more efficient manner, both the current and voltage transformers will be mounted separately from the board. The wires that will be connecting the devices will be designed in consideration of reducing inductance in the jumper by using minimal length and keep the transformers close to the PCB and rear side of the enclosure. Fig. 8.10 provides an illustration of the layout for the rear side of the relay.



Analog Inputs. [F] Sense Inputs. [G] Output contacts. [H] Cooling Fan. [J] Power connection.

Fig. 8.10 PHATCAT Rear Panel Illustration by B. Ross

It’s common in professional grade relays to split the enclosure into a few different levels by adding a shelf for the assortment of components to be mounted on. By mounting the PCB on a removable shelf, it will provide an easy to connect wires and modify parts with ease. The transformers will be mounted to a separate shelf to provide ease of removal and maintenance of the components. The wires connecting the transformers and PCB will be organized in a way that allows for connecting the two levels but not interfere with the

removable shelf. Fig. 8.11 is a design concept of how the layout inside the enclosure is foreseen. This layout will provide plenty of space for thermal dissipation of heat and the routing of connection wires.

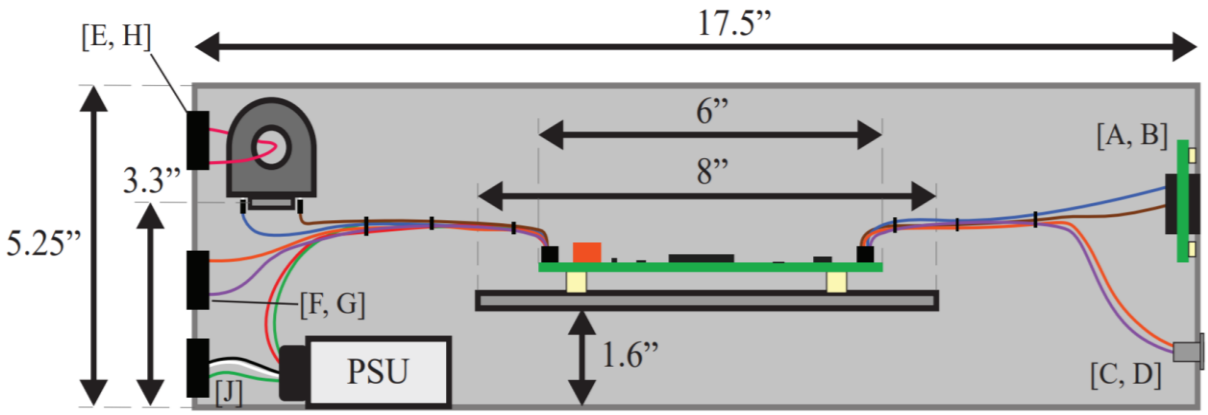


Fig. 8.11 PHATCAT Side View Illustration by B. Ross

9. PROTOTYPE SYSTEM TESTING

In this section, guidelines are given for testing the various modules of PHATCAT's hardware and software. These include the necessary hardware, procedures, and expected results.

9.1 PROTOTYPE HARDWARE TESTING

The following section contains the procedures for testing the major components of PHATCAT's Hardware.

Equipment:

- PHATCAT
- Tektronix DMM 4050 6 ½ Digit Precision Multi-meter (or equivalent)
- Tektronix MSO 4034B Digital Mixed Signal Oscilloscope, 350 MHz, 4 Channel (or equivalent)
- A Desktop PC with the PHATCAT Desktop Application
- A mini USB-B cable
- Doble F6150e OR
- SEL-AMS with SEL-5401 Software OR
- An equivalent low-voltage function generator or protective relaying test kit.

Overvoltage Protection: PHATCAT's output contacts, analog current inputs, analog voltage inputs, and DC sense inputs are designed to withstand a 50% overvoltage for at least 15ms. For the sense inputs and analog inputs, this overvoltage can be applied continuously. The procedure to test the overvoltage protection is outlined below:

1. Analog Current Inputs: Do not connect a constant-voltage supply to PHATCAT's primary current sensing terminals. They are intended for use with a constant current source and have a very low input resistance.
    a. Apply a 15V peak sinusoid between the two pins fastening the CTs to the main board. Measure the voltage differential across the sensing resistor. It should be between 10 and 12V peak. This confirms that the ADC is protected against differential mode overvoltage conditions on the current sense circuits.
    b. Apply a 15V peak sinusoid with respect to PHATCAT's ground to each pin. Measure the voltage at either side of the sense resistor with respect to ground, it should be within 10-12V. This confirms that the ADC is protected against common mode overvoltage conditions on the current sense circuit.
2. Analog Voltage Inputs: PHATCAT's voltage sensing protection can be tested with either the primary side screw terminals or the secondary pins on the main board.
    a. Apply either a sinusoid of either 143V peak on the primary side screw terminals or 15V peak on the secondary side pins. Measure the voltage differential across the protected 180 ohm resistor. It should be within 10-12V. This confirms that the ADC is protected against differential mode overvoltage conditions on the voltage sense circuit.
    b. Apply either a sinusoid of either 143V peak to the primary side screw terminals or 15V peak on the secondary side pins with respect to PHATCAT's ground. Measure the voltage at either side of the protected 180 Ohm resistor with respect to ground, it should be within 10-12V. This confirms that the ADC is protected against common mode overvoltage conditions on the voltage sense circuit.
3. DC Sense Inputs: PHATCAT's sense input protection can be tested by applying a DC voltage at the screw terminals
    a. Apply a 190VDC differential across the sense input. Measure the voltage across the resistor-diode branch of the sense input circuit, it should be regulated between 5-7V.
4. Output Contacts: While other circuits in PHATCAT are capable of withstanding continuous overvoltage, the output contacts **are not**. It is recommended to test this circuit with a voltage source

that will not provide current. If testing with a source that will, it is required that a large (160kOhm +) resistor be placed in series with the source. This allows the voltage clamping capability to be verified without the need for a very brief test.

a. Apply a 190VDC differential across the output contact with the contact in the open position. The voltage across the contact should be regulated near 152V, though this amount will increase linearly with the current provided by the source. See the Vishay P6SMB160CA-E3/52 datasheet for detailed information as to the short-time withstands of the protection diodes.

Current Sensing: The goal of this testing is to ensure that the current transformers for the sense inputs operate as intended and meet specifications of the project requirements. To test the current transformer the following steps should be followed. It's important to note, do not allow the secondary side of the transformer to be left in an open condition. This can severely damage the transformer.

1. Connect the test kit to the rear terminal corresponding to the input desired to be tested. Connect a probe from the oscilloscope in respect to sense resistor. This is for the preparation to record the voltage across the sense resistor.
2. Apply 5A and take the initial reading of the voltage across the sense resistor. After 30 minutes, measure the output again and compare the results. Use the following equation $V_{sense} = \frac{I_{in}}{2500} 492\Omega$ to calculate the expected voltage across the sense resistor where $I_{in}$is the current being supplied. The expected V_{sense} should be around 930-1040mV.
3. To find the input impedance of the current transformer, use the V_{sense} voltage found in step 2 and the I_{in} be 5A. Use the following equation to find the input impedance $Z_{in} = \frac{V_{sense}}{2500 * I_{in}}$. Allowing V_{sense} be 980mV and I_{in}=5A, the input impedance should between $70\mu\Omega$-$85\mu\Omega$.
4. Next, set the test kit for 30A, and record the initial output reading for V_{sense} . Continue the 30A input for 2-3 seconds and again record the V_{sense}. Using the equation from step 2, let the I_{in} be 30A and calculate the expected values. In this test case, the V_{sense} should be between 5.60-6.2V. To achieve a 30A environment with a current limited test kit, the rear side of PHATCAT can be removed to directly loop the test kit lead through the primary hole of the current transformer. Each loop will multiply the current flow proportionate to the number of loops. (E.g, 3 loops at 10A provides a total sum of 30A)

Voltage Sensing: The goal of this testing is to ensure that the voltage transformers for the sense inputs operate as intended and meet specifications of the project requirements. The following equipment will be required.

1. Connect the test kit to the rear terminal corresponding to the input desired to be tested. Connect a probe from the oscilloscope in respect to 180Ω resistor after the protection diodes.
2. Apply 67V on the primary side of the transformer and measure the output voltage with the oscilloscope on 180Ω resistor. The equation $V_{Out} = \frac{1}{9.5} V_{in}$ can be used to calculate the expected voltage value. In this test case, the V_{Out} is should be between 6.7-7.5V.
3. Continue the 67V for 30 minutes and measure the output again and compare to the initial value. Use the same equation from step 2 to calculate the expected V_{Out}.
4. To find the input impedance of the voltage transformer, use the following equations: $I_{out} = \frac{V_{Out}}{5130}$, $Z_{in} = \frac{67}{I_{out}}$. Where I_{out} is calculated using the V_{Out} found in step 2 and Z_{in} is finally found using the I_{out} found in the 1st equation. The expected Z_{in} should be between 46-52kΩ

ADC: Due to the large number of signals, it is recommended to test the channels one at a time, after verifying the current and voltage sensing circuits as well as the LCD.

1. A 60Hz sinusoidal nominal signal (5A for current sense, 67V for voltage sense) should be applied at the analog input screw terminals for the desired channel.
2. The LCD should read the nominal value times the user-defined CT or PT ratio, with a 5% accuracy. This verifies proper magnitude readings.
3. Apply a second, similar signal with a known phase shift to a different analog input. Compare the angular difference between the two phasors. It should be accurate to within 0.1 degrees. Note that, because PHATCAT does not share a common angular reference with the test equipment, the absolute phase angles may vary. This verifies proper timing of the ADC.

LCD: The LCD is tested by verifying that all characters illuminate and that PHATCAT is updating the fields with new measurements.

1. On startup, PHATCAT briefly illuminates all characters on the display. Use this functionality to verify that all characters are functioning.
2. Apply a known analog input to the current or voltage channels and verify that PHATCAT is updating the screen with new measurements. This ensures that PHATCAT's microcontroller is communicating with the LCD

LEDs: The LEDs are tested by verifying that all LEDs illuminate and that PHATCAT is able to control them appropriately.

1. On startup, PHATCAT briefly illuminates all LEDs on the display, use this functionality to verify that all LEDs are functioning.
2. Trigger a fault that causes a protective element to operate, or trigger one of the user-defined logic equations that control the LEDs. The simplest way to do this is to define user equation 'LED1 = PB1' so as to control the LED with a front panel push button. This ensures that PHATCAT's microcontroller is communicating with the LED board.

Output Contacts: The Output Contacts are tested by connecting a load circuit across the contacts and verifying that the load circuit operates as intended.

1. Apply a 125VDC difference across the Output Contact screw terminals to test their durability.
2. Connect a load circuit across the relay contacts. To break a 2A load, it is recommended to apply a 12V potential. Please refer to the Switching Capacity Graph in the Performance Data Section within the Kemet EE2-12NU datasheet. In order for the relay contacts to break a 2A load the potential must not exceed 24V.
3. Measure the voltage drop across the relay contacts which is estimated to be 0.15V. The voltage drop must be less than 1V.
4. Define a logic equation within PHATCAT's setting to control the output contacts via a push button.
5. Press the push button to toggle the output contacts. The relay contacts should close, energizing the load circuit.
6. Press the push button once more. The relay contacts should open, breaking the 2A load circuit and thus de-energizing the circuit.

Sense Inputs: The Sense Inputs are tested by applying a potential difference across the Sense Input screw terminals and the microcontroller is able to read the input signal.

1. Apply a nominal 125VDC potential to the Sense Input screw terminals.

2. The measured current is estimated value is 2mA ±10%. The current drawn at 125VDC nominal voltage should be less than 10mA.
3. Define a logic equation within PHATCAT's settings to read the input and illuminate an LED as an indicator that the input was sensed.

Push Buttons: The Push Buttons are tested by PHATCAT reading in when the buttons are pressed and by illuminating the LED Ring located on the front of the push buttons.

1. A white LED should illuminate for every pushbutton when PHATCAT is turned on.
2. Define the logic for the Push Button within PHATCAT's settings to toggle on and off an LED indicator when the button is pressed.
3. Verify the proper function of the power switch by using it to toggle PHATCAT on and off.

Power Electronics: The goal of this testing is to ensure that the voltage for the individual 12, 5 and 3.3 voltage levels operate as intended and meet specifications of the project requirements. It is important to note that the ripple in the power supply output for 5V be measured to ensure it will not exceed a 0.50V variance. To test the power electronics the following steps should be followed:

1. Ensure all power is turned off and begin connecting the power supply according to the schematic. By turning off the power while connecting the circuit and probes, it will reduce any chance of short somewhere and possibly damaging components.
2. To test the output voltage of each power supply level, connect a DMM to each individual voltage level. The 12V output should be within 11.88-12.12V. The 5V supply should be within 4.94-5.005V. The 3.3V supply should vary from 3.1-3.5V.
3. Connect one probe of the oscilloscope to the output of the 12V power supply. Connect another probe to the output of the 5V power supply.
4. Turn on the power supply and measure the peak-to-peak voltage on the oscilloscope for both the 12V and 5V outputs. Set the trigger voltage slightly higher than the nominal expected voltage level being tested. This will allow for the scope to trigger on the ripple. If the value is small, the oscilloscope can be placed in AC coupling mode to filter out the DC and focus on the ripple of the input.
5. The expected voltage should not vary outside the range of 4.75-5.25V to ensure the accuracy of the ADC is constant. Should the 5V power supply vary outside the range, the accuracy of the digital converter cannot be guaranteed resulting in analysis errors.

9.2 Prototype Software Testing

The following section contains the procedures for testing PHATCAT's software as well as its companion desktop application.

9.2.1 PHATCAT Software Testing

The goal of the following tests is to verify proper performance of PHATCAT's on-board software. The sensitivity and selectivity of the protective algorithms is of primary concern. Software testing should be conducted after hardware testing, as proper software function requires proper hardware function. These tests assume some user familiarity with the test kits typically used to test protective relays as well as familiarity with short-circuit analysis. These are prerequisite for understanding PHATCAT's operation, and there are a great many academic resources available on such topics.

Equipment:

- PHATCAT
- A Desktop PC with the PHATCAT Desktop Application
- A mini USB-B cable
- Doble F6150e OR
- SEL-AMS with SEL-5401 Software OR
- An equivalent low-voltage function generator or protective relaying test kit.

There are two methodologies for providing simulated power system signals to PHATCAT. The first involves the use of a professional grade test kit, such as the Doble F6150e. In this case, the appropriate signals can be sent by connecting the Doble directly to the screw terminals on the back of PHATCAT. However, such test sets can be very expensive, so an option is made available to allow for testing without the need for equipment that can inject large (30A) currents. By bypassing the CTs and PTs on-board PHATCAT, a low-voltage function generator can be used. Simply disconnect the two-pin plugs used to connect the instrument transformers and replace them with the function generator leads. The SEL-AMS is a function generator designed for this purpose that has accompanying software and functionality to make this sort of testing easy. When using the low-voltage test interface, the following gains should be used:

$$V_{V(LV)} = .0351 * V_{PRI} \quad ; \quad V_{I(LV)} = 0.1560 * I_{PRI}$$

For example, to simulate a primary side CT measurement of 5A RMS, 0.78V RMS should be applied to the main board directly. Similarly, to simulate a primary side PT measurement of 67V, 2.35V RMS should be applied to the main board.

Metering: Before testing any protective functions, PHATCAT's metering should be tested. This verifies that the core signal processing (frequency tracking, FFT) is functioning and that the user-defined values such as primary side CT ratio and PT ratio are entered correctly. The phasors given in table 7.3 are recommended as the metering test case.

Table 7.3. Test Case for PHATCAT's Metering Functionality

Input:	**IAW**	**IBW**	**ICW**	**INW**	**IAX**	**IBX**	**ICX**	**INX**
Value:	5.1 ∠ 0°	5.1 ∠-120°	5.1 ∠120°	0.1 ∠0°	5.0 ∠ 0°	5.0 ∠ -120°	5.0 ∠ 120°	0.1 ∠0°
Input:	**VAW**	**VBW**	**VCW**		**VAX**	**VBX**	**VCX**	
Value:	67 ∠ 0°	67 ∠-120°	67 ∠120°		66 ∠ 0°	66 ∠ -120°	66 ∠ 120°	

Send these analog signals to PHATCAT, either via a test kit or function generator (in which case you will have to refer these quantities to their low-voltage counterparts). The voltages and currents should be multiplied times the user-defined CT and PT ratios and displayed on the LCD. The frequency of the signals used should be properly tracked. Check the transformer

Overcurrent Testing: The overcurrent elements should be tested in two ways, their sensitivity and their operating time. The operating time may be difficult to ascertain unless a relay test kit or specialized function generator is used. Such equipment is designed to begin a timer when a fault is played to the relay, and provides an operating time as a part of the test results. There are no rigorous guidelines for testing overcurrent settings, but there are some general guidelines.

a. Define a Boolean expression for one of the output contacts (OUT1) to operate based on the overcurrent elements to be tested. Provide this as a feedback output to any test equipment capable of measuring operation time.

b. Pick a set of analog values for your test based on the overcurrent relay's operating characteristics. There are several guidelines to follow when doing this:
    i. The easiest method for choosing analog values is to use short-circuit software, such as ASPEN Oneliner, to simulate faults around a simple power system with realistic values. The resulting phasors can then be used in the test. It is recommended to simulate external (i.e., not inside the transformer) faults so as not to operate the current differential instead. If the overcurrent is intended to serve as a backup for the differential, be sure to disable the differential when testing.
    ii. If you have a test kit or function generator that supports feedback of a contact, use it to evaluate the operating time of the output contacts. The front panel of the relay will indicate the protective element's operation, but more precise timing is needed to get an accurate measurement. This has the added advantage of including the contact operating time, which is a necessary part of any real-world protection scheme.
    iii. For instantaneous elements, you should choose analog values that exceed the set pick up values by at least 10%. Be sure to run the test for longer than any definite time delays.
    iv. For testing time-inverse overcurrent relays, choose analog values that are at least several multiples of the pickup current. Smaller values yield very high pickup times and are better suited for tripping on extended overloads rather than for faults. The curve equations can be used to provide estimated operating times, add 2 ms to the curve result to account for relay contact operating time.
    v. For testing phase overcurrent elements, a three-phase or line-to-line fault is recommended. A ground fault will produce zero-sequence currents that are likely to make any ground elements operate before the phase overcurrent.
    vi. For testing residual or neutral overcurrent elements, a single line-to-ground fault is recommended.

Current Differential Testing: There are up to four regions in which the differential can be tested: the minimum pickup value, values in the slope 1 region, values in the slope 2 region, and values above the unrestrained pickup value. Refer back to fig. 3.14 for a depiction of the current differential operation characteristic.

a. Define a Boolean expression for an output contact connected to the sense input of a test kit allowing it to be operated by the differential.
b. Define parameters for a theoretical transformer to be tested. A 56MVA, 69/13kV DAB-Y transformer is recommended, as it will ensure that the connection compensation and zero-sequence removal occurs properly.
c. Create a load condition test where the voltages and currents are balanced and 1 p.u. in magnitude and play it to PHATCAT. The differential should not operate. This verifies that the scaling and compensation is correct, as it does not produce any false residual.
d. Because PHATCAT calculates its restraint based on whichever transformer winding has the higher normalized current rating, the recommended testing methodology is as follows:
    i. Use the source-side (69kV in the recommended case) to define the desired value for I_R. Make the high-side current phasors a balanced set with magnitude I_R.
    ii. Use the load-side (13kV) to define the value for I_{op}. The normalized current (1A at rated load) should be less than that on the source side, so that the high side current is used for the restraint. Then, use the user-defined characteristic to find a value of I_{op} that is above the threshold for the given restraint and one that is below. Subtract the used I_R for each phase from this to obtain the desired low side currents.
    iii. For each of the three regions (minimum pickup, slope 1, slope 2), play two tests: one where the operating current exceeds the restraint threshold, and one where it does not. This verifies that PHATCAT is restraining the differential properly.

iv. Play a test where the source-side currents exceed the unrestrained pickup value but not the tripping threshold for the restrained differential. The load-side currents should be zero. This confirms that the unrestrained differential operates even when the restraint does not.

Harmonic Blocking Testing: The goal of the harmonic blocking is to ensure that the differential does not operate when there is a false differential due to nonlinear behavior in the transformer or CT cores. Not all test kits will allow easily controlled generation of harmonics. If this is the case, it is recommended that real-world event data for a transformer energization or saturation event be used. The current differential should be tested before the harmonic blocking, as improper differential behavior may cause false negatives.

a. Define a Boolean expression for an output contact connected to the sense input of a test kit allowing it to be operated by the differential.
b. Define parameters for a theoretical transformer to be tested. A 56MVA, 69/13kV DAB-Y transformer is recommended, as it will ensure that the connection compensation and zero-sequence removal occurs properly. If real-world event data is used, instead define values based on the transformer from which the event was taken. Additionally, define percentage thresholds for the harmonic blocking. 15% is a commonly used threshold.
c. If the test kit supports controlled generation of harmonics, begin with a base case from the current differential testing and add harmonic content that exceeds the threshold. Perform a separate test for 2^{nd}, 4^{th}, and 5^{th} harmonics to ensure each element works properly.
d. If real-world event data is used, simply play the event file to the relay. It is recommended to use software such as Matlab to ascertain the harmonic content of the event beforehand, to be sure it meets the threshold.
e. For either of the tests in (c) and (d), the harmonic blocking LED should briefly illuminate, but the relay should not operate. This verifies that the harmonic blocking properly supervises the current differential.

Overexcitation Testing: The Volts/Hz element can be tested by using a combination of overvoltage and underfrequency to exceed the set percentage threshold.

a. Define a Boolean expression for an output contact controlled by the Volts/Hz element to be read by the test kit.
b. Play a steady-state condition, where the winding voltages and system frequency are near 1 p.u. and ensure that the element does not operate.
c. Play an event where the pickup value is exceeded. A realistic case would be a 150% overvoltage on a 500/230kV transformer during a period of light loading (5% nominal). Be sure to play the test for long enough to exceed the user-defined pickup time. Use the sense input functionality to verify the operating time.

9.2.2 DESKTOP APPLICATION TESTING

The ability to save and load settings is a crucial part of the PHATCAT device and will make it easy to set up the desired configurations for the user.

Settings File Creation:

Procedure

1. Open the application
2. Navigate to file create a new file or open the demo file
3. View the settings tree structure on left side of screen
4. Click on various primary settings to open their sub settings in the right panel
5. Select the sub settings in the right panel you would like to modify

6. Modify settings to suit your needs
7. Navigate to file menu and save the modified settings
8. Restart the application and verify that the settings can be loaded back into application

The boolean parser will parse the logic that the user enters in the desktop application and use it to configure the PHATCAT device.

Test Boolean Parser:

1. To simplify testing the Boolean parser a demo file can be loaded and used
2. When a setting is opened and modifiable it will allow the user to alter it. Otherwise it will be grayed out.
3. If user hovers over a setting a brief description of the setting will populate on screen
4. Each setting has acceptable parameters that can be passed in as logic. These can be viewed by hovering over setting and in tooltip.
5. If invalid expressions are entered the user will be notified and asked to correct
6. If valid expressions are entered, they can be used to configure the settings on the PHATCAT
7. After all settings have been modified to user specification and no error in logic they can be sent to device.

When the computer application is connected to the PHATCAT device the settings can be sent and received between the desktop application and the PHATCAT.

PHATCAT Interface:

1. Connect the computer to the PHATCAT with mini USB-B connecting cable
2. Once connected the desktop application will notify the user it's connected to PHATCAT
3. The desktop application can import the settings currently on the device
4. The settings on the desktop application can be sent to device and notify the user when they have
5. After sending setting configurations to device unplug the from device and reconnect to verify settings through new import

10. ADMINISTRATIVE CONTENT

This section contains both the budget information and project progression milestones set forth by the team.

10.1 PROJECT BUDGET

The following budget represents a cost estimate for the project based on the design implementations currently under consideration. It provides margin for spare parts which may be needed in case parts are unintentionally destroyed. Two development boards are purchased to avoid work interruptions in the event of a damaged board as well as to support different team members simultaneously working on either software development or integration of subsystems with the microcontroller. Margin is added to the PCB costs to account for costs arising from both multiple design iterations and for any premium that must be paid if short lead-times are required. The goal is to provide a conservative estimate of the financial resources required for the entire project, not just the fabrication of the final prototype.

Table 10.1: Project Budget

Feature	Quantity	Unit Cost	Total	Notes
Enclosure	1	$50.00	$50.00	Hardware, screw terminals, etc.
Display	1	$25.00	$25.00	
Power Switching	1	$15.00	$15.00	Buttons, cables, etc.
Development Board	2	$120.00	$240.00	x2 to parallel design processes
Front Panel LEDs	20	$0.30	$10.00	Extra for drivers needed
Front Panel Switches	5	$5.00	$25.00	
PCB Fabrication	N/A	$250.00	$250.00	Considers multiple iterations
Microcontroller	2	$20.00	$40.00	Chip only.
Power Supply	1	$30.00	$30.00	Considers extra converters
Current Sensing	10	$15.00	$150.00	
Voltage Sensing	10	$1.00	$10.00	
Board Protections	1	$50.00	$50.00	Used throughout board.
Output Contacts	3	$20.00	$60.00	
EMI Shields	10	$0.25	$2.50	
Soldering Wire	2	$3.50	$7.00	
Sense Inputs	5	$1.00	$5.00	
Misc. Components	N/A	$20.00	$20.00	Resistors, capacitors, diodes, etc.
ADC/DSP	2	$30.00	$60.00	
Total expected cost			**$1049.50**	

The biggest risks of budget violation are the damaging of development boards and the introduction of new features that require additional hardware. Opportunities for budget outperformance lie the implementation of cheaper methods for implementing current sensing, board protection, and output contacts. Another opportunity is the development of a correct PCB design in a timely manner that does not require an escalated lead time or multiple design cycles.

10.2 MILESTONES

There are several key milestones required for successful project completion. There are two main components, project documentation and prototyping execution. While senior design 1 and 2 decouple these into consecutive processes, this team will be performing the two in parallel. Due to the variety of issues

that are discoverable only through physical prototyping, it is desirable to order selected components, test their function, and begin their integration with other selected components as early as possible. Tables' 10.2 and 10.3 detail major milestones for both project documentation and prototyping execution, respectively.

Table 10.2: Project Documentation Milestones

Project Documentation			
Task	**Start Date**	**Planned End Date**	**Required End Date**
Initial Design Document	1/8/2019	1/27/2019	2/1/2019
Initial Design Document 2.0	1/8/2019	2/10/2019	2/15/2019
60-Page Milestone	1/8/2019	3/24/2019	3/29/2019
100-Page Milestone	1/8/2019	4/7/2019	4/12/2019
Final Report	1/8/2019	4/21/2019	4/22/2019

Table 10.3: Prototyping Execution Milestones

Prototype Development			
Task	**Start Date**	**Planned End Date**	**Required End Date**
Core Component Selection	1/8/2019	3/04/2019	3/29/2019
Individual System Design	2/25/2019	3/24/2019	3/31/2019
Individual System Testing	3/11/2019	4/1/2019	4/12/2019
System Interfacing	3/25/2019	4/14/2019	4/22/2019
PCB Design	3/3/2019	TBD – Senior Design 2	TBD – Senior Design 2
PCB Testing	TBD – Senior Design 2	TBD – Senior Design 2	TBD – Senior Design 2
Prototype Completion	TBD – Senior Design 2	TBD – Senior Design 2	TBD – Senior Design 2

There will no doubt be overlap and reiteration of the various processes associated with prototyping, but these milestones serve as general guidelines.

11. PROJECT SUMMARY AND CONCLUSION

PHATCAT began with the idea of an intelligent device capable of ascertaining a power system transformer's condition as well as detecting and facilitation response to a variety of power system disturbances. It is meant as an educational resource, with the hopes that new protection engineers might gain a deeper understanding of microprocessor relays.

PHATCAT possesses the means for ascertaining power system signals from instrument transformers via its analog front-end. It then produces phasor representations of these quantities through ADC and FFT. It can sense standard 125VDC logic-level inputs and switch external circuits via mechanical contacts. In order to protect itself against harsh industrial conditions, both galvanic isolation and overvoltage protection are provided for all inputs and outputs.

These electronics facilitate practical implementation of several widely-used protection algorithms. Current differential protection is provided as the main method for transformer protection, with proper compensation for various transformer connections and turns ratios. A restraint characteristic increases the algorithm's resilience against sources of error such as static CT error, LTC variation, and CT saturation. Harmonic blocking is available to prevent false operations during transformer energization or saturation. Instantaneous and time-inverse overcurrent protection is also provided, to be used as a backup function for both the current differential and for faults external to PHATCAT. Overexcitation protection allows for protection against core saturation events that may cause excessive heating.

PHATCAT is also prepared to interface with system operators, streaming key quantities to its LCD and indicating important operations via its LEDs. Push-buttons allow for triggering of user-defined events. In fact, all of PHATCAT's functionality is user-customizable. A desktop application allows for key values, such as instrument transformer turns ratios and protection set points to be set. It also supports logic equations, which provide a powerful and flexible framework for use in a variety of applications and power system topologies.

PHATCAT possesses all of the key technologies needed for protecting power system transformers, and thorough documentation has been provided that encapsulates all of the information necessary for other engineers to replicate its design. Reference has been made throughout to industry practice, and, while PHATCAT is not designed with all of the robustness of an industrial-grade microprocessor relay, it nevertheless serves as a demonstration of many concepts that are key in the fascinating world of power system protection.

APPENDIX A – COPYRIGHT PERMISSIONS

For all material reproduced from an outside source, a copyright request has been sent to the copyright holders. For material for which permission has been granted, "reproduced with permission of [copyright holder]" appears in the figure/table caption. Both the request and approval are documented in this section. For material which a request has been sent but no response received, "permission for reproduction requested from [copyright holder]" appears in the figure/table caption. Other formatting is at the request of the copyright holder. The request is documented in this section.

Request for Electromechanical Relay Image (Fig. 2.2):

Contact ABB

Contact information

First Name: Brett

Last Name*: Ross

E-mail*: brettross96@knights.ucf.edu

Company / Organization*: University of Central Florida

Country or region*: United States of America

State*: Florida

ZIP code*: 33511

Phone: + 8134316220

Eg. 44 7911123456 (Start with International dialing code)

Message

My inquiry concerns*: General

Message*

Good evening,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.

We are hoping to obtain permission for the following images:

https://www07.abb.com/images/librariesprovider85/default-album/em_relay.jpg

Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,

Brett Ross

* I accept the terms and conditions.

Request for GE L30 Image (Fig. 2.3):

Copyright Usage Request for Educational Purposes - GE L30 Image

BR Brett Ross
Today, 2:06 PM
Allison.J.Cohen@ge.com

Reply all

Good afternoon,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.

We are hoping to obtain permission for the following images:
http://www.gegridsolutions.com/multilin/pr/UR540/UR-Ease-02_thumb.jpg

Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,

Brett Ross
813.431.6220
Candidate for *B.S. of Electrical Engineering* at **UCF** (SU '19)
brettross96@knights.ucf.edu
Protection & Controls Engineering Co-op at **Duke Energy**
Brett.Ross@duke-energy.com

Thomas, Vincent (GE Renewable Energy) <vincent.thomas2@ge.com>
Mon 3/11, 9:14 AM
Cohen, Allison (GE Renewable Energy) <Allison.J.Cohen@ge.com>; Brett Ross

Reply all

Flag for follow up. Completed on Wednesday, March 13, 2019.

2 attachments (919 KB) Download all Save all to OneDrive - Knights - University of Central Florida

Hello Brett,

Thank you for check with us regarding use of this image.
You have my permission to use the image of the UR protection relay for the purposes you have outlined. Seeing at though you link a simple thumbnail of this relay, I have also included a slightly higher res versions of the relay.
(right facing and left facing examples).

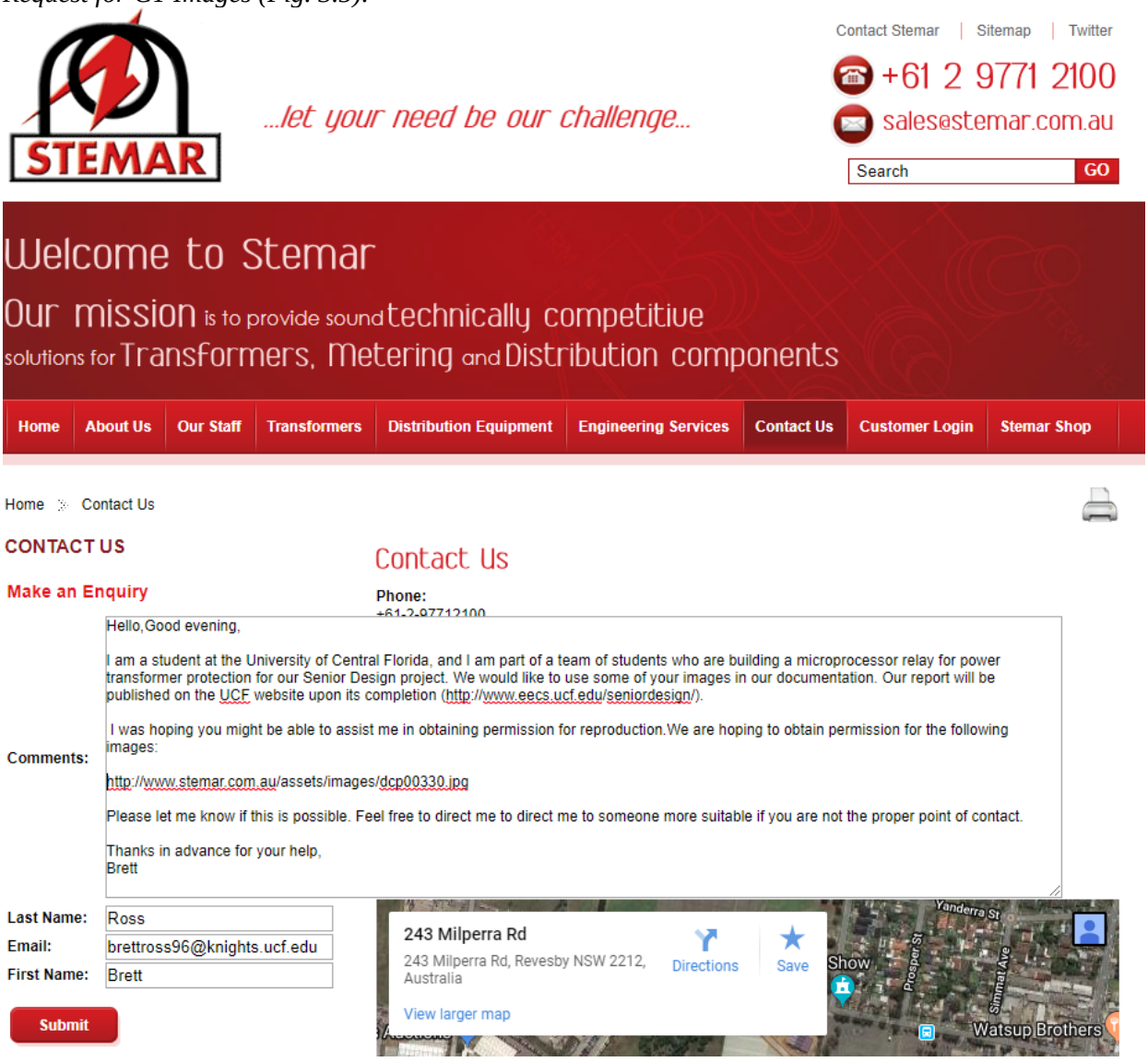
Best of luck with your Senior Design project!

Regards,

Vincent Thomas
Marketing Director
GE
Grid Solutions

647-407-3434

Request for CT Images (Fig. 3.5):



Request for Excitation Curve Images (Fig. 3.7):

Name

Brett Ross

Email

brettross96@knights.ucf.edu

Comment or Message *

Good evening,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.

We are hoping to obtain permission for the following images:

http://voltage-disturbance.com/wp-content/uploads/2018/08/EC2.png

Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,
Brett

Contact Request from Vol-Disturbance Website

A admin@voltage-disturbance.com
Mon 3/4, 8:50 AM
Brett Ross

Reply all

Flag for follow up.

That is fine.

On 2019-03-02 16:53, Brett Ross wrote:
> NAME
>
> Brett Ross
>
> EMAIL
>
> brettross96@knights.ucf.edu
>
> COMMENT OR MESSAGE
>
> Good evening,

Request for CCVT Schematic (Fig 3.8):

Copyright Usage Request: Figure from Energies Article

Brett Ross
Today, 9:46 PM
chenbin@cqu.edu.cn; dulin@cqu.edu.cn

Reply all

Good evening,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.

We are hoping to obtain permission for the following images:
Figure 1 from this article: https://www.mdpi.com/1996-1073/10/3/357/htm

Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,

Brett Ross
813.431.6220
Candidate for *B.S. of Electrical Engineering* at **UCF** (SU '19)
brettross96@knights.ucf.edu
Protection & Controls Engineering Co-op at **Duke Energy**
Brett.Ross@duke-energy.com

Request for SEL-487E Images (Fig. 3.15):

Usage Request for Student Project - SEL487E Images

Brett Ross
Today, 1:44 PM

Good afternoon Janna,

I am forwarding this to you because Ryan is out of office until the 20th.

Thanks so much for your help,

Brett Ross
813.431.6220
Candidate for *B.S. of Electrical Engineering* at **UCF** (SU '19)
brettross96@knights.ucf.edu
Protection & Controls Engineering Co-op at **Duke Energy**
Brett.Ross@duke-energy.com

Brett Ross
Today, 1:43 PM
ryan_trostrud@selinc.com

Reply all

You forwarded this message on 2/9/2019 1:44 PM

Good afternoon Ryan,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for transformer protection for our Senior Design project. Our project is for educational purposes, but we do an analysis of current market offerings as a part of our documentation.

We would like to use images of the SEL-487E in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I wasn't sure who the point of contact is for permissions, but I was hoping you might be able to assist me in obtaining permission for reproduction.

Thanks in advance for your help,

Brett Ross
813.431.6220
Candidate for *B.S. of Electrical Engineering* at **UCF** (SU '19)

J janna_enfinger@selinc.com
Today, 3:04 PM
Brett Ross

Reply all

Flag for follow up.

4 attachments (3 MB) Download all Save all to OneDrive - Knights - University of Central Florida

Hey Brett,

I did get the ok for you to use the images requested. I even got some better, hi res photos for you. Please see attachments. Let me know if you have any questions.

SEL
SCHWEITZER ENGINEERING LABORATORIES, INC.
Janna Enfinger
Customer Service Rep/Southeast Region
Janna_Enfinger@selinc.com
509-334-8197

From: Brett Ross <BrettRoss96@Knights.ucf.edu>
To: "janna_enfinger@selinc.com" <janna_enfinger@selinc.com>
Date: 02/11/2019 06:30 PM
Subject: Re: Fw: Usage Request for Student Project - SEL487E Images

Request for SIPROTEC 5 Images (Fig. 3.16)

Usage Request for Student Project - SIPROTEC 5 Images

BR

Brett Ross
Today, 10:18 AM
support.energy@siemens.com

Reply all

Good morning,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for transformer protection for our Senior Design project. Our project is for educational purposes, but we do an analysis of current market offerings as a part of our documentation.

We would like to use images of the SIPROTEC 5 series relays in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I wasn't sure who the point of contact is for permissions, but I was hoping you might be able to assist me in obtaining permission for reproduction.

Also, I tried to use the configuration tool to obtain some pricing data but I was unable to. I'm not sure if it's easy to get pricing information without a formal quote process, but I was hoping to know A) The starting price for the 7UT87 and B) A pricing for the 7UT87 with nearly its full functionality (Two expansion modules, networking expansions, enough function points for advanced schemes, etc.). These will help us establish context for our project so reviewers will understand one reason why we cannot build something nearly as robust and powerful as the 7UT87.

Thanks in advance for your help,

Brett Ross
813.431.6220
Candidate for *B.S. of Electrical Engineering* at **UCF** (SU '19)
brettross96@knights.ucf.edu
Protection & Controls Engineering Co-op at **Duke Energy**
Brett.Ross@duke-energy.com

P

presspictures.cc@siemens.com
Today, 4:44 AM
Brett Ross

Reply all

Dear Brett, thank you for resending.

you may use the visuals for your educational project.
Do you need the data in higher resolution or are the file you can access sufficient for you?
Just let me know if I can be of any help to you.

Kind regards, Judith

Judith Egelhof
Siemens Photography and Multimedia department
mailto:presspictures.cc@siemens.com

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To help us answer your questions quickly and to your satisfaction, always include all correspondence in your e-mails.

Request for TVS Figure (Fig. 3.17)

Copyrighted Image Usage for Educational Purposes

Brett Ross
Today, 10:29 PM
copyrightcounsel@list.ti.com

Reply all

Good evening,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.

We are hoping to obtain permission for the following images:
Figure 4 on Page 3 of: http://www.ti.com/lit/an/slyt492/slyt492.pdf

Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,

Brett Ross
813.431.6220
Candidate for *B.S. of Electrical Engineering* at **UCF** (SU '19)
brettross96@knights.ucf.edu
Protection & Controls Engineering Co-op at **Duke Energy**
Brett.Ross@duke-energy.com

Approval:

Bassuk, Larry <l-bassuk@ti.com>
Yesterday, 12:38 PM
Brett Ross

Reply all

Flag for follow up.

Dear Brett Ross,

Thank you for your interest in Texas Instruments. We grant the permission you request in your email below.

On each copy, please provide the following credit:

Courtesy Texas Instruments
Regards,

Larry Bassuk
Senior Patent Counsel &
Copyright Counsel
Texas Instruments Incorporated
214-479-1152

Request for Hall Effect Current Image (Fig. 3.18):

To R RodNave@gsu.edu ×

Bcc

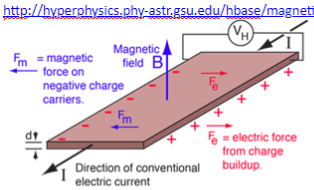
Cc

Copyright Permission

Good Evening,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.

We are hoping to obtain permission for the following images:
http://hyperphysics.phy-astr.gsu.edu/hbase/magnetic/Hall.html



Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,

-Daniel Hobbs.

Copyright Permission

RN Rod Nave <rodnave@gsu.edu>
Yesterday, 8:28 AM
Daniel Hobbs; rodnave <rodnave@mail.phy-astr.gsu.edu>

Reply all

Hello, Daniel,

You are welcome to use images from HyperPhysics for the project as you describe. Since part of the plan is to place it on the University website, I would ask that the copyright be acknowledged with something like " from HyperPhysics, copyright Rod Nave, Georgia State Univ".

Best wishes with the project.

Regards,
Rod Nave RodNave@gsu.edu
HyperPhysics Project
Department of Physics and Astronomy
Georgia State University
Atlanta, GA 30302-5060

Permission for CT Images (Fig. 3.19, 3.20):

[External]Requesting Permission for usage of pictures and information for educational purposes.

WS Wayne Storr <wstorr@aspencore.com>
Thu 2/28, 11:09 AM
Daniel Hobbs

Hello Daniel,

The same conditions apply for all tutorials and/or images as per our answer to your first request.

Regards
Electronics Tutorials

Permission for CT Images (Fig 3.22, 3.24):

Image Request proofs needed

DH

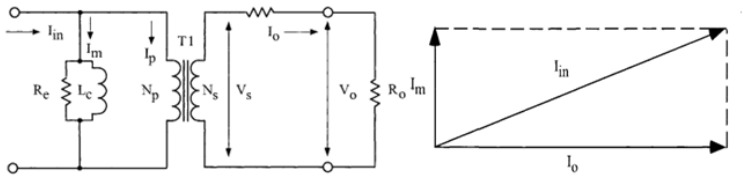
Daniel Hobbs <DanielHobbs@Knights.ucf.edu>

Sun 3/24, 4:45 PM

Brett Ross

Reply all

heres the response for those images, i guess he just wants to reference his website. its from chapter 16 of the pdf's he has listed.



Dear Daniel,
What you have been looking at is a textbook posted for my students in Power Electronics class. If you'd like to cite it, please use the reference posted on https://coefs.uncc.edu/mnoras/courses/power-electronics/tr_design/

Sincerely,
Maciej Noras

Request for Voltage Divider Images (Fig 3.23):

To S sales@digikey.com

Bcc

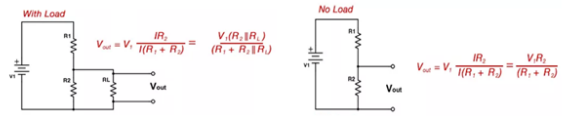
Cc

copy right permission

Good Evening,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.

We are hoping to obtain permission for the following images:



https://www.digikey.com/en/resources/conversion-calculators/conversion-calculator-voltage-divider

Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,

Daniel Hobbs.

Request for CT Excitation Curve Images (Fig 3.21):

To eb@ijpam.eu

Bcc

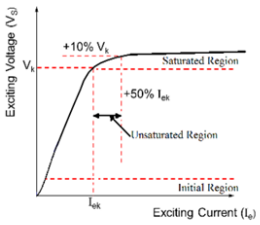
Cc

Copy right

Good Evening,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.

We are hoping to obtain permission for the following images:



Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,

Daniel Hobbs.

Send Discard

Draft saved at 11:57 PM

Request for Filter images (Fig 3.25, 3.27, 3.28):

Good evening,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.

We are hoping to obtain permission for the following images:

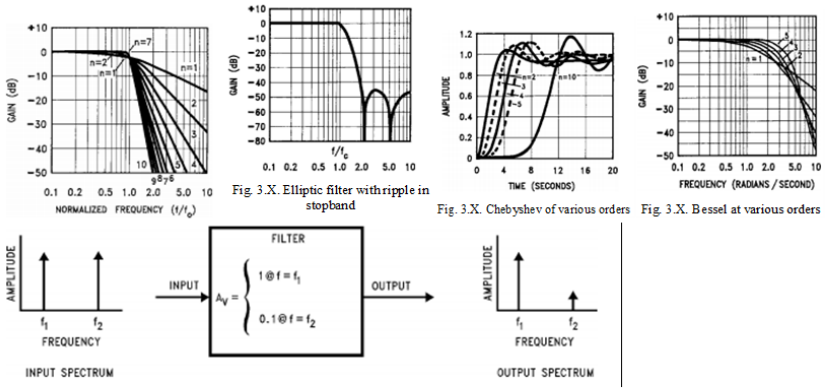


Fig. 3.X. Elliptic filter with ripple in stopband

Fig. 3.X. Chebyshev of various orders

Fig. 3.X. Bessel at various orders

These are coming from the basic introduction to filters, literature number: SNOA224A.

Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,

Daniel Hobbs.

Request for Filter Image in Table (Table 3.6):

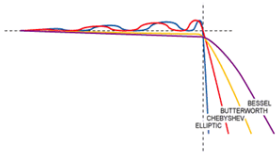
QUESTION OR ISSUE *

Source | Styles | Normal | Font | Size

Good evening

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would li to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist n in obtaining permission for reproduction.

We are hoping to obtain permission for the following images:



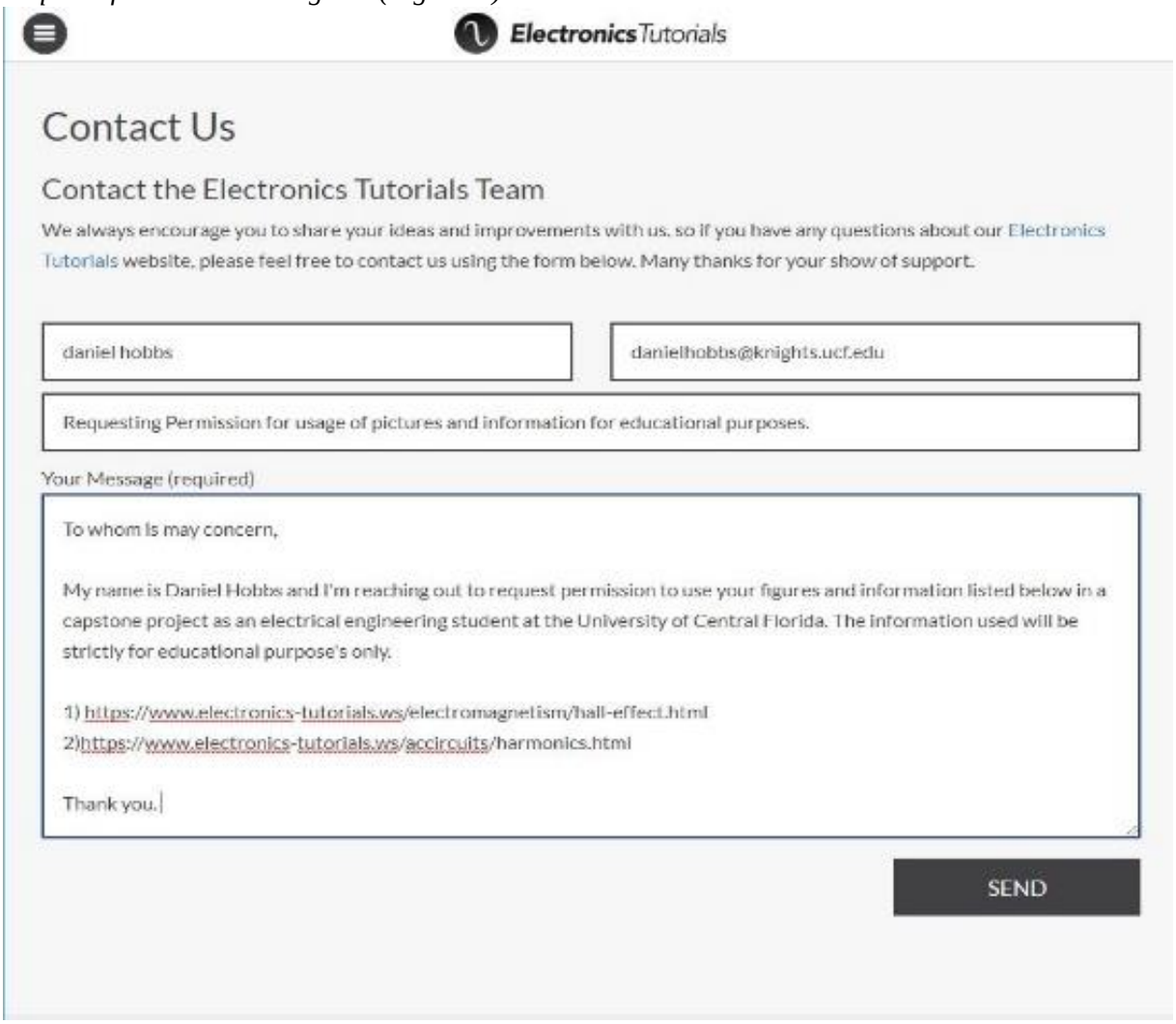
Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,

Daniel Hobbs

body p

Requests for Harmonics Figures (Fig. 3.26)



Electronics Tutorials

Contact Us

Contact the Electronics Tutorials Team

We always encourage you to share your ideas and improvements with us, so if you have any questions about our Electronics Tutorials website, please feel free to contact us using the form below. Many thanks for your show of support.

daniel hobbs

danielhobbs@knights.ucf.edu

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Your Message (required)

To whom is may concern,

My name is Daniel Hobbs and I'm reaching out to request permission to use your figures and information listed below in a capstone project as an electrical engineering student at the University of Central Florida. The information used will be strictly for educational purpose's only.

1) https://www.electronics-tutorials.ws/electromagnetism/hall-effect.html
2)https://www.electronics-tutorials.ws/accircuits/harmonics.html

Thank you.

SEND

[External]Requesting Permission for usage of pictures and information for educational purposes.

WS Wayne Storr <wstorr@aspencore.com>
Wed 2/13, 3:28 AM
Daniel Hobbs

Reply all

Hello Daniel,

Thank you for your email and question, and apologies for the delay in responding.

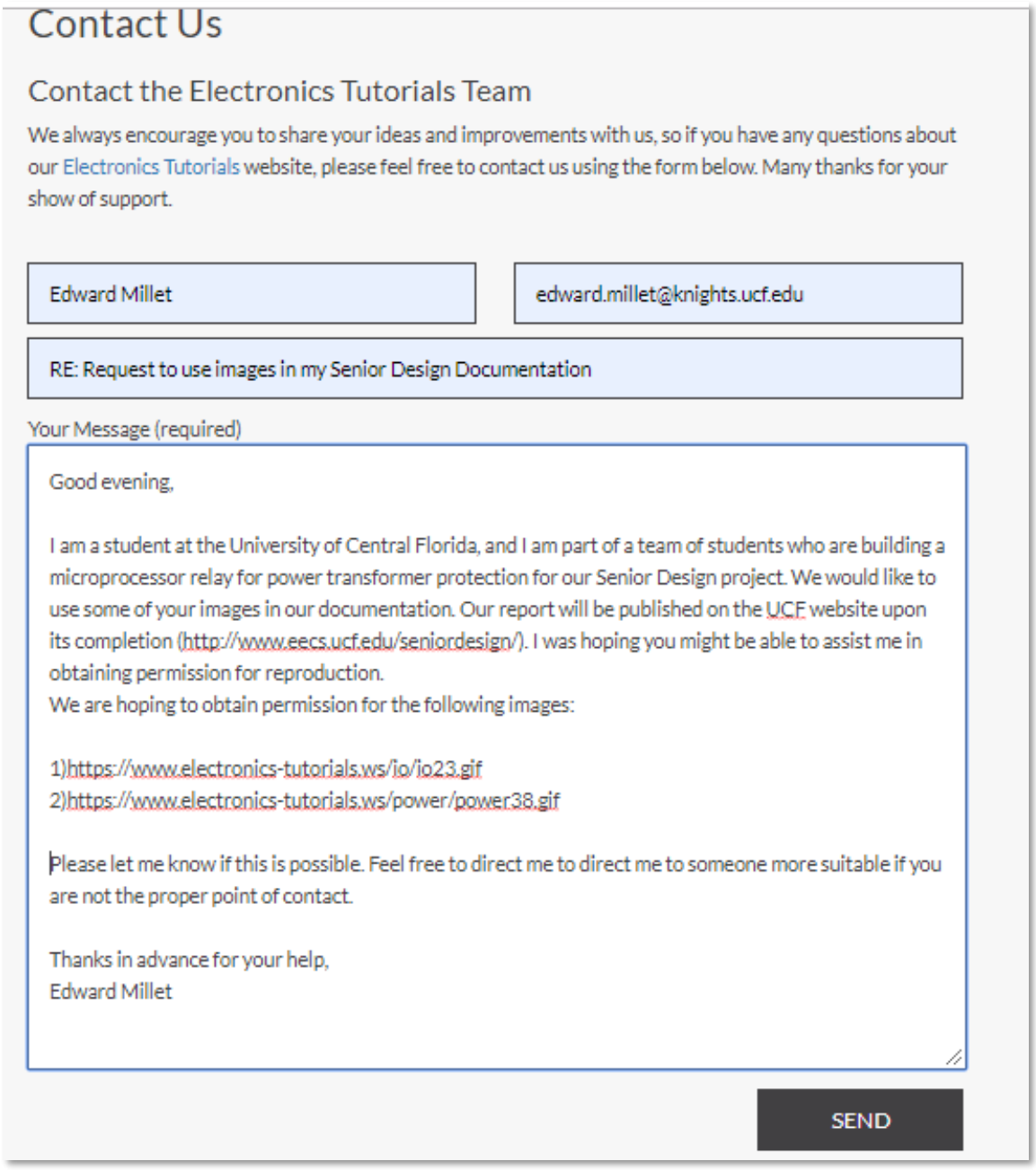
As you have kindly asked we would have no objection to you using the information and/or images from the requested tutorial, free of charge.

However, we must ask that you correctly reference the website: www.electronics-tutorials.ws and any images and/or tutorial content you use accordingly within your presentations.

Good luck with your project.

Regards
Electronics Tutorials

Request for Electromechanical and Solid State Relay Images (Fig. 3.29, 3.30):



Contact Us

Contact the Electronics Tutorials Team

We always encourage you to share your ideas and improvements with us, so if you have any questions about our Electronics Tutorials website, please feel free to contact us using the form below. Many thanks for your show of support.

Edward Millet

edward.millet@knights.ucf.edu

RE: Request to use images in my Senior Design Documentation

Your Message (required)

Good evening,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.
We are hoping to obtain permission for the following images:

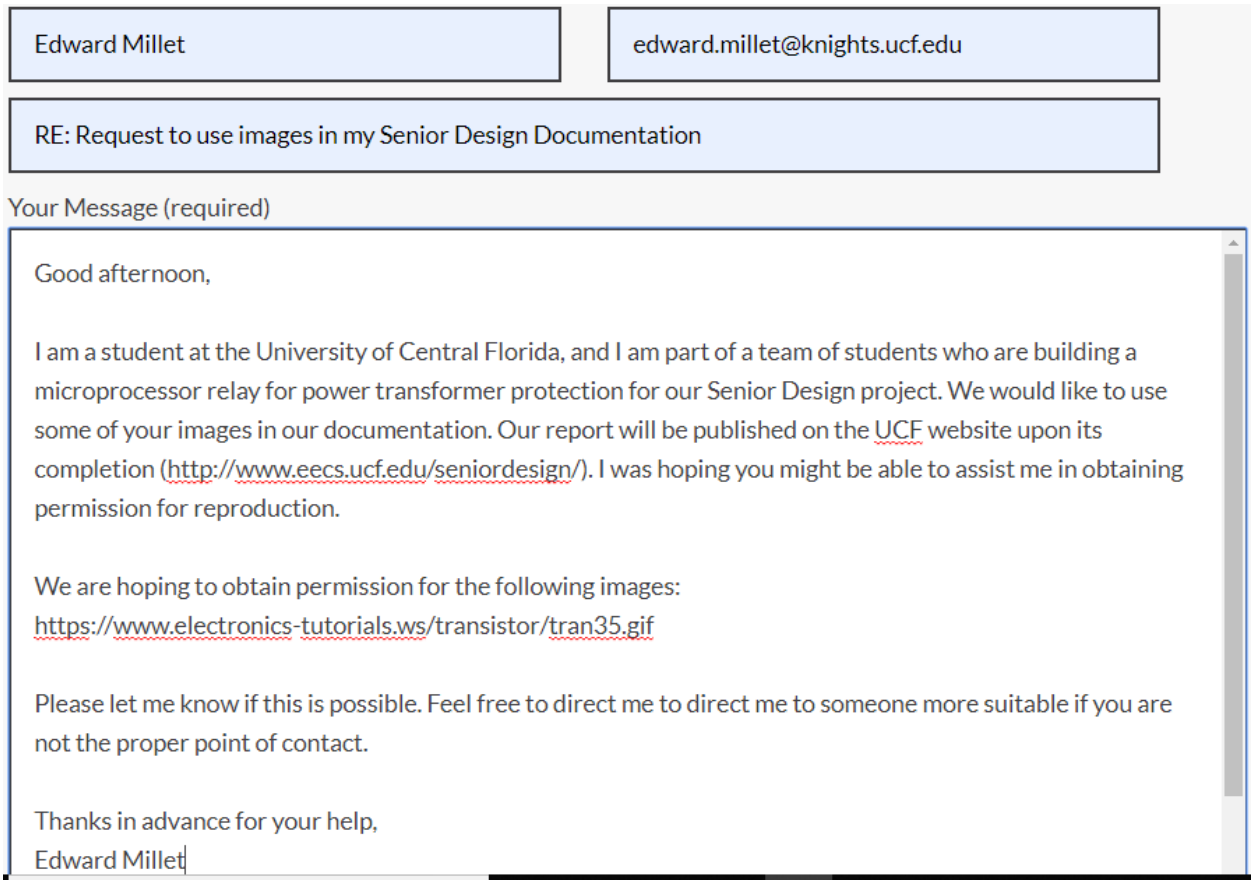
1)https://www.electronics-tutorials.ws/io/io23.gif
2)https://www.electronics-tutorials.ws/power/power38.gif

Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,
Edward Millet

SEND

Request for MOSFET Image (Fig 3.32):



Edward Millet

edward.millet@knights.ucf.edu

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Good afternoon,

I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.

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Thanks in advance for your help,
Edward Millet

Permissions for I2C and SPI Images (Fig 3.33, 3.34):

mail@electrosome.com

Request to use pictures

Good Evening,
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https://electrosome.com/wp-content/uploads/2017/04/SPI-Master-and-Multi-Slave-Connections.png

Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

Thanks in advance for your help,

--
Johnathon DeFour

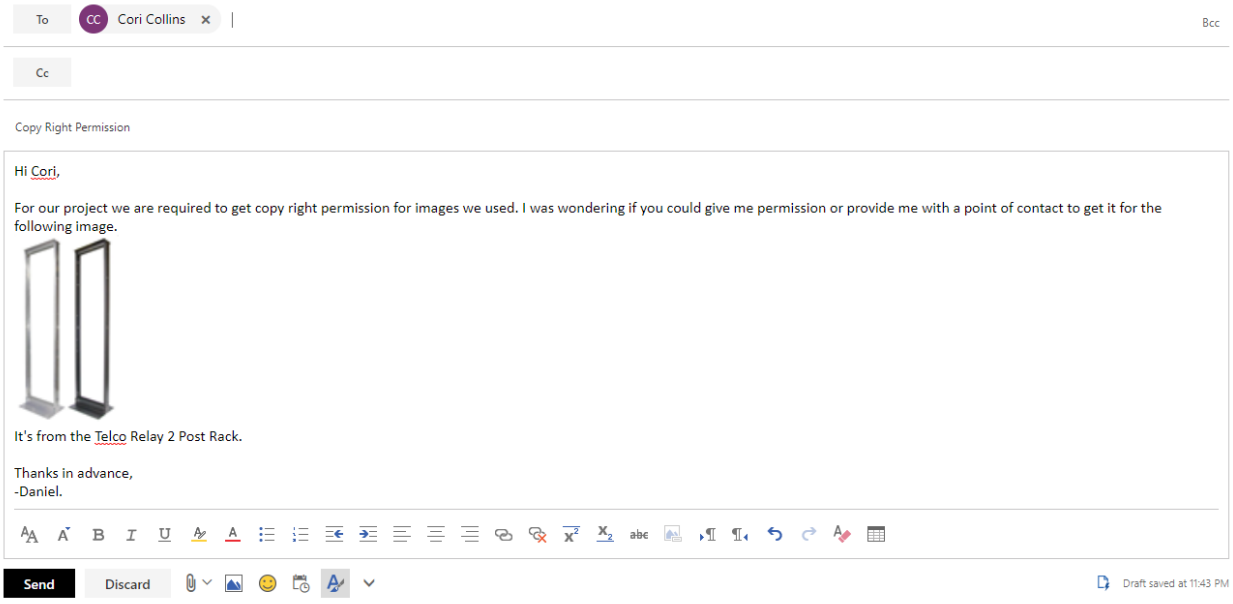
Re: Request to use pictures 2

Johnathon DeFour Good Evening, I am a student at the University of Central Florida, and I am part of a team

electroSome Mail <mail@electrosome.com>
To: Johnathon DeFour

Please feel free to use it.

Permission Request for Relay Rack (Fig 3.44)



Permission Request for ALP Relay Images (Fig. 3.45, 3.46):

To I information@gentec.ca ×

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Cc

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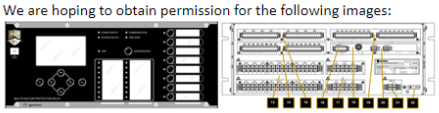
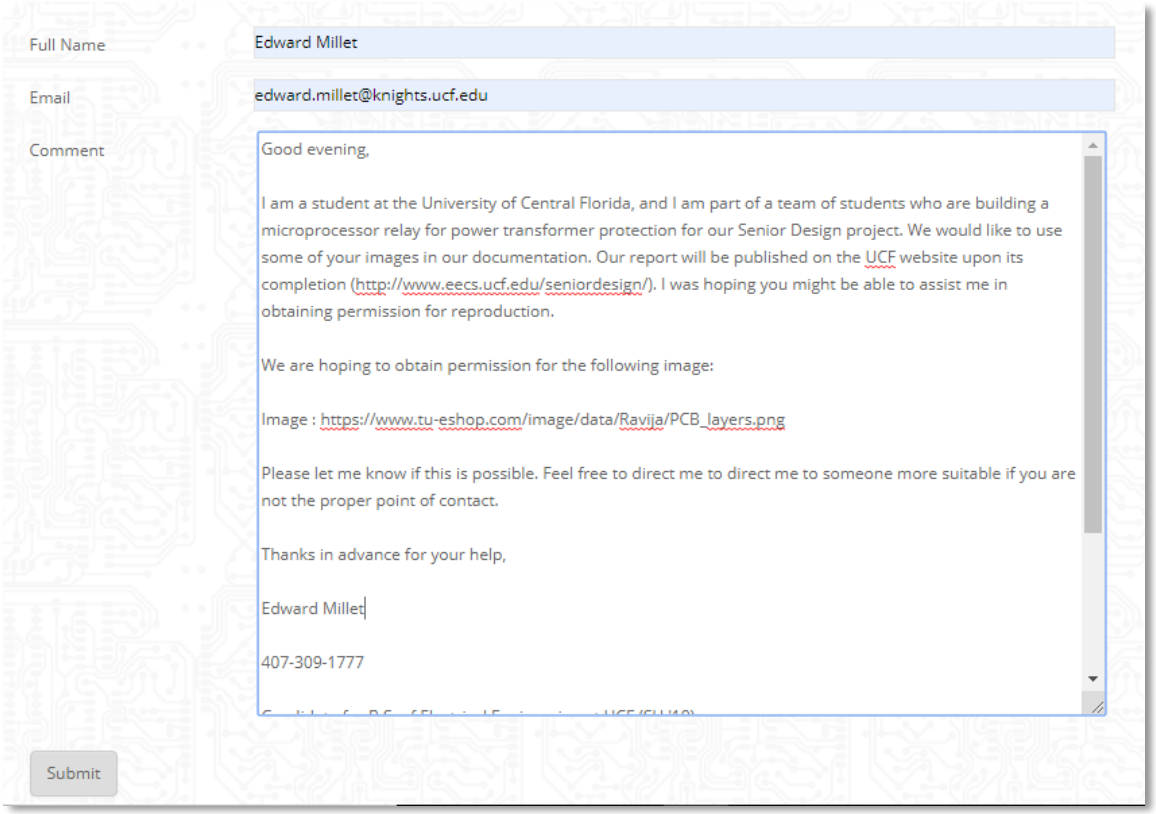


Please let me know if this is possible. Feel free to direct me to direct me to someone more suitable if you are not the proper point of contact.

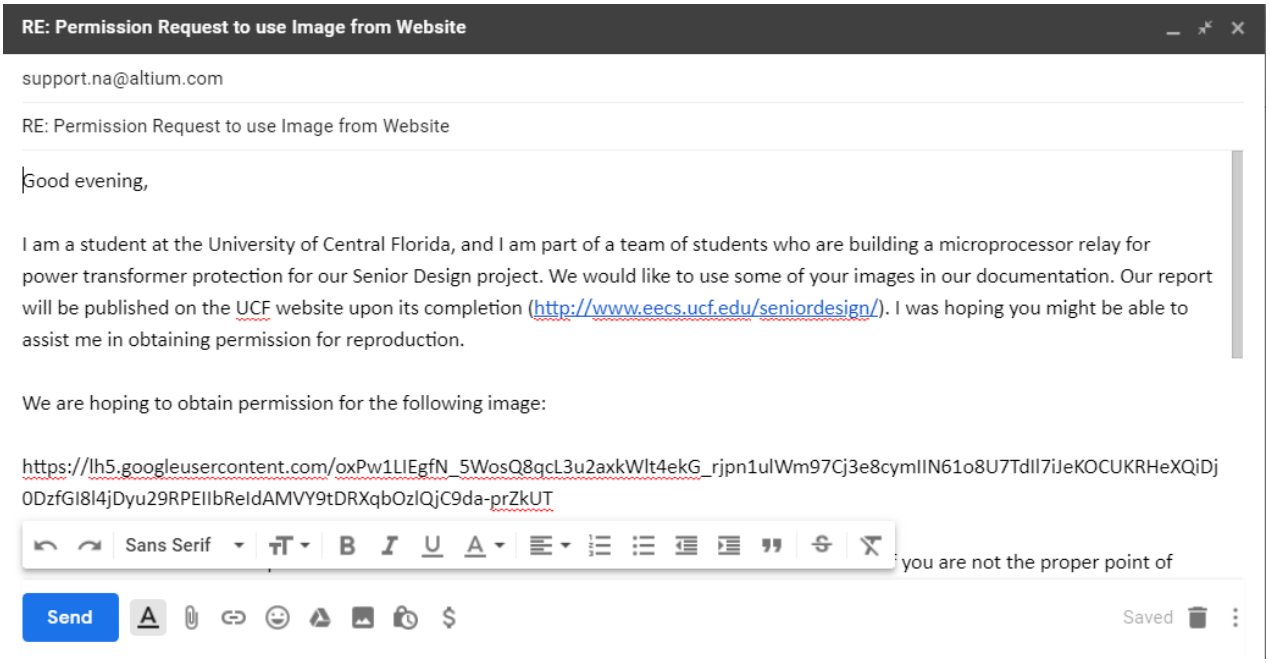
Thanks in advance for your help,

Daniel Hobbs.

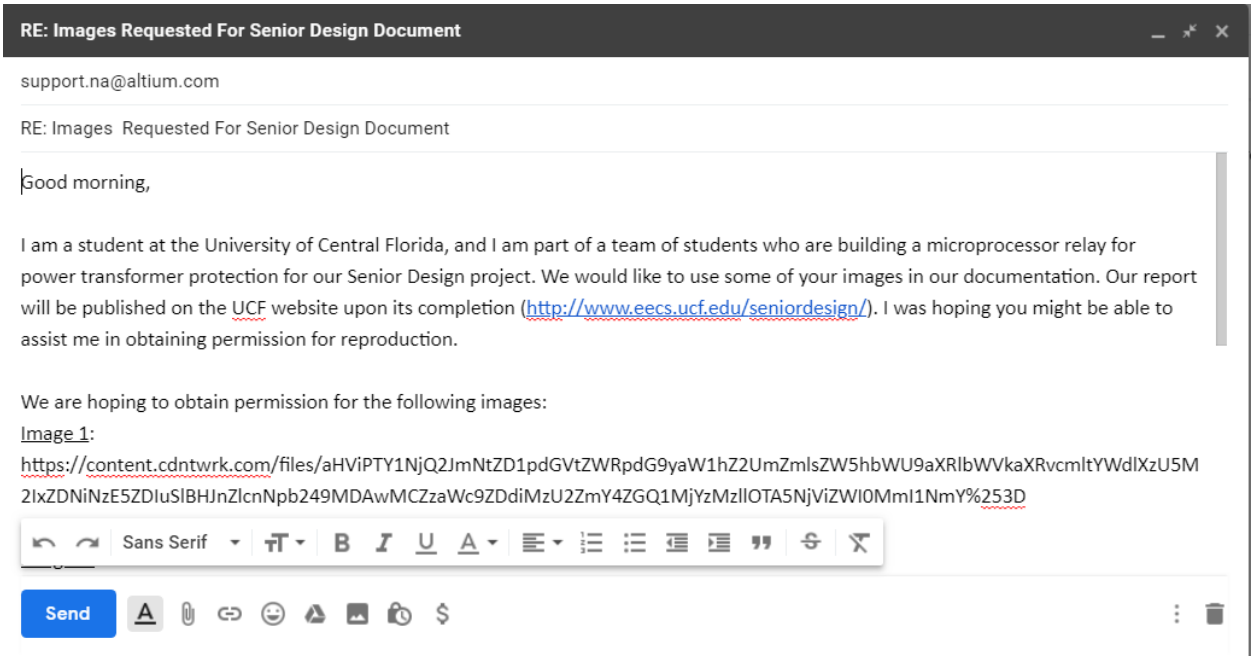
Permissions for PCB Layers Image (Fig. 8.1):



Permissions for PCB Analog/Digital Layout Image (Fig. 8.4):



Permissions for Preferred Trace-Routing Image (Fig. 8.2, 8.3):



RE: Images Requested For Senior Design Document

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RE: Images Requested For Senior Design Document

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I am a student at the University of Central Florida, and I am part of a team of students who are building a microprocessor relay for power transformer protection for our Senior Design project. We would like to use some of your images in our documentation. Our report will be published on the UCF website upon its completion (http://www.eecs.ucf.edu/seniordesign/). I was hoping you might be able to assist me in obtaining permission for reproduction.

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Sans Serif

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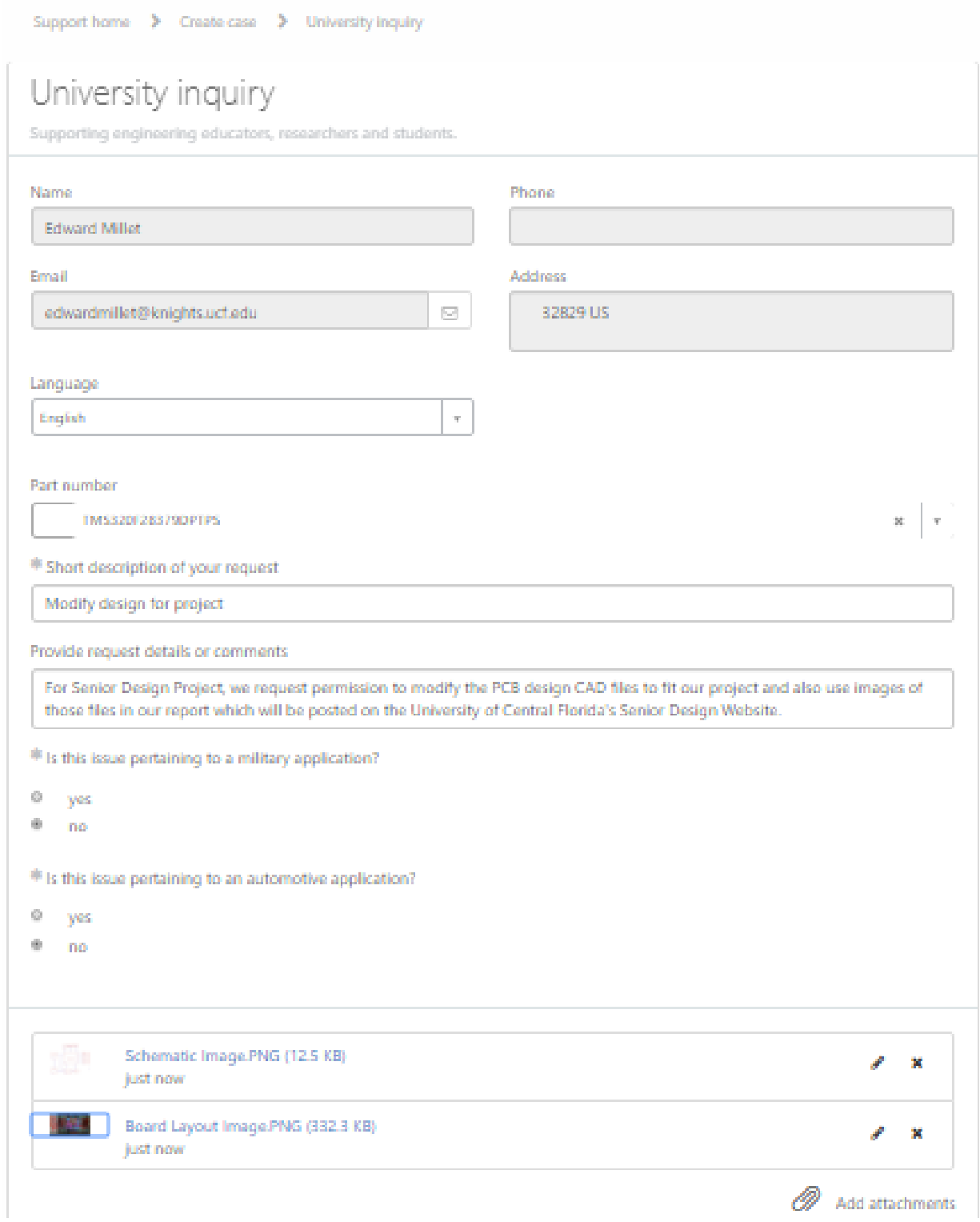
Permissions for Texas Instruments Block Diagram & Board (Fig. 6.9, 8.8)



Support home > Create case > University inquiry

University inquiry

Supporting engineering educators, researchers and students.

Name: Edward Millet

Phone:

Email: edwardmillet@knights.ucf.edu

Address: 32829 US

Language: English

Part number: TMS320F283/9DPTPS

* Short description of your request: Modify design for project

Provide request details or comments: For Senior Design Project, we request permission to modify the PCB design CAD files to fit our project and also use images of those files in our report which will be posted on the University of Central Florida's Senior Design Website.

* Is this issue pertaining to a military application?

- yes
- no

* Is this issue pertaining to an automotive application?

- yes
- no

Schematic Image.PNG (12.5 KB) just now

Board Layout Image.PNG (332.3 KB) just now

Add attachments

APPENDIX B – REFERENCES

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