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Group 1

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1 - Introduction

1.1 Executive Summary

Lockheed Martin is one of the primary defense contractors for the United States military and to the National Aeronautics and Space Administration, and contractor to many other militaries around the world. Lockheed Martin Missiles and Fire Control in Orlando, Florida is sponsoring the project. The plant concentrates on radar development and weapon defense. Currently, one of the main programs at this facility is Joint Air to Ground Missile, or JAGM. The missile will serve as the next generation missile to the U.S. Army, U.S. Navy, and U.S. Marine Corps. It will replace the HELLFIRE missile and Longbow HELLFIRE missile now used on the Apache attack helicopter, and also missiles on the F/A18 Hornet, the Apraho reconnaissance helicopter, the Super Cobra attack helicopter, the Seahawk reconnaissance helicopter, and the Warrior unmanned aerial vehicle. It may also be used on the F-35 Lightning II platform. The JAGM missile has a tri-mode seeker, which will enable it to have far reaching limitations. The seeker is equipped with a semi-active laser, infrared imaging, and millimeter wave radar making it versatile and an all-weather capable missile.

JAGM needs a next generation power supply for the transceiver of this missile. The circuit board must convert the power source voltage and convert it to multiple voltages for the transceiver. The circuit board must also have a timing control unit that will do power up sequence and power down sequence, as well as monitoring the temperature. Timing signals are expected to be highly accurate and reliable. One of the main challenges of this particular project is the limited circuit board space and limited airflow in the system. This is a particular challenge because there must be low heat dissipation from the board. Low heat parts and proper package will have to be considered. Electromagnetic interference (EMI) must be kept to a minimum to insure optimal performance of missile guidance and tracking systems. The power supply needs to be clean, contiguous, and responsive.

The following diagram, Figure 1, is a basic block diagram of the power supply system. In more detail of the system, 32 volts is the only voltage source to the power supply system. The 32 volts must be used to power everything in the circuit and will also be converted into high power and low power voltages. The voltages that will be created from 32 volts is +6V high power, -4 volts, +6 volts low power, and 9 volts. These voltages that need to be generated will be used for a separate circuit board. However, this circuit board will not be considered in this design. The control unit will monitor the output voltages and output currents of specific voltage converters, it will control when the voltage converters are turned on and off, and it will monitor the temperature from a specified temperature sensor in the system.

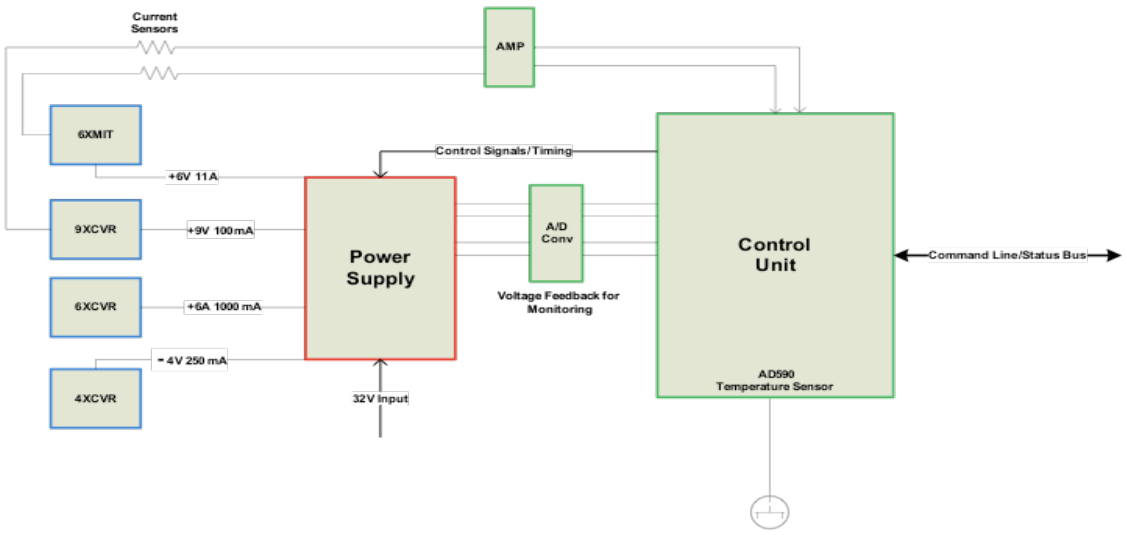

Figure 1.1.1 Block Diagram of system

1.2 Motivation

As engineers, we strive to improve people's lives. The team members of this project want to accomplish this very aspect. The motivation of the project is to design a more useful power supply for the transceiver. A fully functioning transceiver with reliability contributes to a more reliable seeker. The missile itself becomes more reliable because of the seeker. This is like dominoes falling in line. One thing affects the other. Pilots need the reassurance that they are carrying missiles that will save their lives in combat and help them succeed in their mission.

1.3 Objectives & Goals

The JAGM (Joint Air to Ground Missile) is to be a replacement to the Hellfire II, Longbow HellFire missile, and Maverick missiles in current use on many platforms throughout the United States Armed Forces and our Allies. Current platforms include the US Army Apache Helicopter, US Marine Corps Super Cobra, and the US Navy's Seahawk armed reconnaissance helicopter. JAGM could also replace the Maverick missile aboard the US Navy's FA-18 Hornet.

The goal of our project is to create a circuit card that provides sufficient voltage and current required to drive the transceiver subsystem assembly of the missile and provide the appropriate timing and control architecture to implement a power sequence and monitor these voltages. The timing and control architecture's primary responsibility will be to monitor and power sequence the voltages to their subsequent subsystems. Parameters to the problems we will face include extreme temperatures, EMI, thermal constraints and very precise DC voltages with low ripple.

With this multi-platform and multi-environment situation we were tasked to provide a circuit card that could work in harsh environments. This would require us to procure parts that could handle extreme temperature and stress. These parts are generally considered military grade electronics. The fact that the missile the circuit card is going in will possibly be flying at high altitudes where temperatures could exceed -40 degree Celsius and were factors we needed to keep in mind during selection of parts.

The heart of the timing and control architecture subsection will be controlled using some sort of a programmable logic device, such as a CPLD (Complex Programmable Logic Device), Micro-Controller, or Field Programmable Gate Array (FPGA). This device will accept control signals from an external FPGA and provide the appropriate action required. Over this command bus the timing and control architecture will provide status updates on the voltages and current we are monitoring, temperature in the transceiver monitored by the AD590 temperature sensor, and provide power sequencing status updates. This two way communication will require the design of a serial or parallel communication bus with an external clock source that will be provided.

The printed circuit board design will be a challenge in itself. The entire power architecture and timing control unit must all fit onto a single board that has an area of 6 square inches. This specification requires us to select the smallest and most energy efficient parts that we can find. Due to the lack of space these constraints will elevate thermal and EMI problems. Therefore, the group will have the challenge in designing a PCB and selecting parts to alleviate such problems.

1.5 Specification Overview

Lockheed Martin is designing a new radar interface. The RF Engineers of XYZ Corporation have completed their design of the RF components in a new radar transceiver. The rest of the design has been assigned to us. The power supply architecture for the radar transceiver has to be designed in a printed circuit board with an area no greater than 6 inches. The power supply along with its timing and control architecture will receive an input voltage of +32 V. The input voltage has to be processed into different output voltages as required by the radar transceiver. The 6XMIT is used to drive the transceiver. It has to supply a load for durations of 1 to 100 μS and shall not exceed 50% duty cycle. The other voltages supply power to continuous loads. In addition, the output voltages have to follow a power sequence. The 4XCVR must be powered first, then +6, then +9, and laslty the +6 VDC. Upon a system failure or shutting down the system the power down sequence is reversed by turning off the 6XMIT first and then following the same order in a reversed manner. Figure 1.5.1 summarizes the power sequence.

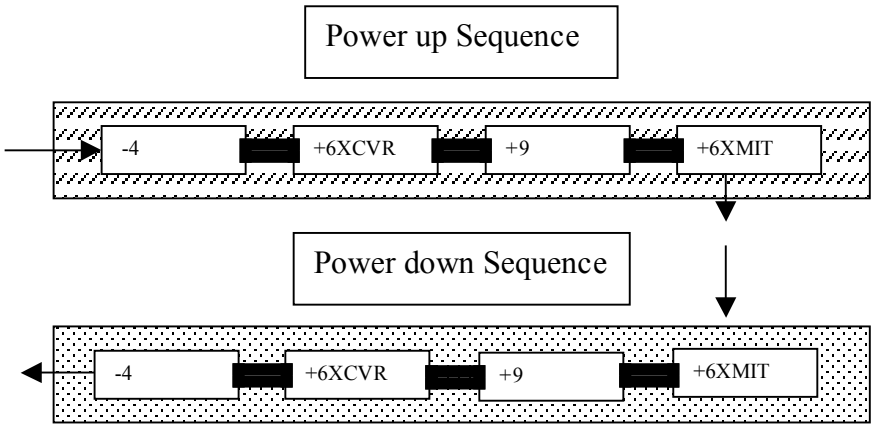

Figure 1.5.1 Power Sequence Summary

2 - System Design Considerations

2.1 32 V Input

32 volts (32Vin) will be provided to power the system. The 32Vin will only have a voltage ripple of 100uV. The 32Vin is used to generate voltages that the specifications mention. 3.3 volts (3.3Vin) will also be provided to supply operating power to the FPGA. This voltage will not need to be filtered.

2.2 Voltage Generation Requirements

Four voltages must be generated in a specific sequence. There is one high power signal to be generated. Then three low power signals that must be generated. The high power signal has more tolerance for ripple voltage than the low power signals. The four output voltages that the radar transceiver needs are as follows in Table 2.2.1. The table includes the necessary output current, regulation, and ripple voltage.

Signal	Output Voltage	Output Current	Regulation	Ripple Voltage
6XMIT	6VDC	11 A	3%	1mV
9XCVR	+9VDC	100mA	3%	100uV
6XCVR	+6VDC	1000mA	3%	100uV
4XCVR	-4VDC	250mA	3%	100uV

Table 2.2.1 Voltage Generation Requirements

2.3 Noise Requirements

Noise is the unwanted part of an electrical signal. It is created by electrical interferences by other devices in a circuit or by electrical interferences external to the system coming from the environment. It is a nuisance because it interferes with accuracy. Voltage ripple is a result of noise. Some systems may need to be more accurate than others and voltage ripple is a major factor to consider a particular device and whether it is appropriate for that particular circuit design. The input power will have 100uV ripple voltage. The low power output signals must have only 100uV ripple voltage. However, the high power output power can be 10mV ripple voltage. The power supply must output clean voltages to the transceiver.

2.4 Thermal Requirements

The radar transceiver is mounted on gimbal with only convection cooling of approximately 3 watts and heat sink available to control temperature. The heat sink is aluminum with 5 inch diameter and 0.35 inch thickness. Due to the lack of cooling means, the heat generated in the conversion of +32 V to other voltages must be minimized to maximize the operation time of the radar transceiver. The goal is to operate the radar transceiver in 7 minutes intervals between power downs for cool off. In order to meet these requirements, DC to DC convertors have to be implemented to obtain efficiencies above 90 %. Operating temperature range called by the customer is -55 degrees Celsius to +85 degrees Celsius.

2.5 EMI Requirements

The EMI requirement is to use the devices with the lowest EMI rating. EMI is the generation of unwanted frequencies from nearby devices or equipment. EMI can come from the switching of any device. Digital devices can be extremely noisy because of the internal switching. EMI is especially critical in the design of the power supply because it cannot affect the transceiver. The transceiver's efficiency can be affected by the frequencies generated from the power supply. Even the harmonics from the generated frequencies can affect the operation of the transceiver.

2.6 PCB Layout Constraints

One of the limiting factors of the topology is the area is only 6 square inches. The height of the parts mounted on the board has negligible clearance. Any part should fit in the space allotted for the board in the seeker. The circuit board may be any shape. Parts may be mounted on both sides of the board or just one side of the board. The only constraint is that the parts chosen for the design only take 6 square inches of real-state on the board. There are no constraints on how or where the board must be manufactured. There is unlimited amount of layers allowed in the PCB design.

2.7 RoHS Compliance

It is preferable to acquire parts that are non-RoHS compliant. If it is necessary to purchase RoHS compliant parts because of availability, then the pins must be coated with lead. Also, it is imperative that the part not be made mostly with tin. Parts used in the design must be rugged, and if the part is RoHS compliant it will degrade more quickly.

3 - Research

3.1 Introduction

Proper research for this project is vital to achieve the task of completing a functioning design. The project will require the team members involved to learn about new topics that have not been taught in the undergraduate program. Most of the material that the members of the group will deal with in this project is considered 'graduate level' material. In order to gain a better understanding of the overall picture, Scott Faulkner, the sponsor of the project will meet with the group every two weeks in order to keep the group in the right track. The project will be split into three parts; each member will get a section of the project. Extensive research on the assigned topic will be done by the members of the group and at the end of the first semester a design will be proposed based on the research done by the group. It is believed that the main challenge of this project will be populating all the components in a 6 square inches printed circuit board without overheating the components and keeping the electromagnetic interference levels extremely low so that other components in the circuit are not affected by it.

3.2 Research Methods

At first the group consisted of four EE students. Upon reading the guidelines of the project given to the group by Lockheed Martin, it was decided that the initial research would be equally divided among the group members since all members have gone through the same pre-engineering classes. During the second week, specific topics were chosen by each group member based on interest of the topic. The power supply architecture and hardware design was split between Catherine Donoso and Diego Rocha. The timing and control architecture was split between Josef Von Niederhausern and Keith Weston. For the first two months, each member searched for numerous resources that could be used to meet the design goals given to the group. The group focused mainly on the data-sheets of well known companies such as Linear Technology, Texas Instruments, and Xilinx. During that period, the group met twice a week to discuss the progress of the team as a whole and to set goals such as having a certain amount of information for the next meeting. In addition, the group met

with the sponsor of the project, Scott Faulkner every two weeks to discuss questions. A month before the first phase of the project had to be finished; Josef Von Niederhausern dropped the class because of personal conflicts. His part of the project was divided equally among the rest of the members of the group. As of right now, the group is finishing the design; the prototype will be built next semester.

3.3 Simulation

Simulation is a powerful tool for analyzing, designing, and operating complex systems. It enables the designer to test the prototype and debug it before actually building it. Additionally, a proper modeling of the system will prove to some extent that the prototype design will function properly and will give the designer a better insight of how the components operate within the system. In general, the advantages of simulating circuits are the following:

- Predict results and verify equations provided by manufacturer.
- Understand why observed events occur.
- Identify and solve problems before building prototype.
- Explore new ideas and verify its impact on the circuit.
- Communicate the integrity of the prototype.

Several fancy programs for circuit simulations are available in the industry. However; most of them are very expensive and therefore it is almost impossible for students to get a hold of them. Ironically, major manufacturers have started developing spice programs that simulate their products and even go a step further as to build the circuit that the designer needs to implement as is the case with Texas Instruments. So in order to simplify the design process, all the components for the power supply were chosen from one manufacturer and that is Linear Technology. Upon weeks of doing research, it was found that Linear Technology provided the components needed to complete the design. Consequently, Linear Technology provides a spice program for simulation purpose called LTspice. As a result, all the simulations in this document were done in LTspice.

LTspice is another spice program in the market that is provided for free by Linear Technology. The program allows measurements of currents and voltages that are “virtually impossible to do any other way” according to the designer at Linear technology. The success of these analog circuit simulators has made circuit simulation spread to board level circuit design. It is easier in many cases to simulate rather than breadboard, and the ability to analyze the circuit in the simulation for performance and problems speeds the design of well understood robust circuits.

There are currently approximately fifteen hundred Linear Technology products according to the Linear Technology website. The program includes

demonstration files that allow the designer to watch step-load response, start-up and transient behavior on a cycle by cycle basis. Included with the spice is a full featured schematic entry program for entering new circuits. Further, spectrum analysis can also be done in the software. This facilitates meeting the noise requirements given to the designer.

3.4 Electro-Magnetic Interference Solutions

Electro-Magnetic Interference or EMI emissions come out of equipment or components and affect the performance of the circuitry. The two types of EMI are radiated and conductive EMI. Radiated EMI occurs when two components that are separated by space with no hard wire connection somehow end up being connected through a path provided by radiated noise. On the other hand, conductive EMI results when two components that are not supposed to be connected end up with a connection through wire paths within the circuit. Incidentally, both types of noise can exist at the same time. The figure below illustrates both radiated and conductive noise.

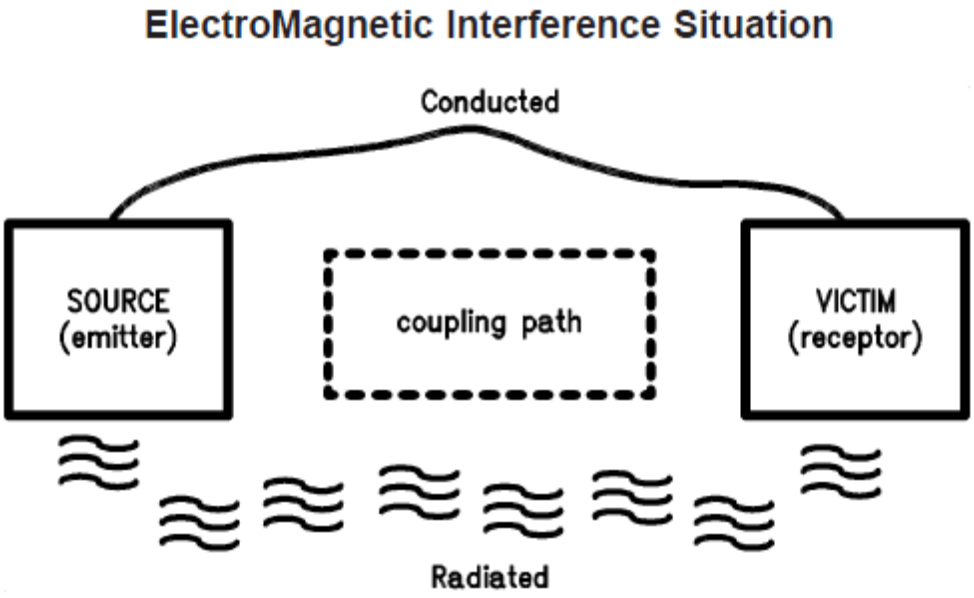

Figure 3.4.1 Shows unwanted coupling paths through radiated and conducted EMI

As mentioned before, one the disadvantages of using dc/dc in power supplies is that they introduce noise in the system. When any element switches logic from two reference voltages, it generates current spikes that produce a voltage transient**.** This introduces conducted noise in the system which can be eliminated using filters. Radiated noise in a dc/dc buck topology comes out of the magnetic field in the inductor. One way to suppress the radiated noise is by shielding the source of noise, and grounding the element that is acting as a shield. All these different solutions add more size to the area in which all the

components will be mounted, and since the area given in the specs is limited only to six inches squared, minimizing the size of the components is critical.

LTI4612 belongs to the µModule family of the Linear Technology dc/dc modules. One of the main features of the LTI4612 is that it is an “ultra-low-noise” module. The designers at Linear Technology have taken all the required measurements to minimize the radiated and conducted EMI caused by the device. Low pass filters are incorporated in the module thereby reducing the conducted noise and the inductor is also inside the package as opposed to the LTM4607 where the inductor is outside the package which results in a potential source of radiated EMI. Furthermore the LTM4607 can also be driven by an external clock. This adds a great advantage in reducing noise because a clock that spreads the spectrum such as the LTC6908-1 can be used. The idea behind using a spread spectrum technique to reduce EMI is to keep the clock moving. Thus the energy released by the device does not have a strong signal at a fixed frequency; instead the energy is spread out randomly within a certain range of frequencies with less intensity. The figure below is a clear example of what happens in the frequency domain when the spectrum is spread and when it is not.

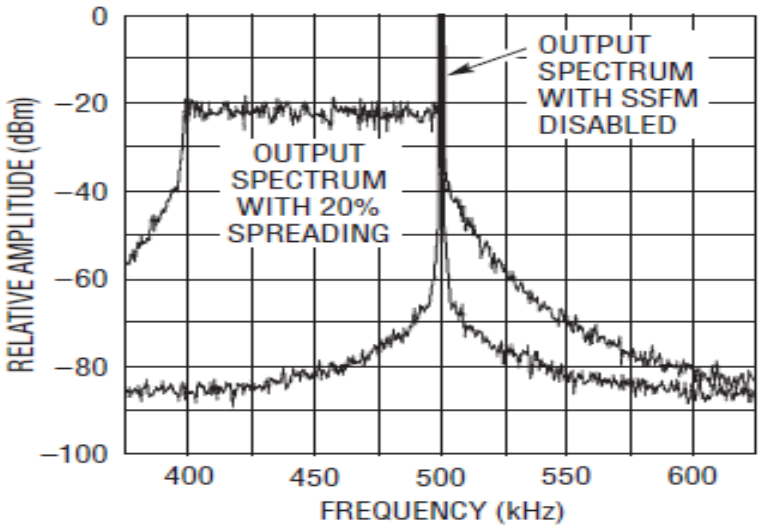

Figure 3.4.2
Frequency spectrum of clock with and without spread spectrum.

Previously it was determined that special care must be taken when paralleling two sources and that the simplest solution to this problem is to find a dc-dc module that addresses the issue. Linear Technology offers what they call the “µModule power supply solutions.” They have developed eight dc/dc µModule families to address specific power requirements**.** The LTM4607 is one of the eight modules of the µModule family. It is a high power surface mount buck/boost package that can handle up to 10A in continuous mode. There is also the LTM4605 which offers an output current of up to 12A; this will indeed solve the problem of having to parallel two chips to get more power. However, there is a

problem with the LTM4605 which is that it can only take an input voltage ranging from 4.5V to 20V and since the voltage provided to the system is 32V, the LTM4605 will not work unless the input voltage is dropped. As opposed to the LTM4605, the LTM4607 input voltage ranges from 4.5V to 36V which meets the input voltage requirement. The only issue with this module is that it can only output a maximum current of 10A and hence paralleling the modules becomes the only solution to get the current needed. Since the first requirement every time two sources are paralleled is to have the same output voltage, the dc/dc module has to be set up to meet this requirement. This is done by programming the output voltage through the internal PWM controller of the LTM4607. Adding a resistor from the Vfb pin to the SGND pin programs the output voltage. The following equation determines the output voltage:

$Vout = (0.8) * [(100k + Rfb) / (Rfb)]$

where Rfb is the resistor across the VFB pin to the SGND pin, see Figure 3.4.3 for pins reference.

The table, Table 3.4.1, below shows the resistance value to get a desired output voltage.

Rfb Resistor (0.5%) vs Output Voltage							
Vout	0.8V	1.5V	2.5V	3.3V	5V	6V	8V
Rfb	Open	115k	47.5k	32.4k	19.1k	15.4k	11k
Vout	9V	10V	12V	15V	16V	20V	24V
Rfb	9.76k	8.66k	7.15k	5.62k	5.23k	4.12k	3.4k

Table 3.4.1 look up table to set up the output voltage for the LTM4607.

Once the two voltages have the same magnitude then they are ready to be paralleled. Linear technology uses a poly-phase parallel configuration**.** The purpose of the configuration is to reduce the output voltage ripple. This is achieved by running an external clock signal that connects to the PLLIN pin of each module with one of the clocks being shifted by 180° electrical degrees. The figure below, Figure 3.4.3, shows the poly-phase configuration.

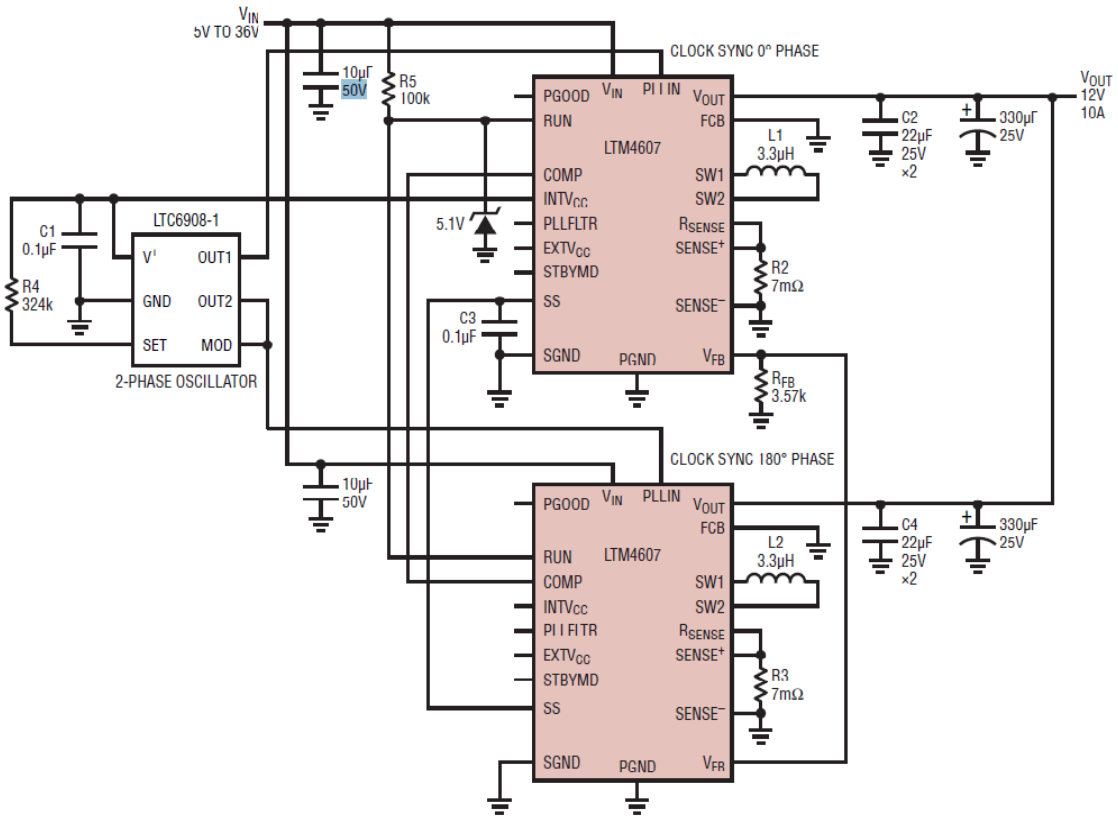

Figure 3.4.3 LTM4607 in Parallel

The schematic above from Linear Technology shows two LTM4607 µmodules connected in parallel. The 2-phase oscillator sends two clock signals that are 180° electrical degrees at a rate of 400 kHz. This is also known as the poly-phase or interleaved switch operation, which lowers the output voltage ripple by a theoretical value of two.

3.5 Thermal

Thermal considerations must be taken into account in any design. The temperature will affect the performance of the system and even may prevent the system from operating if it is not running under necessary temperature ranges. The ambient temperature and junction-to-ambient temperature are measured for each part on a circuit board. The ambient temperature is the temperature of the air around the system when the part is operating, while the junction-to-ambient temperature is the temperature of the silicon die in the part. The ambient temperature is dependent on the PCB layout. The junction-to-ambient temperature is a constant given by the manufacturer of the part multiplied by the dissipated heat of the part. It is measured in degrees Celsius per watt. The temperature of the part is then the ambient temperature added to the calculated junction-to-ambient temperature.

3.6 Communication Protocols

Our project requires a serial communication interface in order to receive and send command and control information to and from the main system. We looked at several serial interfaces. We were given the general specification of how they have accomplished this in previous versions of the missile. This included a generic serial bus using three wires sending a 24 bit address, 8 bits for addressing and 16 bits of data.

3.6.1 I^2C

I^2C is an acronym for Inter Integrated Circuit bus. The bus physically consists of 2 active wires and a ground connection. The I^2C bus was developed by Philips Semiconductor in the early 1980's to maximize hardware efficiency and circuit simplicity. See Figure 2 below. The I^2C interface is simply a master/slave type interface. Simplicity in the I^2C system is primarily due to the bidirectional two wire design, a serial data line (SDA) and serial clock line (SCL). Bi-directional communication is possible through the use of wire (the lines are either passive high or active-low). The I^2C BUS protocol also allows collision detection, clock synchronization and hand-shaking for multi-master systems. The clock is always generated by the master, but the slave may hold it low to generate a wait state. In most systems the microcontroller is the master and the external peripheral devices are slaves.

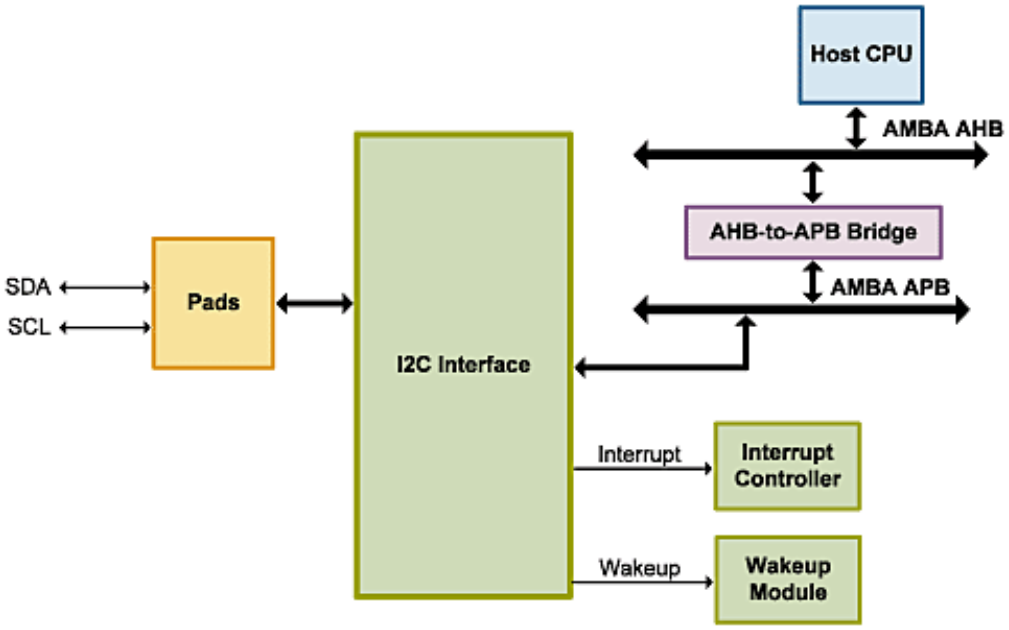

Figure 3.6.1.1: I2C Block Diagram

The active wires, SDA (Serial Data line) and SCL (Serial CLock line), are both bidirectional.The key advantage of this interface is that the SDA and SCL lines are the only two lines required for full duplexed communication between multiple devices and the interface runs at a fairly low speed (100kHz to 400kHz). With I^2C, each component on the bus has a unique address. Chips can act as a receiver and/or transmitter depending on their functionality.

3.6.2 SPI

SPI (Serial Peripheral Interface) is a serial bus standard established by Motorola . Devices communicate using a master/slave relationship, in which the master initiates the data frame. Unlike the I^2C interface SPI has a lack of built-in device addressing so it requires more hardware resources than I^2C when there is more than one slave. SPI tends to be much simpler when only a single master slave relationship exists. Unlike I^2C SPI uses four signals and hence four wires. These signals are the following:

- Serial Clock (SCLK)
- MOSI/SIMO (Master Output, Slave Input)
- MISO/SOMI (Master Input, Slave Output)
- (ÇSS) slave select

As shown in the figure below, the SCLK line is the clock line, the clock is generated by the master and drives the communication in both directions, and this line is an input to all slaves. The MOSI line is the master data output, slave data input, and it carries data from the master to the slave. The MISO line is the master data input, slave data output, and it carries data from the slave to the master. Finally the SS or sometimes known as the CS line is the slave select or chip select line, it is toggled to select a slave to communicate.

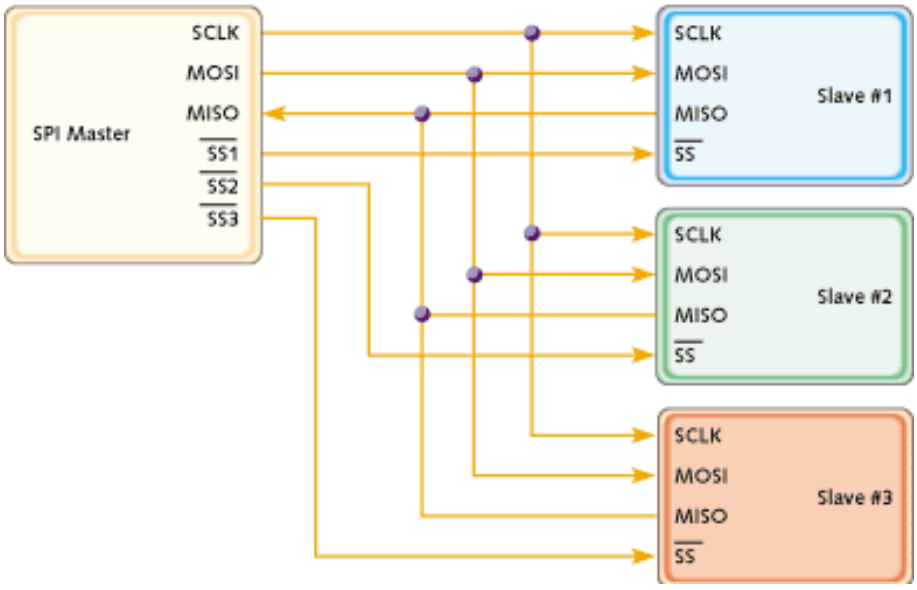

Figure 3.6.2.1 Master to slave communication

Having four wires, while not completely undesirable, does have its drawbacks in the area of space requirement. Since size is probably our most limiting requirement we decided to look for other solutions that have the least amount of wires for the desired affect. While wire size is not the only limiting factor, it is of course one, that cannot be overlooked.

3.6.3 UART(universal asynchronous receiver/transmitter)

This protocol (see Figure 3.6.3.1 below) is either a synchronous USART or asynchronous serial transmission (UART). In synchronous mode it is required that the sender and receiver share a clock with one another, or that the sender provide some other timing signal to the receiver for the next bit of the data. The downside of this synchronous communication is that it can require extra wiring or circuits to share the clock signal between the sender and receiver. In most forms of serial synchronous communication, if there is no data available at the time of transmit, blank characters must be sent so that data is always being transmitted. This is where synchronous communication is usually more efficient because only data bits are transmitted between sender and receiver.

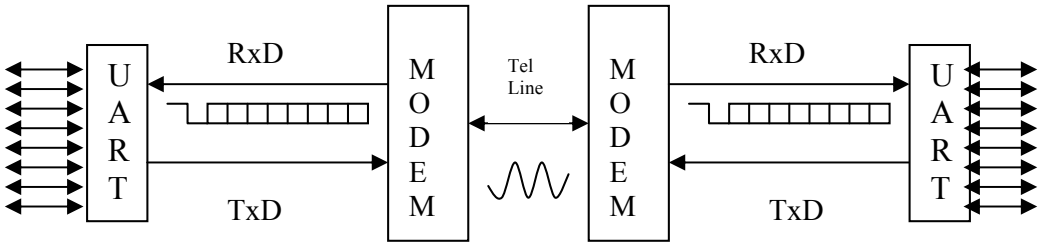

Figure 3.6.3.1 UART to Modem (PENDING PERMISSION FROM ACTEL)

In asynchronous mode the sender and receiver must agree on timing parameters in advance. To do this extra bits must be added to each word which are then used to synchronize the sending and receiving units. When a word is given to the UART for Asynchronous transmissions, a start bit is added to the beginning of each word that is to be transmitted. This start bit is used to alert the receiver that a word of data is about to be sent, and to force the clock in the receiver into synchronization with the clock in the transmitter. These two clocks must be accurate enough to not have the frequency drift by more than 10% during the transmission of the remaining bits in the word. After the Start Bit, the individual bits of the word of data are sent, with the least significant bit (LSB) being sent first. Each bit in the transmission is transmitted for exactly the same amount of time as all of the other bits, and the receiver “looks” at the wire at approximately halfway through the period assigned to each bit to determine if the bit is a 1 or a 0. After the entire data word has been sent the transmitter may add a parity bit that the transmitter generates. The parity it can be used by the receiver to perform error checking. Then a stop bit is sent by the transmitter.

3.6.4 1-Wire

The Maxim 1-Wire interface is a simple communication and device power delivery scheme that multiplexes both device signaling and power on an interface consisting of a single contact and ground return. The basis of 1-Wire technology is a serial protocol using a single data line plus ground reference for communication. 1-Wire is the only voltage-based digital system that works with two contacts, data and ground, for half-duplex bidirectional communication. A typical 1-Wire configuration will contain a single master and one or more slave devices sharing a common 1-Wire line. Communication is half-duplex and always controlled by the master.

Benefits of the 1-wire interface are the following:

- Single Contact Sufficient for Control and Operation
- Unique ID Factory-Lasered in Each Device
- Power Derived from Signal Bus ("Parasitically Powered")

- Multi-drop Capable: Supports Multiple Devices on Single Line
- Exceptional ESD Performance

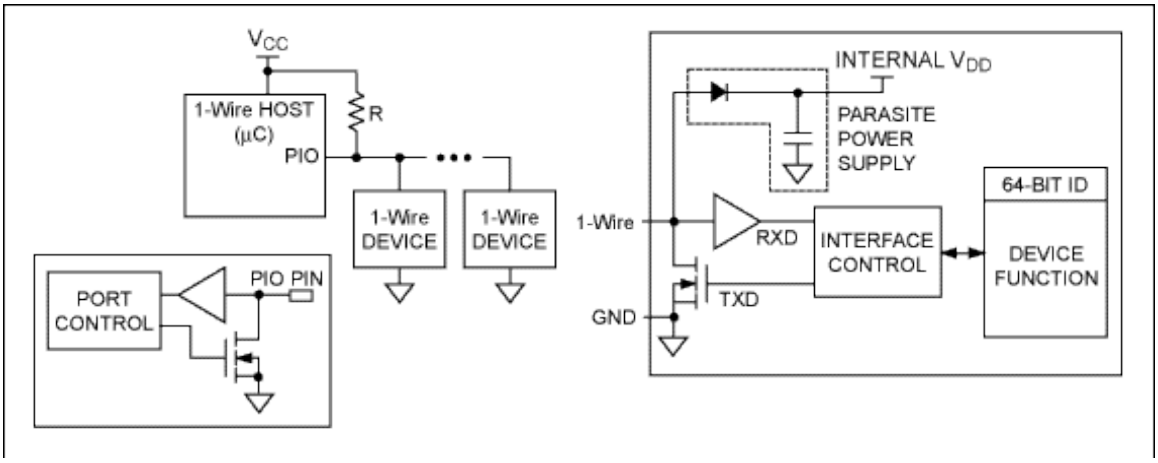

Figure 3.6.4.1 Internal 1-Wire (PERMISSION PENDING FROM MAXIM)

A 1-Wire master initiates the communication with one or more 1-Wire slave devices on the 1-Wire bus. Each 1-Wire slave device has a unique, unalterable, factory-programmed, 64-bit identification, which serves as it's device address. An 8-bit family code, which is a subset of the 64-bit ID, identifies the device type and functionality. 1-Wire slave devices operate in two different modes:

Parasitic Mode:
- The slave device operates directly off off the power from the bus.

Normal
- They draw off of a voltage input ranging from 2.8V-5.25V

3.7 Power Architecture

3.7.1 Linear Voltage Regulator

Linear regulator is another type of power supply, but this type usually handles lower voltages because it generates heat and can only step-down voltage. A linear regulator uses either a bipolar transistor or MOSFET, to convert the voltage. The bipolar transistor or MOSFET generates the heat because they effectively act as resistors. It is only 35 to 65 percent efficient. However, they do not create significant noise. Linear regulators have a time delay in which to respond to the change in load current. There are three different types of linear regulators. They are the low dropout regulator (LDO), standard regulator, and quasi LDO regulator. One of the main differences between them is the drop out voltage. The higher the dropout voltage the more power the regulator dissipates, and this creates a heat issue. The standard regulator has the largest dropout

voltage making it the least efficient. However, the LDO regulator has the lowest dropout voltage, which makes it the most efficient. The second main factor is the ground current. The ground current is supplied by the source, but is not used on the load. The current is unused and, therefore, 'wasted'. In this case, the standard regulator is more efficient because it has the lowest ground current.

3.7.2 DC-DC Converter

The switching power supply is one type of power supply. The power supply is usually used for higher voltages when considering low heat dissipation. The uniqueness of the power supply is that it used a transformer to step-down or step-up the voltage. It is quite efficient ranging from 65 to 95 percent. The signal is then converted to a DC signal to output. However, a great disadvantage is the RFI noise that it causes because of the high frequency switching in the transformer. Topology is an important consideration when using this type of power supply. Generally, if the switching power supply needs to handle over 40 volts there is a specific topology that must used to safety precaution. Considerations in topology also include, multiple outputs, voltage stress, and current stress. The PCB layout is also fundamental consideration in the design of the board. Traces can behave as inductors and resistors. If a trace is long and there are continuous changes in current, high voltages can be created. Also, the width of the traces must be considered. If the traces are too narrow, a high voltage drop can occur because current cannot flow as readily creating the affect of an antenna and, thus, introducing unnecessary noise.

The objective of the design is to process a raw input power into a conditioned output power. In the process, a device has to be utilized so that the flow of energy between the source and the load has very little resistance. A century ago, a resistive element would have been used in order to get a desired voltage. Consequently, the energy dissipated across the resistor would have been the squared of the current flowing through the resistor times its resistance, thus resulting in a very inefficient system. With the development of semiconductors, a new industry, power electronics, has emerged in which power transfer between a source and a load with a conditioned output power is possible. Power electronics takes advantage of passive and active components to make power transfer between two points as efficient as possible.

A DC/DC converter is a system that takes an input voltage and outputs either a higher voltage, same voltage or lower voltage to the load. When the output voltage is higher than the input voltage, the DC/DC converter is called a boost converter and when the output voltage is lower than the input voltage the converter is called a buck converter. For this design, an input power of +32V has to be processed into six different low voltages; therefore, the buck converter will be the focus of this section. A simplified version of a buck converter is shown below in figure 3.7.2.1

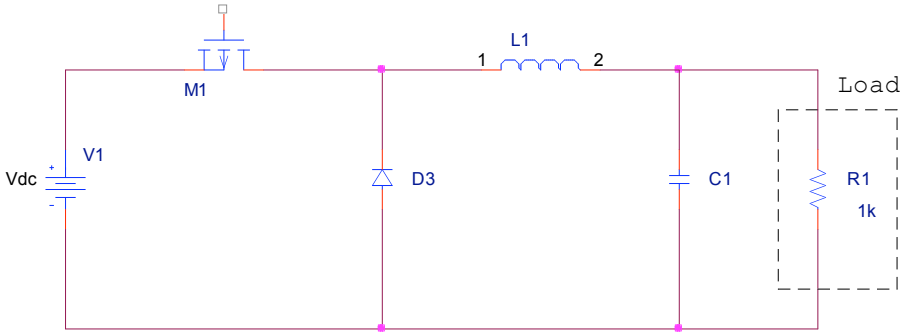

Figure 3.7.2.1 Simplified schematic of a buck converter

As seen in the figure above, the buck converter consists of the following elements:

- A dc input voltage source Vdc. This is the incoming raw power to the network that has to be conditioned.
- A MOSFET which acts as a controlled switch. The MOSFET is controlled by a driver circuitry.
- A diode set up to provide a path for the current when the MOSFET is opened.
- A filter inductor L and a filter capacitor C. Under the assumption that the inductor current is always positive and never zero, the converter is called the 'continuous conduction mode.'

It can be seen from the circuit above that when the switch is on or the MOSFET is commanded to the on state, the diode D is reverse-biased. When the switch is off, the diode conducts to provide a path for the current in the inductor. Consequently, when the switch is on and current is flowing through the inductor, a positive voltage results across the inductor, VL = Vg-Vo. This voltage causes a linear increase in the inductor current. When the switch is turned off, the current keeps flowing through the inductor because of the energy stored in the magnetic field, and as mentioned before this current flows through the diode until the switch is turned again. By controlling the duty cycle of the on and off states, the output voltage can be controlled with the following equation, Vo = D*Vin

The equations for the relationships among input voltage, output voltage, duty cycle, and other voltages in the circuit can be derived by solving two circuits which account for the switch being on and off. These equations are available in the literature along with its derivations.

The DC/DC umodule family is a new family created by Linear Technology. The umodule regulator is a complete system integrated in one substrate. The system contains the MOSFET and its controller inside the package. In this family, Linear Technology has incorporated previous designs into one package where efficiency is improved.

The micro-module family falls under the category of High Efficiency dc/dc converters. No doubt efficiency is one of the most important aspects of the application requirements for the power supply; however, there is a requirement that is more important than efficiency and that is the radiated and conductive noise introduced by the module. It is well known that dc/dc converters introduce conductive noise due to the high frequency switching inside the modules and radiated noise is created by the magnetic fields of the inductor used in the circuit. Since the power supply will power a transmitter, the noise requirements are extremely tight. Any noise introduced by the power supply leads to catastrophic effects in the system.

The ultra-low noise devices in the micro-module family have been designed at Linear Technology so that radiated and conducted EMI caused by the device is minimized. In order to achieve reduction in EMI, low pass filters have been incorporated in the modules thus reducing high frequencies that may cause interference with adjacent circuitry. The module has also been designed so that common mode rejection is optimized within the package. The ultra-low noise modules also allow the use of external clocks to drive the converter. This allows the designer to choose spread frequency oscillators. By spreading the frequency, the energy concentrated at the switching frequency can then be spread within a plus or minus 10 percent margin. This is achieved by allowing the clock frequency vary within a margin from the center frequency.

3.7.2.1 Paralleling dc/dc converters

The power supply for the transmitter requires a pulsed current of 11 Amps with a variable frequency that ranges in between 10-100 kHz. In order to obtain efficiencies higher than 90% dc to dc converters have to be implemented. In recent years, with the explosion of laptop computers and portable electronics such as cell-phones a new industry has emerged in low power electronics. This sector contains integrated circuits (ICs) that perform buck and boost topologies leaving the designer with the option of choosing bulky output capacitors, inductors and resistors to meet the design requirements. Typically most small sized dc-dc converter modules only provide a current of 8Amps or less with output voltages of 3.5V. Because of this, paralleling the output of the dc-dc converter is desired in order to boost up the current. However; it is well known that when two sources are paralleled, they must have the same magnitude, phase, and frequency so that there is no potential difference between the two sources. In this application, making sure that the two sources have the same frequency or phase is not a concern since the output of the sources is DC. Thus in order to protect the dc to dc modules; they must have the same magnitude. An easy way to protect the chips in case there is a potential difference between the two sources is to place a diode on the output of the positive lead of each dc-dc converter IC as shown below in Figure 3.7.2.1.1.

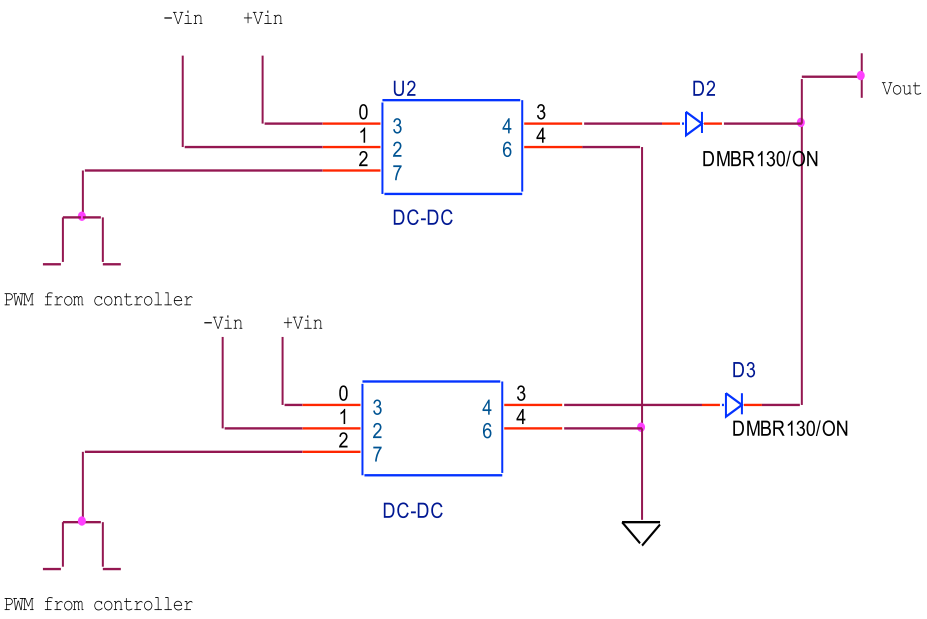

Figure 3.7.2.1.1
Simple way of protecting dc/dc modules in parallel mode.

Although the solution presented above works for many small signal applications that is not the case for the high power source to be designed because of the heat created by the diode losses. As stated previously, the current drawn by the load will be a pulsed with a frequency that ranges from 10 kHz to 100 kHz with a peak of 11 amps at 50% duty cycle or less. Therefore, if diodes are placed at the outputs of the dc-dc package, the conduction losses attributed by the diodes will be close to 9 watts plus the switching losses. Because of this, using diodes to protect the chips is not the best solution. Another way to solve this issue is to find a dc to dc package that offers the option of paralleling the outputs.

3.7.2.2 Ripple attenuation

The 6XMIT or the highest power supply of the system is used to drive the transmitter which draws a pulsed current with a peak of 11A and with a duty cycle less than 50 percent. The requirement for the voltage supplied to the load must have a low-ripple-voltage no greater than 1mV. As a result, choosing the right components becomes a critical part of the design. The µModule dc/dc converters family by Linear Technology offers the ability to design a power supply with a specific output voltage ripple and the equations are as follows:
The ripple percentage is typically set to 20% to 40% of the maximum inductor current. As seen in the equation,

Vripple = [*Vout* (*Vin* - *Vout*)] / [8 * L * *Cout* * *Vin* * *f*^2],

the output ripple voltage depends on several variables. The frequency of the device can be set anywhere between 200 kHz-400 kHz. This can be set up in two different ways; one way is to provide a clock signal to the device by connecting it to the INTVcc pin or by applying a voltage that ranges from 0.5 V – 2V to the PLLFLTR Pin, where 0.5V equals 200 kHz and 2V equals 400 kHz. The range in between the two frequencies is linear. The disadvantage of the latter option is that the efficiency of the dc/dc module decreases because power dissipates across the MOSFET in charge of setting up the frequency inside the module. Once the frequency of the dc/dc converter is chosen, the selection of the inductor follows next. The inductance is first found by using the formula above, once the inductor value is known then the proprieties of the inductor have to be considered. An inductor with a low DC resistance is preferred so that the I^2R losses are minimized. Also the inductor must be able to handle the peak inductor current without saturation. To minimize radiated noise, a toroid, pot core or shielded bobbing inductor is preferred.

The input voltage, output voltage and load current have already been assigned. Vin equals 32V, Vout equals 6V and the load current is 11 A. The only variable left out in order to solve for Vripple is the output capacitors. The bulk output capacitors are chosen such as their equivalent series resistance or ESR is as low as possible to meet the output voltage ripple and transient requirements. The most common capacitors used to meet low ripple specs are the low ESR tantalum capacitor, the low ESR polymer capacitor or the ceramic capacitor**.** In addition, placing the output capacitors in paralleled is optimal due to the fact that these adds more capacitance and lowers the ESR value, the lower the ESR the better. The table below, Table 3.7.2.2.1, provided by Linear Technology shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoots at a current transient.

V_{IN} (V)	V_{OUT} (V)	R_{SENSE} (0.5W RATING)	Inductor (µH)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	$I_{OUT(MAX)}$* (A)
12	5	2 × 18mΩ 0.5W	2.2	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	12
20	5	2 × 18mΩ 0.5W	2.5	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	12
24	5	2 × 18mΩ 0.5W	2.5	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	12
32	5	2 × 20mΩ 0.5W	3.3	2 × 10µF 50V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	10
36	5	2 × 20mΩ 0.5W	3.3	2 × 10µF 50V	150µF 50V	2 × 22µF 25V	2 × 180µF 16V	10
5	8	2 × 16mW 0.5W	1.5	None	150µF 35V	4 × 22µF 25V	2 × 180µF 16V	7
12	8	2 × 18mΩ 0.5W	2.2	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	12
20	8	2 × 20mW 0.5W	3.3	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	11
24	8	2 × 20mΩ 0.5W	3.3	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	11
32	8	2 × 20mΩ 0.5W	4.7	2 × 10µF 50V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	10
36	8	2 × 22mΩ 0.5W	4.7	2 × 10µF 50V	150µF 50V	2 × 22µF 25V	2 × 180µF 16V	10
5	10	2 × 16mW 0.5W	2.2	None	150µF 35V	4 × 22µF 25V	2 × 180µF 16V	6
15	10	2 × 18mW 0.5W	2.2	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	12
20	10	2 × 20mW 0.5W	3.3	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	11
24	10	2 × 18mΩ 0.5W	3.3	2 × 10µF 25V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	11
32	10	2 × 22mΩ 0.5W	4.7	2 × 10µF 50V	150µF 35V	2 × 22µF 25V	2 × 180µF 16V	10

Table 3.7.2.2.1
Typical components for different power requirements where f = 400 kHz.
(Permission pending from Linear Technology)

3.7.2.3 LTM4607 µModule

The LTM 4607 falls under the category of High Efficiency dc/dc converters of the µModule family. No doubt efficiency is one of the most important aspects of the application requirements for the power supply; however, there is a requirement that is more important than efficiency and that is the radiated and conductive noise introduced by the module. It is well known that dc/dc converters introduce conductive noise due to the high frequency switching inside the modules and radiated noise is created by the magnetic fields of the inductor used in the circuit. Since the power supply will power a transmitter, the noise requirements are extremely tight. Any noise introduced by the power supply leads to catastrophic effects in the system. Therefore, if the LTM4607 ends up being the component selected, an evaluation board has to be acquired in order to learn more about the noise that this module introduces.

3.7.2.4 LTM4612 uModule

The LTM4612 belongs to the family of 'ultra-low noise' DC/DC converters. It operates with a wide range of input voltages from 5V to 36V and can provide output voltages from 3.3V to 15V set by a single resistor. The maximum continuous current that the module can provide is 5A and the maximum peak

current is 7A. The only components that the designer has to choose are bulk input and output capacitors to finish the design. The output capacitor is chosen to satisfy several requirements. Since capacitors are not ideal, parasitic components have to be taken into account. In general, a capacitor contains an equivalent series resistance or ESR and an equivalent series inductance also known as ESL. The ESR of a capacitor plays a role in the ripple of the output voltage. By referring to the right side of Figure 3.7.2.4.1 below, one can see that the choke will have a ripple current introduced by the switching element.

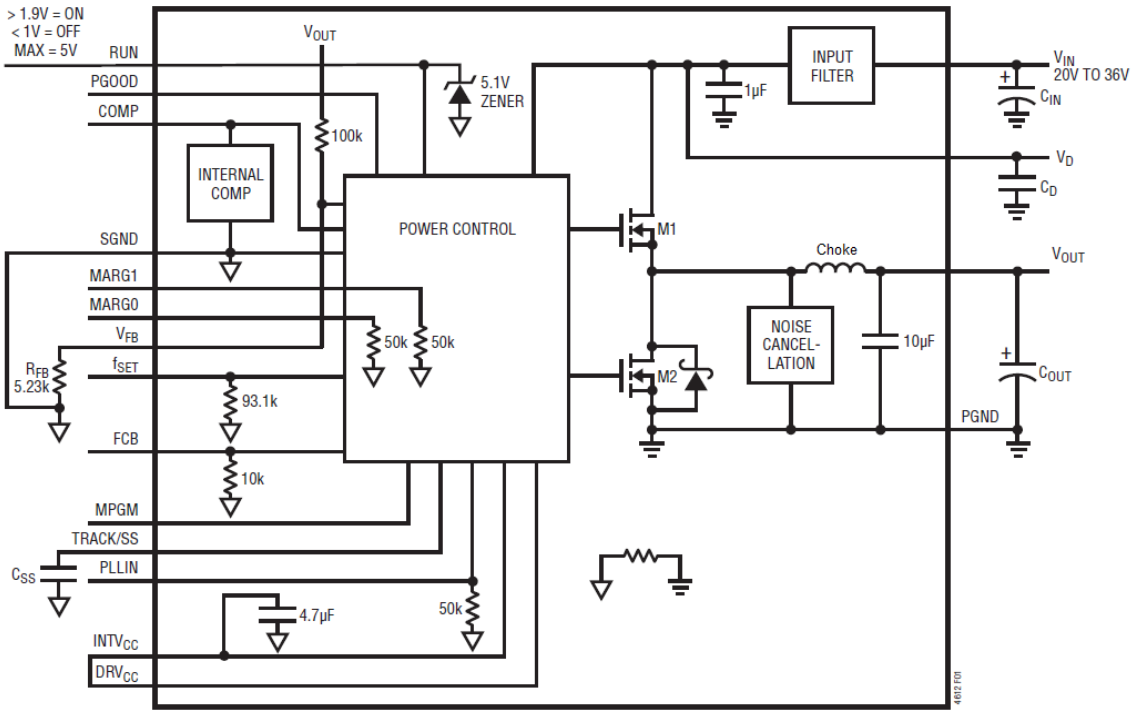

Figure 3.7.2.4.1
Simplified schematic of the LTM4612 module
(Permission pending from Linear Technology)

When the switching element turns on, the choke stores energy in its magnetic field. When the switch turns off the choke, it will create a voltage that will try to keep the current flowing as long as there is energy in the magnetic field, according to Lenz's law. This phenomenon creates a high frequency current ripple in the choke where the high frequency is introduced by the switching element. In the Figure 3.7.2.4.2 below, the ripple caused the inductor in the LTM4612 module is shown with respect to the output voltage. In addition, the high ripple current will follow the path with the least resistance which is provided by the output capacitor at high frequencies thereby generating a ripple on the output voltage because of the output's capacitor ESR. Thus, the ESR of the capacitor has to be chosen so that it is as small as possible. Modern low ESR

electrolytic capacitors are now designed for DC/DC applications, and the ESR values are provided by the manufacturers. As far as the ESL is concerned, it can generally be neglected for switching frequencies below 500 kHz.

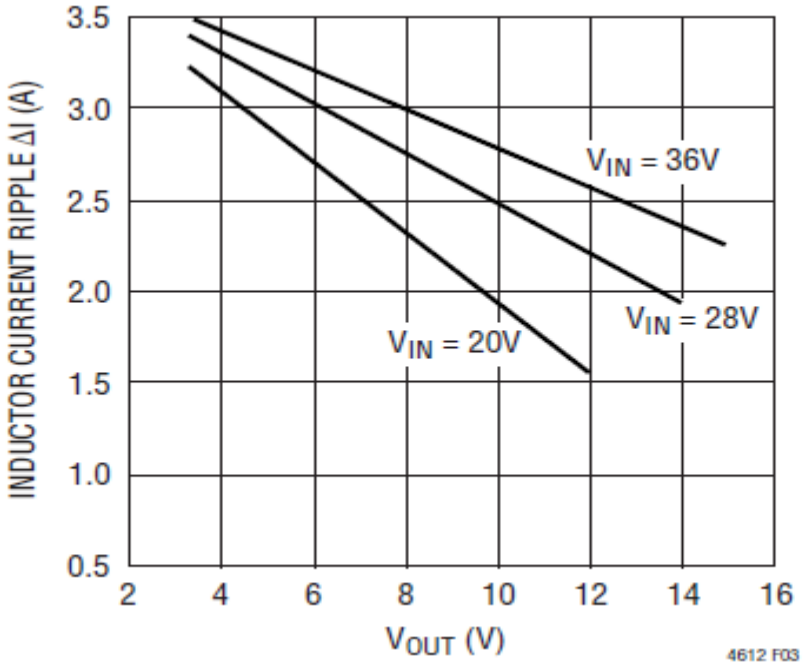

Figure 3.7.2.4.2
Inductor current ripple vs. output voltage
(permission pending from Linear Technology)

To be precise, there are two ripples that are introduced by the output capacitor and its equivalent series resistance. They are not in phase because the ripple generated by the ESR is proportional to I2-I1. The ripple due to the output capacitor is proportional to the integral of that current. However, for a worst-case comparison one can make the assumption that they are in phase, hence when they are not in phase the ripple is less.

The LTM4612 employs a high switching frequency and an adaptive on-time current mode architecture that enables a very fast transient response to line and load changes without sacrificing stability. It also has an onboard input filter and noise cancellation circuits that achieve low noise coupling which help on reducing the EMI; this is shown in 3.5.2.4. Furthermore, the DC/DC module can be synchronized with an external clock for reducing undesirable frequency and allows poly-phase operation for high load currents. Usually, a spread spectrum oscillator is used as the clock. The frequency of the oscillator is set to a fixed value with the ability to vary within a certain margin, usually plus or minus 10%. By spreading the spectrum, the energy associated with the driver for the switching element is essentially spread within frequencies close to the center

frequency. If the spreading of the spectrum technique is not utilized, all the energy coming from the driver for the switching element is concentrated on the center frequency. Figure 3.5.2.6 and figure 3.5.2.7 below show simulated results where the difference between spreading the spectrum and not spreading the spectrum is clearly seen.

In general, poly-phase operation is desired when dc/dc converters have to output more than the rated current. The LTM4612, just like the LTM4606 gives the designer the option of paralleling the modules for high load currents. Furthermore, the LTM4612 allows the paralleled modules to have very good current sharing because it is a current mode controlled device. The current mode controller limits the cycle by cycle inductor current during transients and steady state operation. The controller also provides a foldback current limiter that limits the current in the event of an overload condition. Additionally, if the output voltage falls by more than 50 percent, then the maximum output current is progressively lowered to about one sixth of its full current limit value. The output voltage on the LTM4612 is set by using the equation below.

$Vout = 0.6V\,[(100k/N) + (Rfb)]\,/\,[Rfb]$

The following diagram, Figure 3.7.2.4.3, is the frequency spectrum.

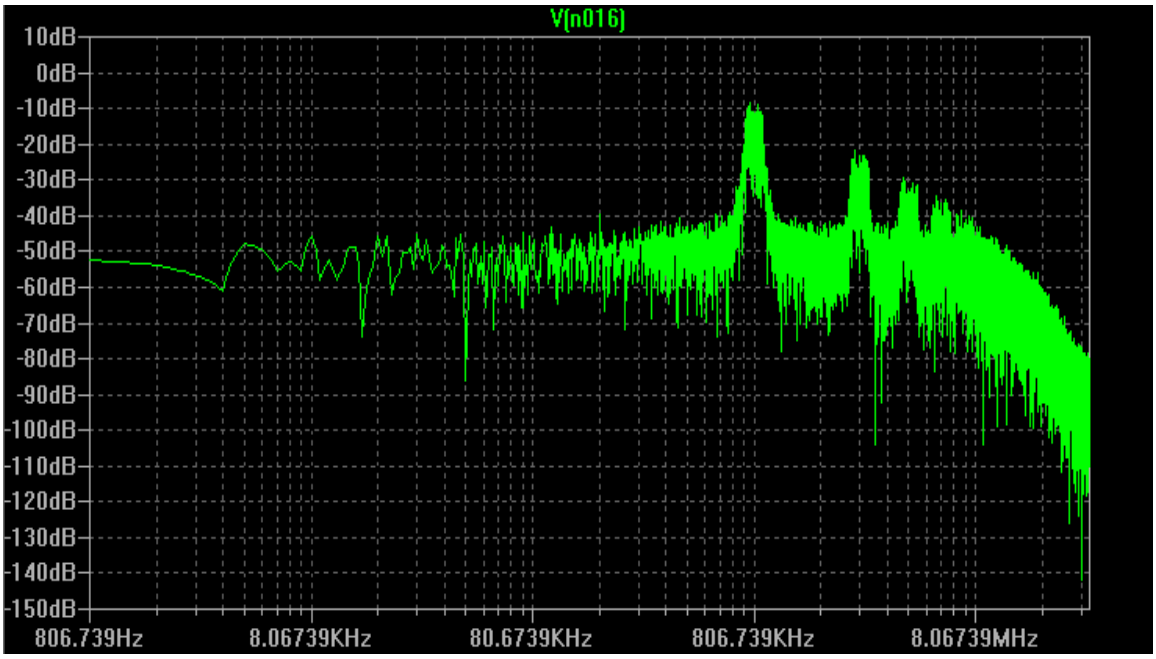

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Figure 3.7.2.4.3
Frequency spectrum of the clock signal for the LTM4612 utilizing the spread spectrum technique.

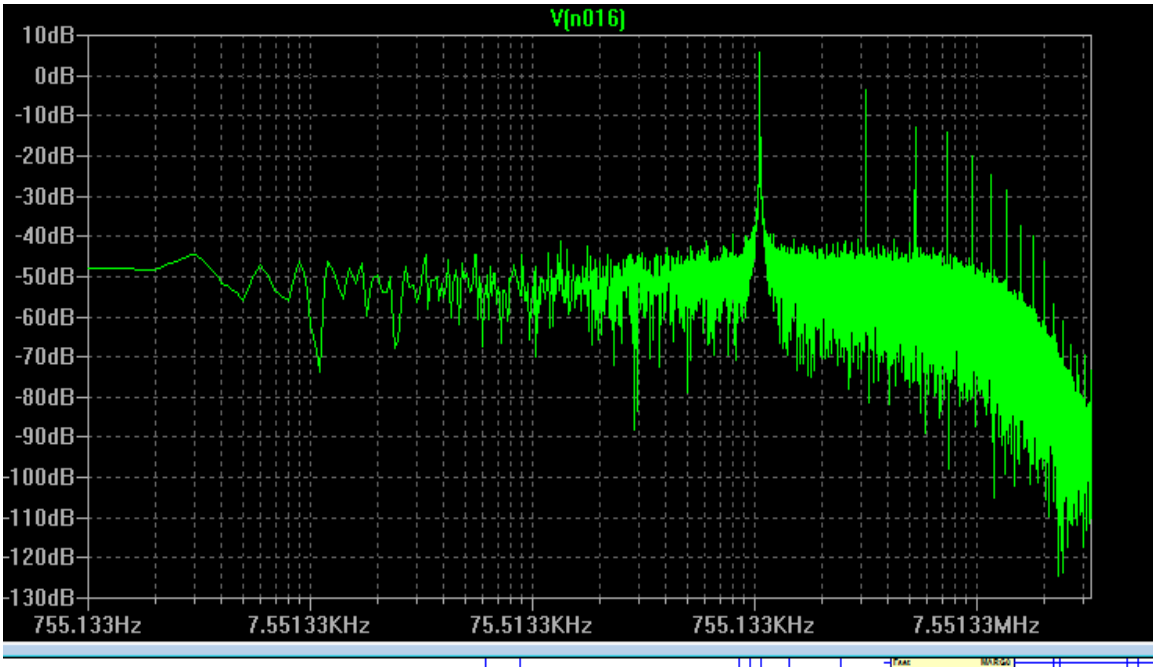


Figure 3.7.2.4.4.
Spectrum of clock when the spreading spectrum technique is not used

The figures above clearly show that more energy is concentrated at the switching frequency when the spreading spectrum technique is not implemented. One drawback that could result from having a lot of energy concentrated at one point is EMI. Thus, in order to prevent EMI, a device that spreads the spectrum should be considered in the design phase.

3.7.2.5 LTM4612 Pins

Knowing the pins of the device will expedite both the simulation and design process. As a result, the purpose of this section is to describe the different pins and its functions. All the pins are shown in Figure 3.7.2.5.1 below. Directly below are the pin functions.

VIN: The source is connected across this pin and GND. It is recommended the placement of decoupling capacitance between this pin and GND.

PGND: Power ground pins for input and output returns. It is important to note here that the LTM4612 does not provide isolation; therefore, an internal slow blow fuse should be added in the circuit to protect the unit from catastrophic failure.

Vout: The load is connected across this pin and PGND. It is recommended to place decoupling capacitance across this pin and PGND. It should be connected as close to the pins as possible.

Vd (pins B7, C7): Top FET drain pins. Adding more capacitors between this pin and PGND will reduce the input ripple to the module.

DRVcc(Pins C10, E11, E12): Usually these pins are connected to INTVcc for powering the internal MOSFET drivers. An internal low dropout regulator produces an internal 5V supply that powers the control circuitry and DRVcc, equation 3 calculates the power dissipated by the regulator. The power dissipated with the 32V input voltage is 0.54W. Therefore, this pin should be biased with an external voltage no greater than 6V and 50mA to improve the efficiency of the unit. By doing this, the losses will be 20mA*5V which equals 0.1W as opposed to 0.54W.

*Ploss = 20mA ** (*Vin - 5V*)……. equation 3

INTVcc(Pin A7): This pin is for additional decoupling of the 5V internal regulator.

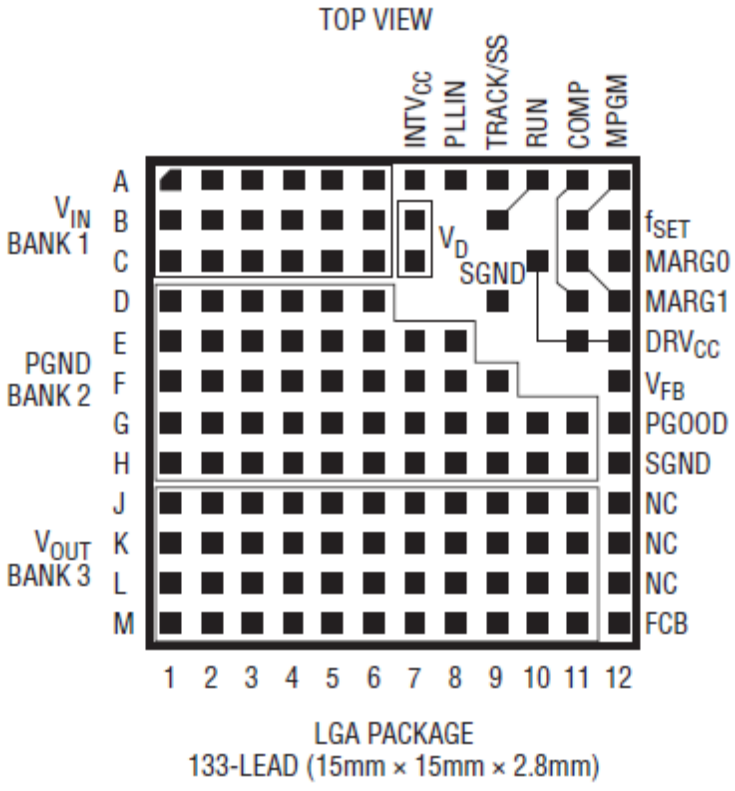


Figure 3.7.2.5.1
LTM4612 Pin configuration. Linear Technology LTM4612 Datasheet.

PLLIN (Pin A8): This pin gives the designer the option of using external clock synchronization to the phase detector. The LTM4612 has a phase-locked loop

comprised of an internal voltage controlled oscillator and a phase detector. This allows the internal top MOSFET turn-on to be locked to the rising edge of the external clock. The frequency range is +- 30% around the set operating frequency. A pulse detection circuit is used to detect a clock on the PLLIN pin to turn on the phase-locked loop.

FCB: This pin forces continuous mode operation when connected to PGND or discontinuous mode operation when connected to INTVcc.

Track/SS (pin A9): One of the requirements on this design is power sequencing. By placing a capacitor across the Track pin and PGND the ramp rate can controlled. A soft start capacitor can be used for soft start turn on as a standalone regulator. In addition, output voltage tracking can be programmed externally using this pin. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider.

MPGM (Pins A12, B11): Programmable Margining Input. A resistor from these pins to ground sets a current that is equal to 1.18V/R. This current multiplied by 10k will equal a value in millivolts that is a percentage of the 0.6V reference voltage. When paralleling two modules, the MPGM pin requires an individual resistor.

RUN (Pins A10, B9): Run Control Pins. A voltage above 1.9V will turn on the module, and below 1V will turn off the module. A programmable UVLO function can be accomplished with a resistor from VIN to this pin that is has a 5.1V zener to ground. Maximum pin voltage is 5V. The run pin will make the down power sequencing easier because the only thing that the FPGA has to do is send a low signal to the pin in order to shut off the module.

PGOOD (Pin G12): Output Voltage Power Good Indicator. Open-drain logic output is pulled to ground when the output voltage is not within +- 10% of the regulation point. This occurs after a 25µs power bad mask timer expires.

SGND (Pins D9, H12): Signal Ground Pins. These pins connect to PGND at output capacitor point.

Comp pin: The comp pin is the external compensation pin. Although the module has already been internally compensated for most output voltages, this pin provides the designer more options for optimizing the control loop.

FSET (Pin B12): Frequency Set Internally to 850 kHz at 12V Output. An external resistor can be placed from this pin to ground to increase frequency. This pin can be decoupled with a 1000pF capacitor.

VFB (Pin F12): The Negative Input of the Error Amplifier. Internally, this pin is connected to VOUT with a 100k precision resistor. Different output voltages can be programmed with an additional resistor between the VFB and SGND pins.

3.7.2.6 LTM4612 Summary

The LTM4612 is a standalone non-isolated DC/DC power module. It is able to deliver up to 5A of continuous current and a maximum peak current of 7 A. This is accomplished with the help of external input and output capacitors. The input capacitors reduced the incoming ripple from the source. In this application, input capacitors will not be a major concern because the source provided to the power supply has a low ripple of 100uV. The module also provides precisely regulated output voltage which is programmable by a single resistor, Rfb. As mentioned previously, the LTM4612 has an integrated constant on-time current mode regulator with FETs that have ultralow Rds on, thereby improving the efficiency at high loads. The typical switching frequency of the module is 850 kHz at full load. The internal feedback loop compensation gives the LTM4612 sufficient stability margins and good transient performance under a wide range of operating conditions. The LTM4612 also belongs to the family of ultra-low noise switching power modules. It provides internal filters and noise cancelling circuits that achieve low noise coupling.

Current mode control provides cycle by cycle current limiting. In case an over-current occurs, the LTM4612 provides protection circuitry. Internal overvoltage and undervoltage comparators pull the open drain PGOOD output low if the output feedback voltage is within a +- 10% margin. If an output overvoltage exists, the internal FET M1 is turned off and the FET M2 is held on until the overvoltage is cleared. Figure 3.7.2.4.1 shows the location of M1 and M2 Pulling the RUN pin below 1V forces the controller into its shutdown state by turning off both M1 and M2. The RUN pin will facilitate the power sequencing algorithm set by the FPGA.

To make the LTM4612 more efficient, the DRVcc should be connected to an external 5V external bias supply. By doing this, efficiency improvement will occur due to the reduced power loss in the internal linear regulator. Since the input voltage to the module is relatively high, biasing the DRVcc should be considered. If the DRVcc is not biased with an external source, then pins INTVcc and DRVcc have to be connected. This will trigger the internal 5V linear regulator that is in charge of powering the internal gate drivers.

Overall, the LTM4612 provides all the characteristics needed for the design of the high power module mainly because of its ultralow noise characteristics as well as its capability of accepting high input voltages. Furthermore, the ability of connect as many modules as desired makes this device the perfect choice for the high power supply. Its current mode controller and protections are also a great feature to have because it reduces the need of extra circuitry in the PCB. All

these features plus being a module designed for low output voltage ripple makes the LTM4612 a great choice.

3.8 Positive to Negative Voltage Converter

As the name implies, this device takes a positive input and outputs a negative voltage. A positive to negative voltage converter can be a buck-boost switching power supply. A buck-boost converter creates a negative voltage by canceling out the oscillations produced in the process. A negative impedance is created in result, thus getting a negative voltage.

3.9 Ripple Attenuator

A ripple attenuator can be used when a device outputs ripple voltage higher than tolerances in the design allow. The device takes the AC noise of the DC signal out. The noise of the signal must be known to select the proper attenuator. The specifications are given by specifying the noise of a certain frequency range. The ripple attenuator must be rated for a specific frequency range.

3.10 PCB Layout and Topology

The PCB layout is the design of the physical circuit board. There are methods for mounting parts on the board, and there are methods for routing the wire to interconnect every part in the circuit. Often, the board consists for several layers of different material. Top and bottom layers have the footprints of the parts. The footprint consists of the actual solder points for a part. The layers in between will function as the ground plane, power plane, or signal layer. The layers must be in proper order in order to avoid unwanted short circuits or open circuits. The diagram below, Figure 3.10.1, does not in any way reflect the proper layer stack-up. It just demonstrates the layers needed in a PCB layout.

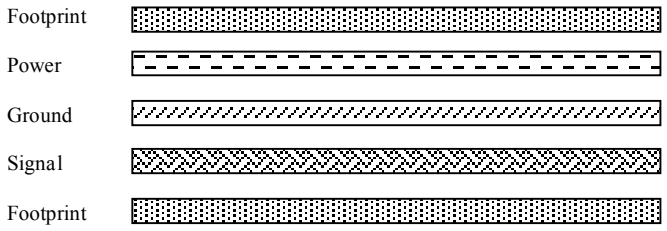


Figure 3.10.1 PCB Layout

It is imperative to consider the amount of current running through wire traces. The wire traces will have to be a certain width corresponding with the amount of current. The width and length of the traces are crucial. Depending on the amount of current flowing through the trace will determine the width. The length should be as short as possible to eliminate losses. Higher current such as 10

amps would require a width of about 500 mils. For lower current such as 100mA would require a width of about 1 mil. Often, 1 layer will be dedicated to high power signals. To avoid crosstalk, traces must not run too close together. Layer to layer signals should be perpendicular, they must not run parallel to each other either to avoid EMI problems. The diagram below, Figure 3.10.2, shows how the traces must be laid out from layer to layer.

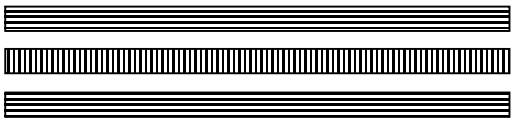


Figure 3.10.2 Perpendicular traces

Thermal conditions must also be considered. Certain parts may need to be laid out in a specific area of the board. When installing and soldering a part, high heat on another part nearby may be harmful. Through-hole and surface mounted parts are a large consideration in topology. The through-hole parts produce more heat and take more space. However, the surface mounted parts are more expensive.

3.11 Filtering

Capacitors have a fundamental function in the design of a circuit. They will filter the signal for a desire input or output. For example, the input signal to a linear regulator from a switching power supply would, normally, be a ramp function. However, there must be a constant signal. The capacitors would produce this desired function with the correct capacitance values. Capacitors will provide instant power when the switch is closed. Depending on the application this may be desirable. Turbo Caps from TTI are a new solution to saving valuable space on the printed wiring board (PWB). These capacitors can be vertically stacked. These ceramic capacitors are ideal for filtering both input and output of switching power supplies. They can handle high current at high frequencies and high power. Also, they can handle operating temperatures from -55 degrees Celsius to +85 degrees Celsius. Of course, this type of capacitor can handle high frequencies, but, often, the capacitance is lost at RF frequencies. They do not handle AC signals either between of the constant switching. Capacitors can introduce unnecessary inductance to the circuit. At extreme high temperatures and extreme low temperatures, they can lose capacitance. Most sensitive type of capacitor is the electrolytic capacitor. Capacitors are also often used to eliminate ripple voltage on the power lines. The capacitor is also used to place between power and ground. These are referred to as decoupling capacitors. This is a fail proof way of isolating power from ground.

3.12 Analog to Digital Signals

Voltage supervisor is an IC used to monitor the output of a device. Logic high will output if the set voltage is reached. If the device does not output the correct voltage a logic low will be send to the output. The input voltage is compared to the reference voltage usually implemented by using a voltage divider. The IC gives a simple method to monitor low voltages. Many times the output from the voltage supervisor can be sent to an FPGA.

Analog to digital converters (ADC) will take an actual analog signal and convert it to a digital signal where a device can process the signal, such as a FPGA or microcontroller. The FPGA or microcontroller is set or programmed by the engineer to translate the digital signals. One of the most important parameters of an ADC is choosing the resolution of its output. There is 2^N combinations, N being the bit amount. The higher the resolution the greater accuracy of the digital signal sent to the FPGA or microcontroller.

3.13 RoHS Compliant

There is a continuing struggle with tin whiskers. The tin whisker phenomenon has been a problem since the 1940s where electrical equipment made with cadmium, tin or aluminum grow what looks like metal whiskers. This is serious threat to the equipment because it can create shorts between parts that are near each other. However, it had been found that if lead is mixed with any of the common metals used, cadmium, tin, and aluminum that this phenomenon can be prevented. This saves the electronics from potential failure and thus compromising people's safety also. There is a grave problem with this issue. As lead can be harmful to humans and the environment, countries around the world are working towards enforcing laws that will prevent the manufacturing of electronics with lead. The argument remains, though, that lead is also preventing potential accidents if the electrical equipment fail. The European Union has already passed legislation called the Restriction of Hazardous Substances, or RoHs restrictions. These are restrictions on the use of hazardous materials. This legislation will affect companies around the world because they will either have to not sell to EU or find alternative materials to manufacture their product without having to compromise the risk of tin whisker. Also, not all industries are required to abide by the regulations including military. However, there lies the risk of companies swaying away completely from lead products which the military needs to operate electronics for many years. In this project it is necessary to find parts that are still made with lead.

3.14 Trade Studies

The high current signal requires more power and has less tolerance for ripple voltage than the low current signals. This signal can be treated differently in the design. Switching power supplies and pre-regulator modules (PRM) with voltage-

transformation module (VTM) handle high power signals. PRM/VTM take up physical space on the board.

The LTM4612 was compared and contrasted to the LTM 4606 and LTM8022. LTM 4606 and LTM 4612 were both considered for the switching power supply. They are rated for low EMI and low ripple voltage. However, the LTM 4612 and LTM 8022 met specifications for input and output voltage. EMI was strongest between 150MHz to 250 MHz for both the LTM 4606 and 4612. The screenshots capture the EMI results for both switching power supplies. The LTM 4612 exhibited the best results because there is minimal disturbance when compared to the reference screenshot. There is about a 5-db difference in noise, or the EMI noise in the LTM 4606 is about 3 times higher. The EMI was measured when power was off to use as a reference to compare the EMI when the part was on. The diagrams below, Figures 3.7.1-3.7.4 show the EMI present around the part when the part is on and off.

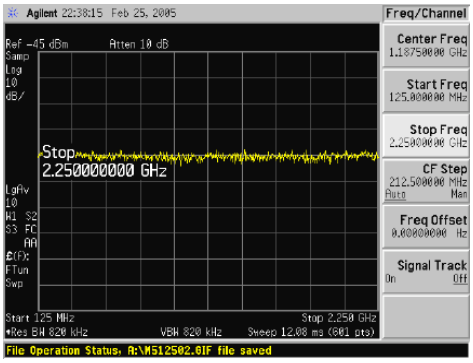


Figure 3.9.1 Reference.
No power applied to LTM 4612.

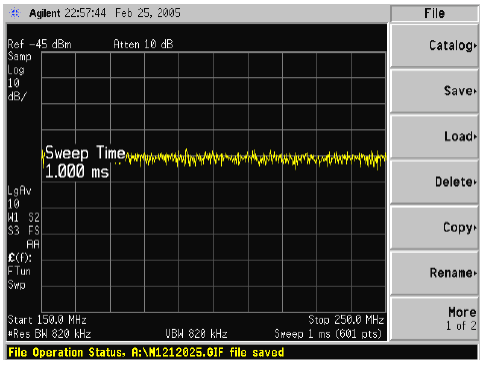


Figure 3.9.2
Power applied to LTM 4612.

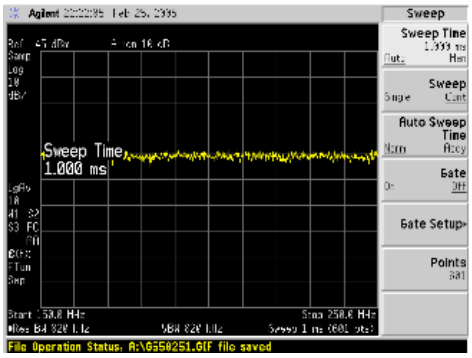


Figure 3.9.3 Reference.
No power applied to LTM 4606

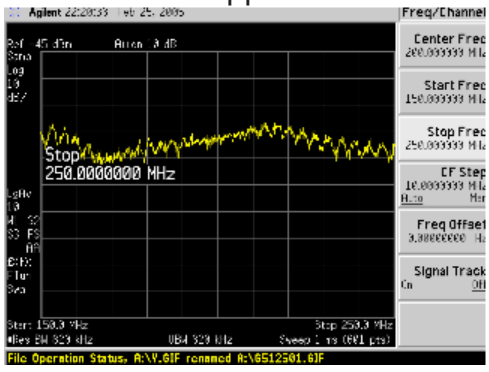


Figure 3.9.4
Power applied to LTM 4606.

Both the LTM 4612 and LTM 8022 have maximum junction temperature of 125 degrees celsius. The junction to ambient temperature for LTM 8022 is 24 degrees celsius per 1 watt. However, the junction to ambient temperature for the LTM 4612 is 14.9 degrees per 1 watt. LTM 4612 has a better temperature rating for the amount of output power generated. Since there is no airflow the

junction-to-ambient temperature is an imperative parameter to consider. The following figures display the estimated power loss for specific input and output voltages for the LTM 4612 and LTM 8022. The low current signal lines will not generate much power. Both have relatively low power output. Also, LTM 8022 could only handle a maximum of 1 amp. Therefore, junction-to-ambient power was a strong factor in choosing the LTM 4612 over the LTM 8022.

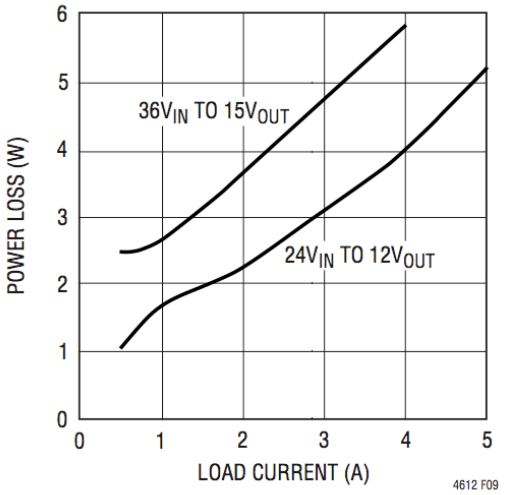


Figure 3.9.5 Linear Technology. LTM 4612 Datasheet. Power loss for 12Vout and 15Vout.

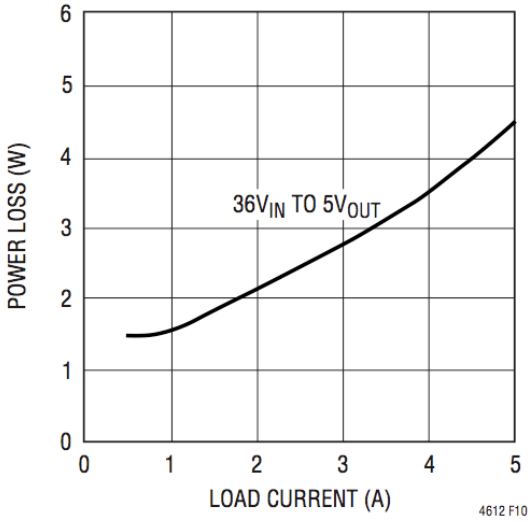


Figure 3.9.6. Linear Technology. LTM 4612 Datasheet. Power loss for 5Vout.

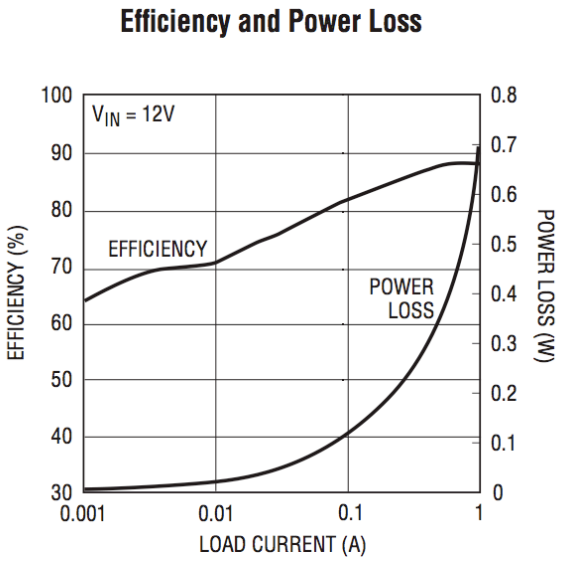


Figure 3.9.7 . Linear Technology. LTM 4612 Datasheet. Efficiency and Power Loss.

Many companies did not offer linear regulators that handle the temperature range called for by the customer, which is -55 degrees Celsius to +85 degrees Celsius. Another main issue was the output current. If the output current from the specifications was not met, then the potential of putting two linear regulators in parallel had to be considered. There are only specific parts that can be put in this configuration. The LTM1963 from Linear Technology was the only part that could be found to meet specifications.

The LT1964 has two packages from which to choose. The DD package is 0.21 mm^2 larger than the S5 package. In this case, the size is insignificant. However, the junction-to-ambient temperature (TJA) difference is impressive. The DD package has a TJA difference of 85 degrees Celsius. The DD package was a clear choice for the design to minimize heat dissipation as possible.

The purpose of the analog-to-digital converter (ADC) and the voltage supervisor were chosen for the same reason. The voltages of the power supply needed to be monitored, but they were analog signals that needed to be translated for the FPGA to read. The operation of the ADC is too complicated for this application. The voltage supervisor has a package that is much smaller than the ADC. For lack of space on the board it was important to find the smallest components possible. A disadvantage to the voltage supervisor is that it only will take low voltage inputs. However, in this application it was not an issue. ADC often are used in higher voltage applications. Then the final design did not need voltage supervisors because the final FPGA already has ADC integrated in the chip. This alleviates extra wire routing for the 4 voltage supervisors that would be monitoring the linear converters.

4 - Hardware Description

4.1 Available Resources

There will be 32 volts available for the system. This will be the main power to the system. There will also be 3.3 volts available. The FPGA can be biased with this voltage. Therefore, there is no need to build anything to generate these voltages necessary for the power supply and timing control unit.

4.2 Heat dissipation capabilities

The switching power supplies and linear regulators will dissipate enough power that need to be considered and not exceed the allowable junction temperature. The output voltage from the SWPS will affect the input to the LDO. To optimize performance the following calculations are considered. The power dissipation from LT1963 can be calculated by [Iout*(Vin-Vout)] + (Ignd)Vin. Ignd can be found from the graph below, Figure 4.2.1.

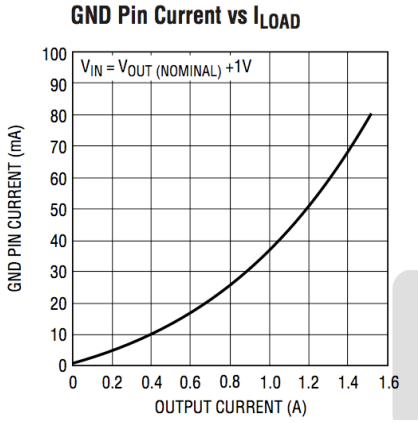


Figure 4.2.1 Linear Technology. LT1963 Datasheet.

The SWPS dissipated power is found by the following method. First, calculate Power in = Power out / efficiency. Then Power dissipated = Power in - Power out. Efficiency can be approximated from the graph below Figure 4.2.2.

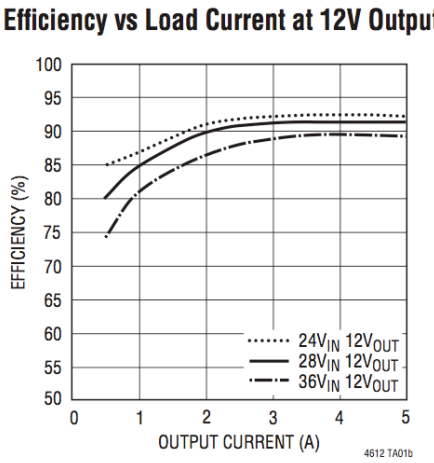


Figure 4.2.2 Linear Technology. LT4612 Datasheet.

For all scenarios, the maximum junction temperature, Tjamax, equals 125 degrees celsius for the SWPS. Tjamax = 150 degrees celsius for the LDO. Maximum ambient temperature, Tamax, equals 59 degrees celsius.
First, the 6 volt line is considered. In order to be sure the junction temperature is below the maximum allowable temperature of 150 degrees celsius for the LT4612 SWPS, the ambient temperature is a constant of 59 degrees celsius. The design will set the output voltage of the SWPS at 8 volts. This makes the power dissipation at 4.2 watts and does not exceed the junction temperature. Since the input to the LDO is 8 volts, the power dissipation is 2.3 watts. This keeps the junction temperature of the LDO below 150 degrees celsius also. The following diagrams display the LDO's input voltage linear relationship with power dissipation, the LDO's linear relationship between power dissipation and junction temperature, the SWPS's linear relationship between output voltage and power dissipation, and SWPS's linear relationship between power dissipation and junction temperature.

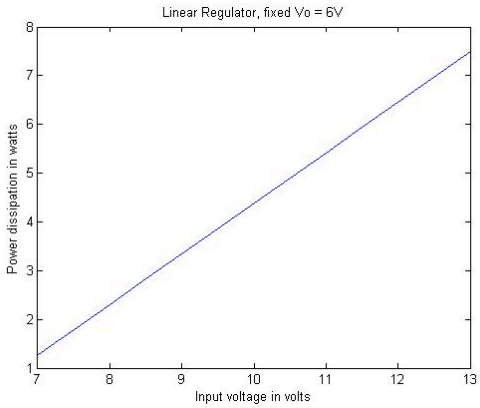


Figure 4.2.3

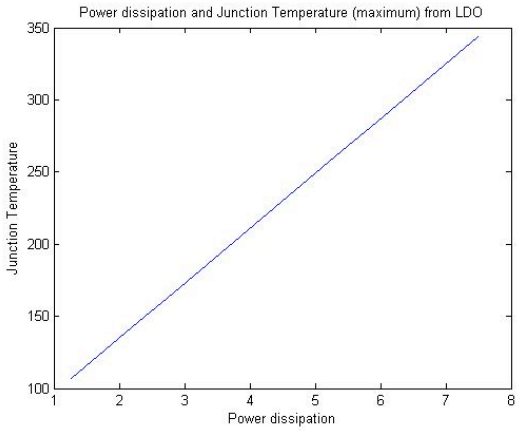
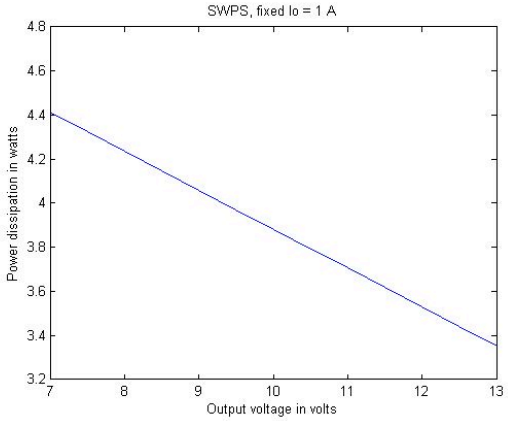


Figure 4.2.4

Linear Regulator Power Dissipation Linear Regulator Power Diss. & Temp.



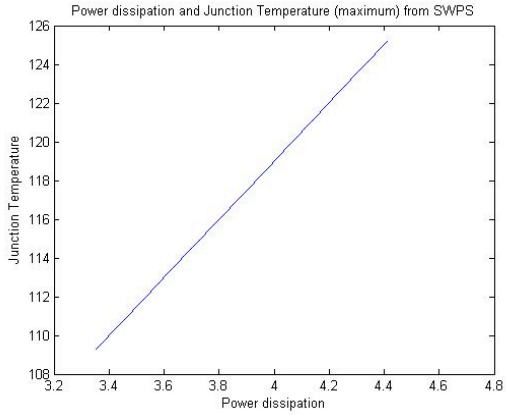
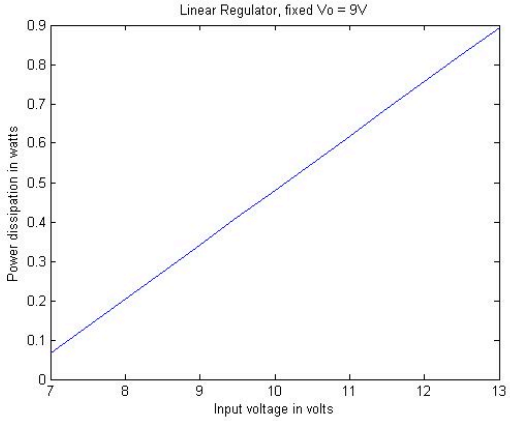


Figure 4.2.5
SWPS Power Dissipation

Figure 4.2.6
SWPS Power Diss. & Temp.

The next is the 9 volt line thermal considerations.



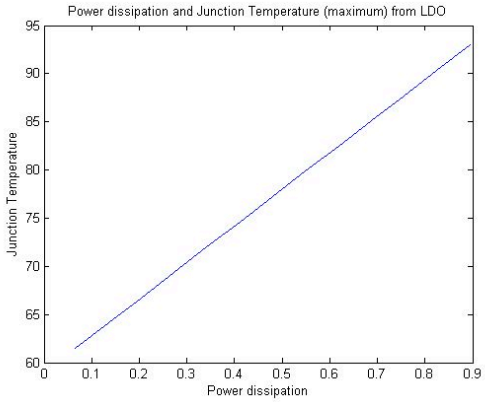


Figure 4.2.7
Linear Regulator Power Dissipation

Figure 4.2.8
Linear Regulator Power Diss. & Temp.

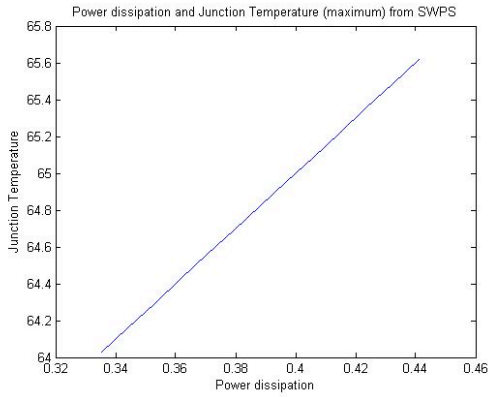


Figure 4.2.9
SWPS Power Dissipation

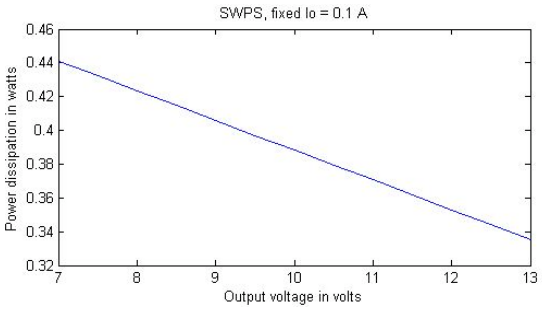


Figure 4.2.10
SWPS Power Diss. & Temp.

4.3 Power Architecture

4.3.1 Linear Voltage Regulator and DC-DC converter/Switching Power

The purpose of the power supply is to generate multiple voltages that the transceiver must receive for operation. The voltages must be turned on in sequential order and then shutdown in the specific reverse order that they were turned on. The system provides the power supply with 32 volts. There is one high current signal and three remaining low current signals that are generated. The 32 volts is fed to three switching power supplies. A significant challenge in designing this circuit is heat dissipation. There is no airflow in the system. Therefore, heat sinks are not practical for the design. Instead, the design will have to be based upon parts that dissipate low heat and a design that does not create high power. 1 to 2 watts is an acceptable range for the part. Stepping down the voltage from 32 volts down to the required voltages creates high enough power that will generate unwanted heat in the system. The switching power supply will step down the voltage almost to the desired voltage. The switching power supply dissipates low enough heat for requirements. However, it creates undesirable EMI levels and voltage ripple as per the specifications. A linear regulator will give a cleaner output signal. The linear regulator will be used as a filter. This is enough for the tolerances of ripple voltage at 1mV. The high current signal (6VDC) must be an output of +6 volts at 11 amps. The figure below, Figure 4.3.1.1, demonstrates the high power signal.

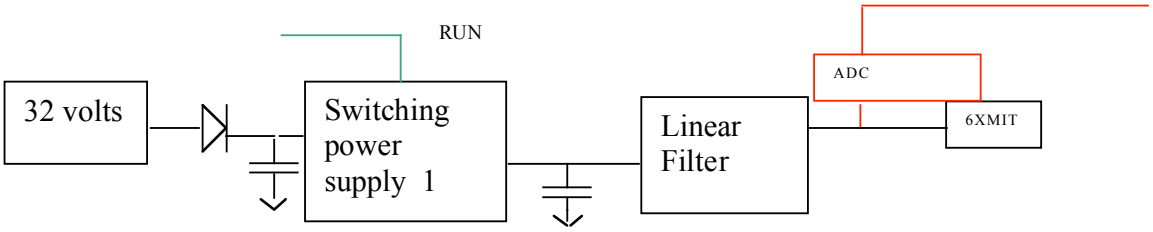


Figure 4.3.1.1 High Power Line

It is more imperative that the output from the lower power lines have even cleaner signal than the high power line. The lower current signals have tighter tolerances, so the design needs to clean the signal more. The linear regulators can still handle the tolerances given by the specifications. The low current signals are +9 volts at 100 milliamps with 100 microvolts, +6 volts at 1 A with 100 microvolts, and -4 volts at 250 milliamps at 100 microvolts. Since the linear regulator has lower levels of EMI and ripple voltage, it cannot be replaced by the switching power supply, but the linear regulator creates too much heat because the step-down voltage delta is high for this part. Dropping 32 volts down to the specified low current voltages will create too much power, and thus too much heat for the system. Both parts will have to be used in the design. Capacitors in the design of the power supply give a square signal. Without the capacitor design an undesired ramp function will be generated instead, leading into the linear regulator. The linear regulator needs a relative consistent voltage at an instant. Without the capacitors the linear regulator receives a ramping voltage. The capacitors hold the voltage until the switch is turned on and the regulator gets the consistent voltage at once. The LTM 4612 experimentally outputs about 11mV. Then in order to reach tight tolerances for ripple voltage, the ripple attenuator will create an even cleaner signal. Refer to Figure 4.3.1.2 for the block diagram of the low power signal.

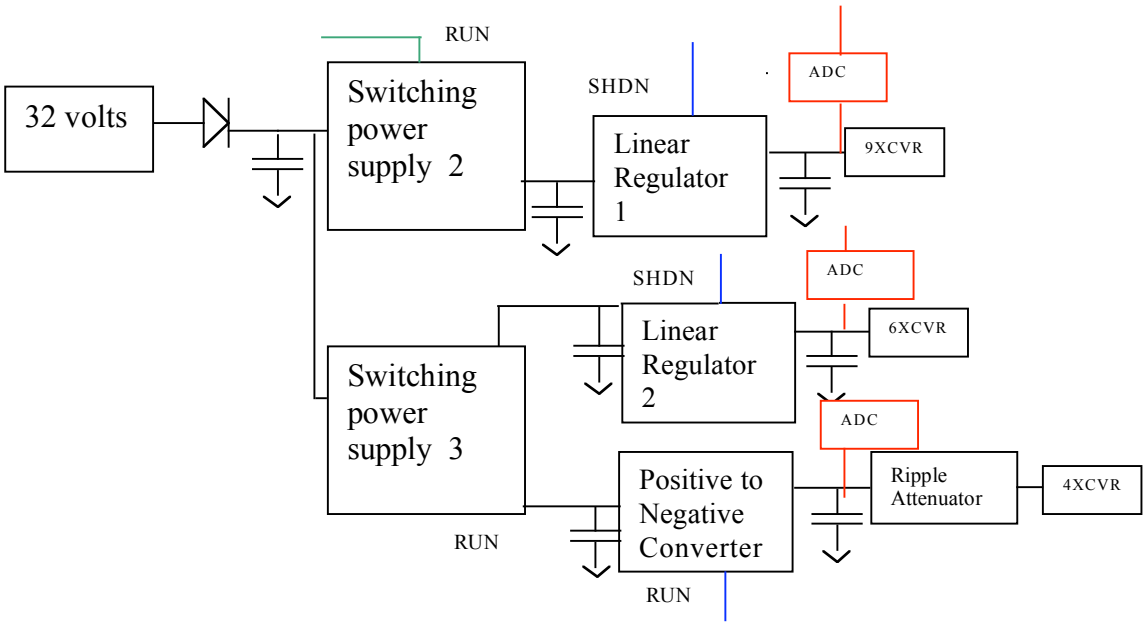


Figure 4.3.1.2 Low Power Lines

4.3.2 EMI

4.3.2.1 Noise Simulations

Linear Technology provides access to circuit simulator software to simulate their parts. Since the design will use three Linear Technology parts, it was convenient to use the simulation software to obtain specific results to the design intended. The first circuit to be simulated is the 6 volt line. The noise generation simulated in this circuit will also reflect the 9 volt line. The LTM4612 switching power supply exhibits noise at its output in the simulations as expected by information in the data sheet. The output capacitors will filter the noise to an extent. The following diagram, Figure 4.3.2.1.1, is the circuit used for the LTM simulations. C1 is the output capacitor that is changed to observe changes in the output noise.

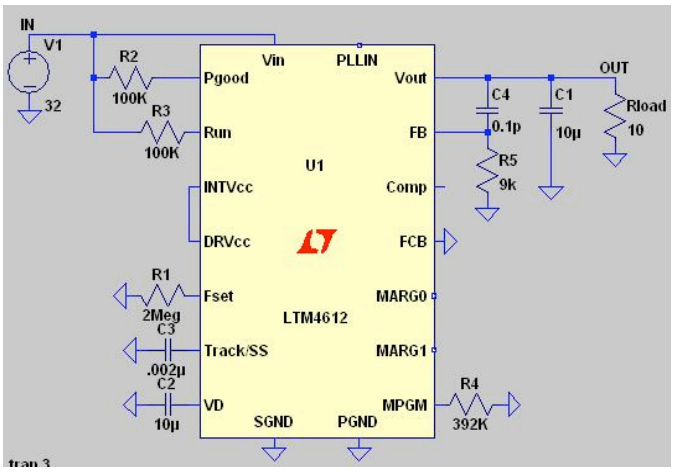


Figure 4.3.2.1.1
LT4612 uses 10uF output capacitor. Recommended circuit by Linear Technology

The following diagram, Figure 4.3.2.2, displays the simulated results when 10uF output capacitor is used.

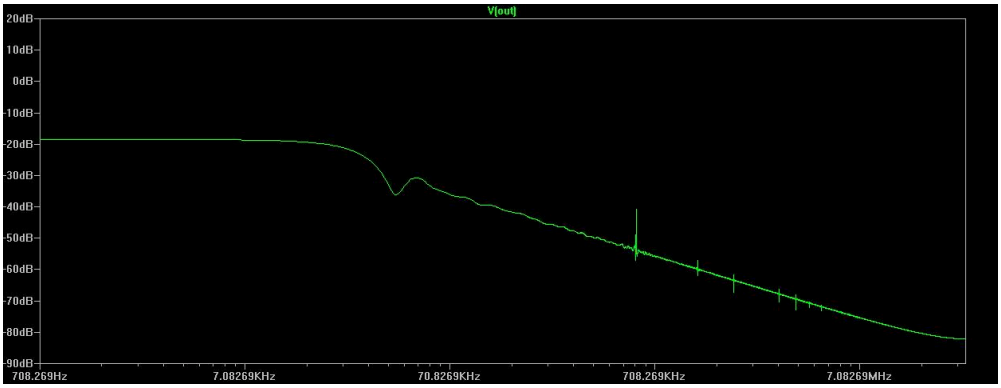


Figure 4.3.2.1.2
Noise vs. Frequency at output of LTM4612 uses output capacitor of 10uF.

The output signal of the LTM4612 has a cleaner signal when the value of the capacitance is higher. The following diagram, Figure 4.3.2.1.3, is the simulated result when the output capacitance is 80uF.

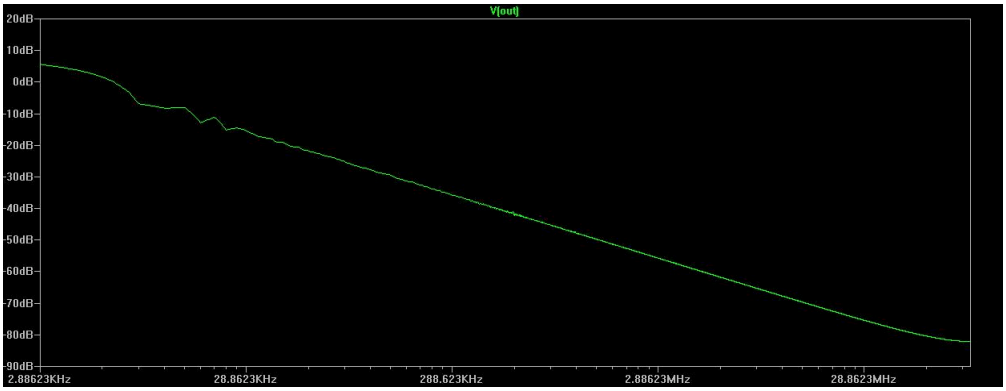


Figure 4.3.21.3
Noise vs. Frequency at output of LTM4612 uses output capacitor of 80uF.

The two following diagrams show even cleaner signals as the capacitance is raised higher. The diagram, Figure 4.3.2.1.4, shows the output capacitance for 100uF.

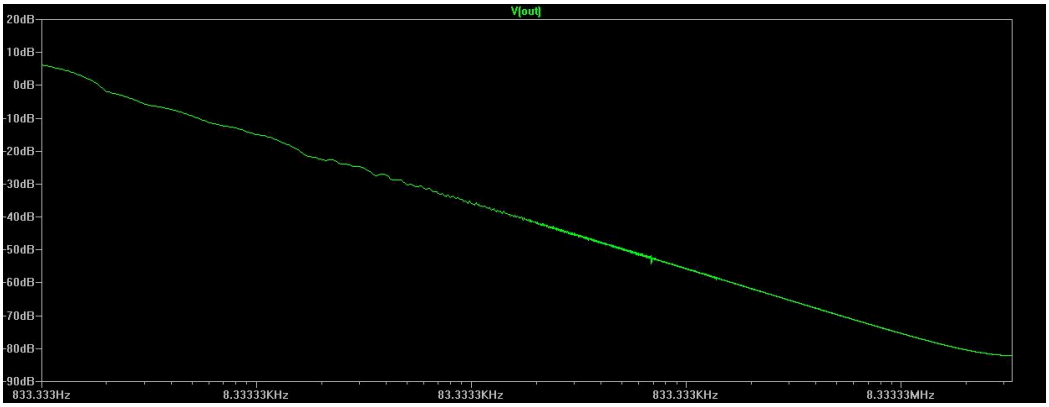


Figure 4.3.2.1.4
Noise vs. Frequency at output of LTM4612 uses output capacitor of 100uF.

Finally the following diagram, Figure 4.3.2.1.5, uses 200uF for the output capacitor. This shows the cleanest signal.

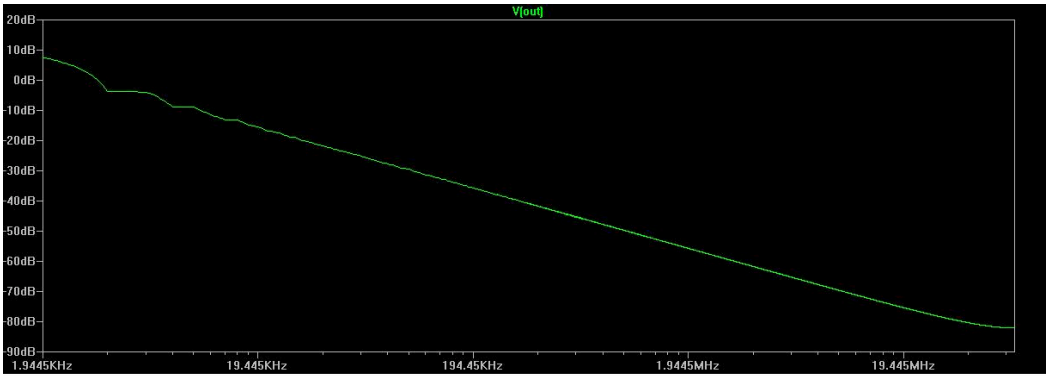


Figure 4.2.6.1.5
Noise vs. Frequency at output of LTM4612 uses output capacitor of 200uF.

The LT1963 positive linear used for the 9 volt line and the 6 volt, low power line exhibits a clean output signal. The linear regulator is a good filter, which is shown in the simulated results. The output capacitor does not greatly affect the output signal as far as noise. The following diagram, Figure 4.3.2.1.6, is the LT1963 circuit used for the simulated results.

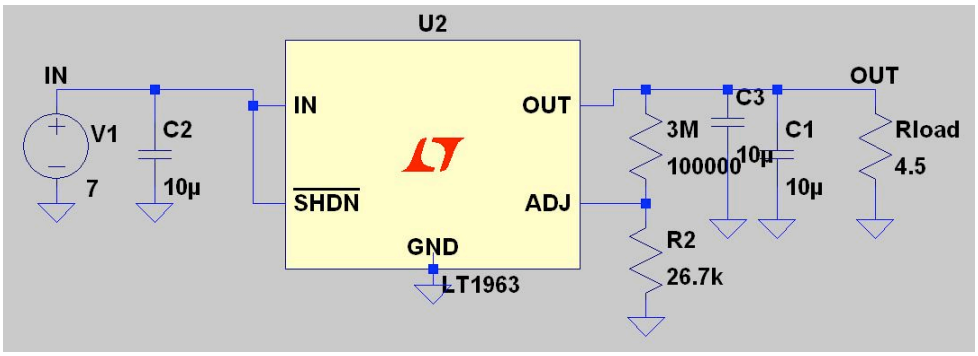


Figure 4.3.2.1.6 Linear Regulator
Recommended circuit by Linear Technology

The noise at a wide range of frequencies is low, especially compared to the LTM4612. This will provide a clean voltage that is required in the specifications. The following diagram, Figure 4.3.2.1.7, exhibits low noise across a a frequency spectrum.

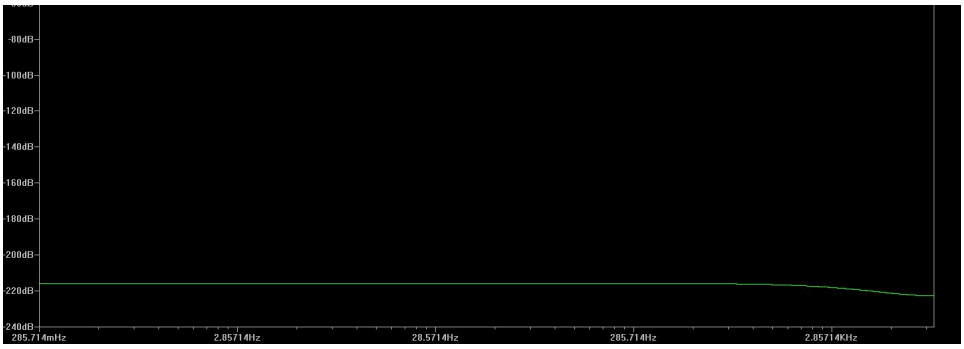


Figure 4.3.2.1.7
Noise vs. Frequency at output of LT1963.

The LTC3704 is very noisy. The circuit was set for the output current and output voltage to meet specifications. The following circuit, Figure 4.3.2.1.8, was used for the noise simulations.

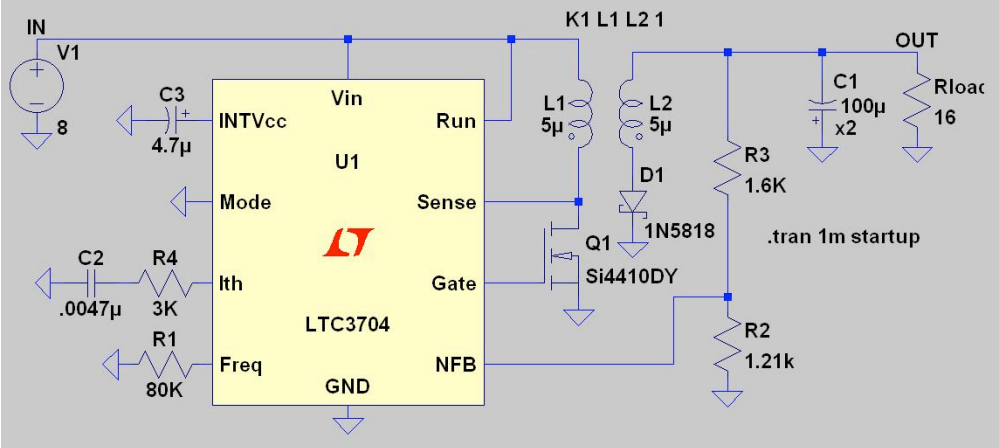


Figure 4.3.2.1.8
Negative to positive converter
Recommended circuit by Linear Technology

Over the frequency spectrum, the output of the LTC3704 is noisy as the simulation proves. The following diagram, Figure 4.3.2.1.9, displays the noise over a wide frequency spectrum.

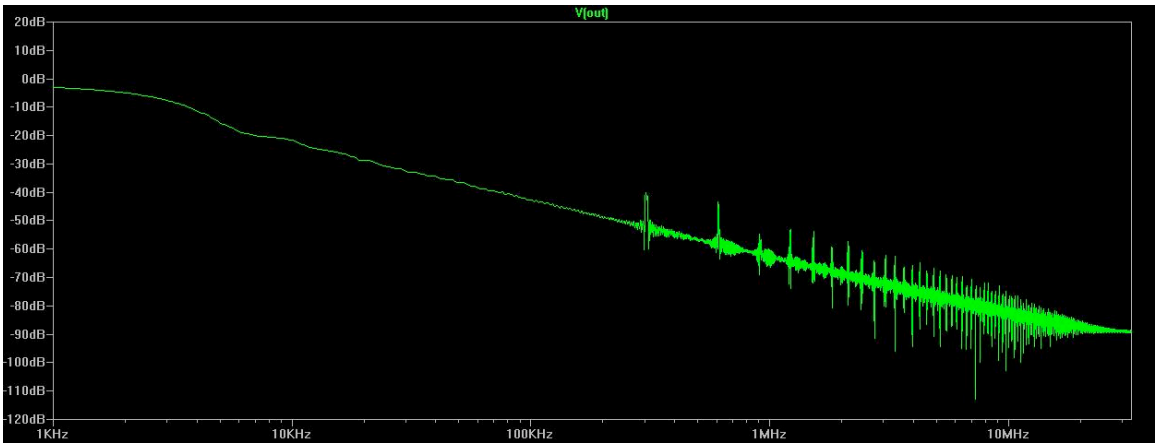


Figure 4.3.2.1.9
Noise of Negative to positive converter

4.3.2.2 - Voltage, Current, and Time Response Simulation

The simulations for the LT4612 reflect the values from the schematic (refer to Figure 4.3.2.1.1). The output voltage response did not change with the change of values of the output capacitors. Vin is 32 volts. Vout is 6 volts. The following diagram, Figure 4.3.2.2.1, displays the simulated results of input voltage, output voltage, and output current.

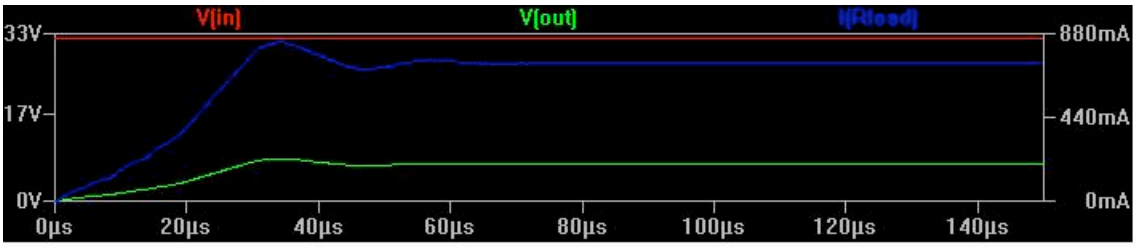


Figure 4.3.2.2.1
Voltage vs. Time and Current vs. Time

The output ripple voltage is about 30mV according to the simulations. This does not meet the specified ripple voltage of 100uV. This is another reason to use a filter. The following diagram, Figure 4.3.2.2.2, displays the output ripple voltage.

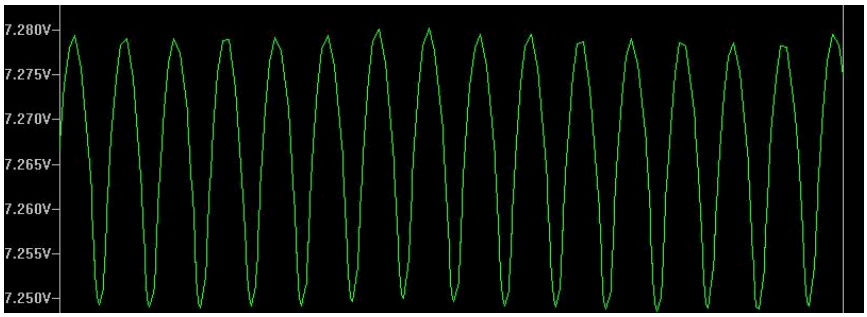


Figure 4.3.2.2.2
Output ripple voltage from LT4612.

The following diagram indicates that a 7-volt input signal and 6 volt output signal can be done with low noise from the LT1963. Reaction time between the part turning on and the output signal is instantaneous according to the simulated results. Also, there is no obvious ripple voltage from the resolution of the voltage plot unlike the LTM4612. The following diagram, Figure 4.3.2.2.3, shows the input voltage, output voltage, and output current.

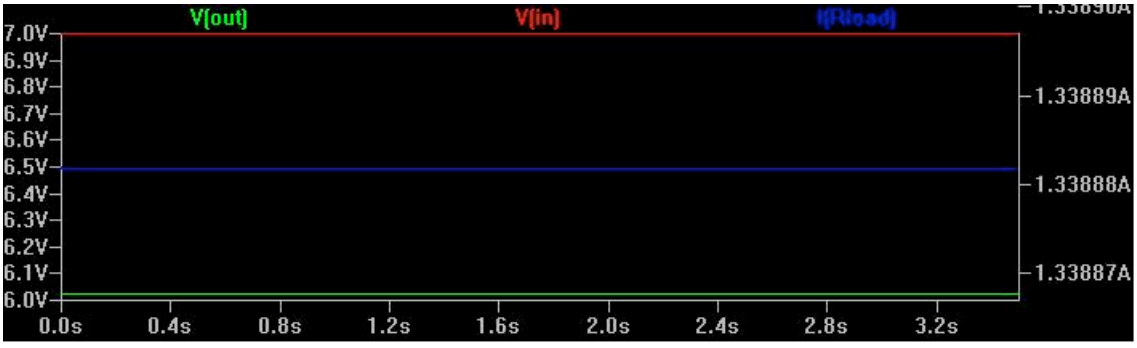


Figure 4.3.2.2.3
Voltage vs. Time and Current vs. Time for LT1963

From the simulations, there will be no ripple voltage for any scenarios of input voltage and output voltage.

The LTC3704 circuit mentioned above (refer to Figure 4.3.2.1.8), had Vout = -4 and Iout = 250mA as called by the specifications. The following diagram, Figure 4.3.2.2.4, shows the simulation results.

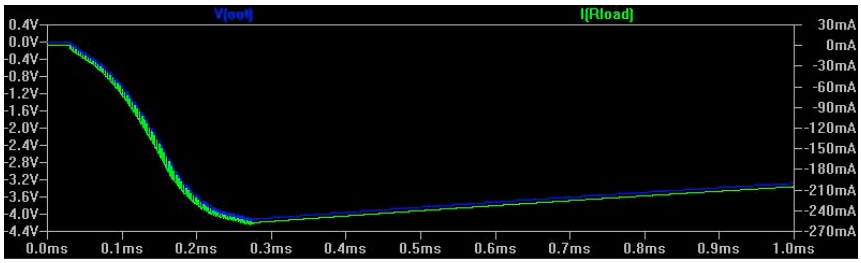


Figure 4.3.2.2.4
Voltage vs. Time and Current vs Time for LTC3704

4.3.3 Power Sequencing

In order to monitor all the voltages, the output of each linear regulator for both high power and lower power signals will be sent to the FPGA. The signals will be sent to the integrated ADC in the FPGA. Power sequencing will have to happen in the following order. There will be 3.3 volts available from another circuit board not considered in this design. The 3.3 volts will be used to power the FPGA. FPGA must turn on first, separate from the power architecture since the FPGA is controlling the power on sequence. The FPGA must control the power sequence because the FPGA is programmed to do a specific task. If the power signals are controlled otherwise by the system there is no feedback to regulate the signals properly. Once the FPGA is on, the power sequencing commences. The power signal must be turned on in sequential order starting with the -4 volt line, the +6 volt line, +9 volt line, and lastly the +6 high power signal line. The switching power supply needs to be enabled before the linear regulator for each signal line. The FPGA sends a signal to the RUN pin of the switching power supply to enable the chip. The PGOOD pin from the switching power supply will send a signal to the FPGA. PGOOD pin sends either a high or low signal depending on if the correct output voltage was sent out of the chip. The following diagram, Figure 4.3.31, demonstrates the inputs and outputs of the FPGA to the switching power supply.

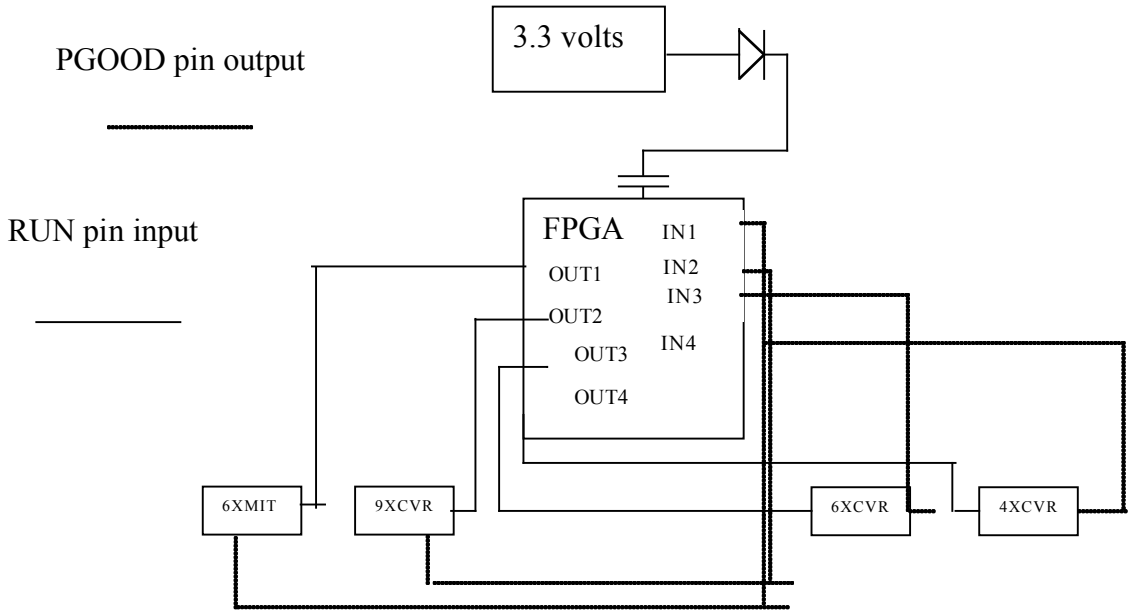


Figure 4.3.3.1
FPGA I/O with switching power supply

The positive to negative converter is triggered by the RUN pin also. However, the output of the converter must be fed to the integrated ADC in the FPGA in order for the FPGA to read a high or a low signal. The diagram below, Figure 4.3.3.2, demonstrates the communication between the converter and the FPGA.

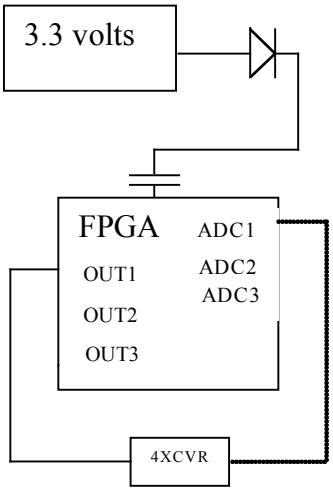


Figure 4.3.3.2
FPGA I/O with positive to negative converter

If the FPGA receives a correct voltage reading, it will trigger the linear converter next by pulling the SHDN pin high. The output of the linear converter is sent to the input of the FPGA. The following diagram, Figure 4.3.3.3, demonstrates the

inputs and outputs of the FPGA only considering monitoring voltages from the linear regulators.

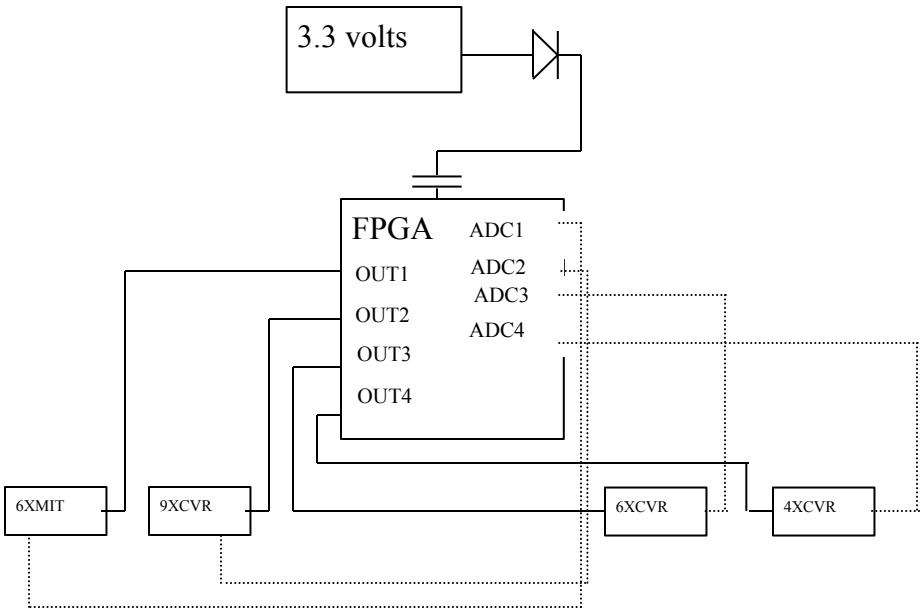


Figure 4.3.3.3
FPGA I/O for linear regulators.

The power sequencing is now discussed in more detail. Once power sequencing commences the switching power supply 3 and positive to negative converter will be enabled first to output -4V. The converter is part number LTC3704 from Linear Technology. The output from the converter will be fed to the integrated ADC in the FPGA. Since the signal is high the FPGA then will enable linear regulator 2. The positive linear regulator is an LT1963A also from Linear Technology. The output is fed again to another integrated ADC in the FPGA. Switching power supply 2 is enabled next which is the +9V line. The same process applies to the +9V line as the +6V line. The signal from the power supply, pin PGOOD is sent to the FPGA. Since the signal is high, the FPGA will enable linear regulator 1 to get the low power of +6V output. The output signal is sent to the integrated ADC in the FPGA which will verify if it is the correct voltage. Refer to the following diagram, Figure 4.3.3.4, for the block diagram that displays the parts used in the power sequence.

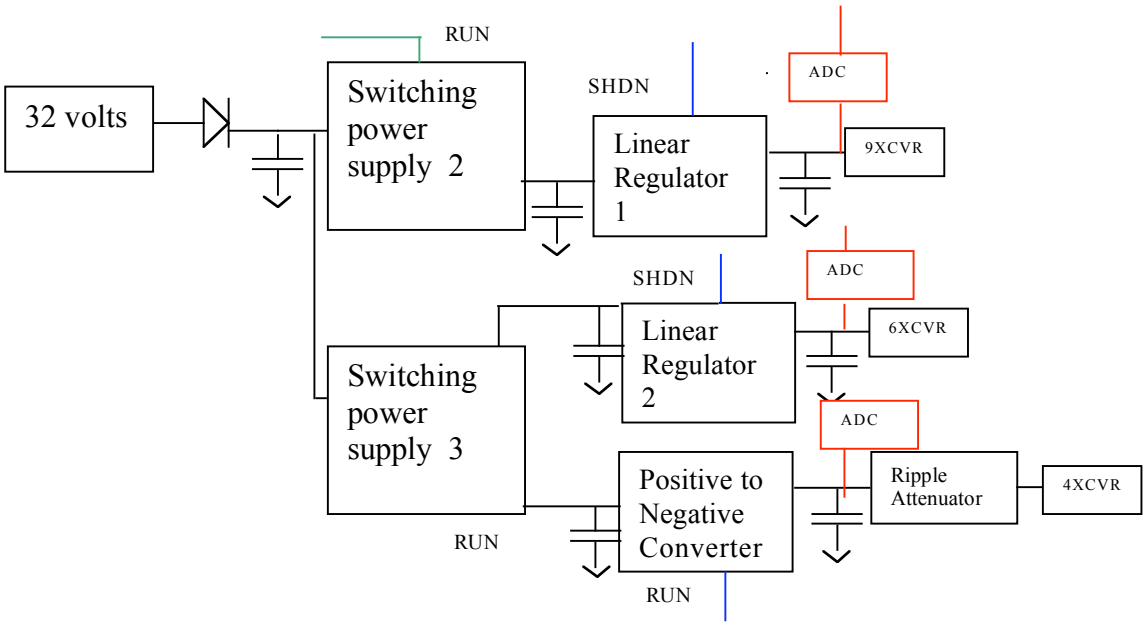


Figure 4.3.3.4
Parts used in Low Power Sequence

Next the switching power supply 1 is enabled and if there is a correct voltage, the FPGA will enable the linear regulator. If the voltage is correct, then power down sequence can commence. The diagram below, Figure 4.3.3.5, displays the high power sequence.

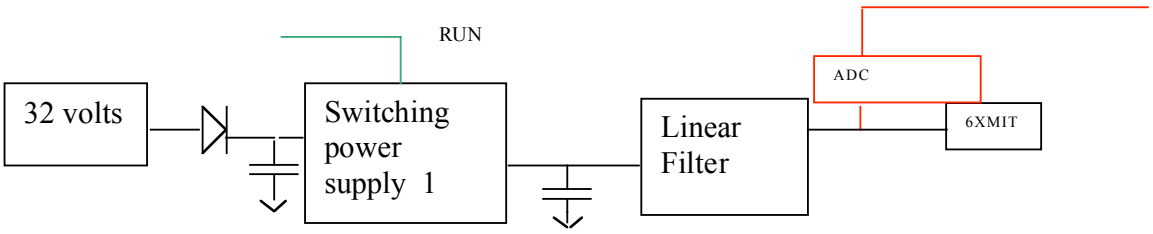


Figure 4.3.3.5
Parts used in High Power Sequence

The FPGA will disable the linear regulator by pulling the pin low. The FPGA will detect there is an active low output voltage from the ADC. Then the FPGA can continue to disable the switching power supply 1. The FPGA will continue to shut off the low power lines. This process will continue in the exact opposite order of power up sequence . Capacitor must be placed where 32 volts enters the circuit board. This will allow enough reserve power if 32 volts were to fail. The high power and low power signals must be turned off in the proper order. With the fail-safe capacitor this will allow enough time for the power supply to shut off properly. The diode is placed before this capacitor to ensure that current is not

drawn back out of the system, and thus losing the voltage that was to go to the power supply as it shuts off.

4.4 Timing and Control System Architecture

4.4.1 Overview Selection Process

There are two parts to the timing and control architecture. The heart of which will be some type of programmable device; the other is the peripheral sensing equipment (Current Sensors, A/D Convertors etc...). The type of programmable device needed for this project is a programmable logic device. The choices available to us including a chip all the way to an FPGA varied, but project limitations directed us to consider a microcontroller or Field Programmable gate arrays (FPGA). Application-specific Integrated Circuits (ASIC) were not an option since we would need the ability to change the configurations down the line, as the project progressed. A Complex Programmable Logic Device (CPLD) has the resources necessary to accomplish what we need but is more limited in function than an FPGA. A Microcontroller is single-chip computer designed specifically for either device or communication control. The typical one is comprised of a microprocessor, its memory, and the input/output ports. The microcontroller was a valid choice for our needs but since our goal was to increase scalability and modernize the design of the Timing and Control System, an FPGA was a popular choice.

FPGA's are programmable logic devices that are typically used for prototyping an ASIC. While FPGAs are typically a bit slower than their ASIC counterparts, the development and manufacturing costs of these devices are much less than those of an ASIC implementation. FPGAs are normally programmed in either Verilog or VHDL depending on the company or user preference. These devices require the use of a design compiler that will take coded or CAD circuitry and convert it to a mask that the FPGA will implement.

We evaluated the products available from three main companies that produce FPGAs: Xilinx, Altera and Actel. While there are many more companies that produce FPGA's these companies tend to be the industry leaders. Since longevity and support of parts is a consideration in the project, going with a company that has a rich history in the field was an important factor in the decision-making process. The following are FPGA limiting factors:

- low operating temperatures
- onboard Non Volatile Memory(NVM)
- timing signal accuracy of 5ns (200 MHZ)
- low power usage as required for the entire assembly
- low profile quad flatpack design
- Footprint should be minimal
- Temperature

Due to its environment of operating inside of a missile that will be flying at high altitudes we were required to select an FPGA that could handle an operating temperature as low as -40 degrees Celsius.

FPGA Requirements:

- At least 200,000 system gates
- At least 4000 Logic Cells
- 28 KB of distributed RAM
- 288 KB of block RAM
- 1 DCM
- Sufficient I/O ports
- As much integration as possible
- Small foorprint
- Industrial/Military Temperature Grade
- height of <1-2 mm

As most companies had comparable products that would meet our gate., I/O and memory requirements; the FPGA height was going to be our deciding factor. If available, we need a chip that could integrate as many of the parts all on one piece of silicon the more space saving we would achieve. These parts that have mixed digital and analog signals are known as Mixed-Signal FPGA"s. Currently the only company that makes a Mixed-Signal FPGA is Actel. The Actel Fusion family of FPGA's met every specification and also included ADC (Analog to Digital Convertors) integrated directly on the chip. As seen in Figure 4.3.1.1 below the AFS250 FPGA had the requirements we needed. While the AFS600 and AFS1500 also met our requirements; the gate and memory requirements we received already had the necessary specifications to grow with our project, so these FPGA's would limit our ability to keep the IC as small as possible.

Fusion Devices		AFS090	AFS250	AFS600	AFS1500
ARM-Enabled Fusion Devices	CoreMP7 [1]			M7AFS600	
	Cortex-M1 [2]		M1AFS250	M1AFS600	M1AFS1500
General Information	System Gates	90,000	250,000	600,000	1,500,000
	Tiles (D-flip-flops)	2,304	6,144	13,824	38,400
	Secure (AES) ISP	Yes	Yes	Yes	Yes
	PLLs	1	1	2	2
	Globals	18	18	18	18
Memory	Flash Memory Blocks (2 Mbits)	1	1	2	4
	Total Flash Memory Bits	2 M	2 M	4 M	8 M
	FlashROM Bits	1 k	1 k	1 k	1 k
	RAM Blocks (4,608 bits)	6	8	24	60
	RAM kbits	27	36	108	270
Analog and I/Os	Analog Quads	5	6	10	10
	Analog Input Channels	15	18	30	30
	Gate Driver Outputs	5	6	10	10
	I/O Banks (+ JTAG)	4	4	5	5
	Maximum Digital I/Os	75	114	172	252
	Analog I/Os	20	24	40	40

Notes:
1. *Refer to the CoreMP7 datasheet for more information.*
2. *Refer to the Cortex-M1 product brief for more information.*

Figure 4.4.1.1 Fusion Devices (Permission pending from Actel)

There are were specific FPGAs that would meet size requirements. The Fusion family of FPGA's come in various sizes. Since minimum board space was our biggest priority we went with the AFS250-QNG180I. This chip has all the specifications as shown in Figure 4.3.1.1 above and also the more detailed specifications that come from the QNG180I. The Q is the quad flat pack design giving us the desired height of 0.75mm (see figure 4.3.1.2 below). The "N" is for no-lead giving us ROHS compliance. the 180 is for 180 pin pack, and the I gives us industrial grade temperatures.

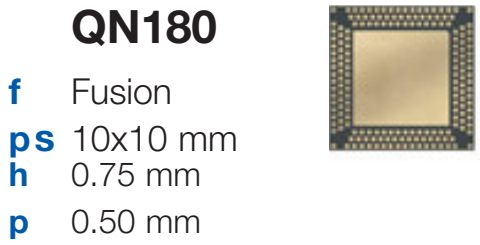


Figure 4.4.1.2 Dimensions of FPGA **(Permission pending from Actel)**

4.4.2 Power

This device because it is flash based exhibits power characteristics similar to an ASIC. The Fusion device has many admirable power characteristics which are the following:

- No power-on current surge and no high current transition, both of which occur on many FPGAs.
- Low dynamic power consumption
- Single 3.3 V Power Supply with On-Chip 1.5 V regulator, thus only 3.3V from external system is needed
- Sleep and Standby Low Power Modes

Standby Mode/Sleep Mode

The addition of the RTC (Real Time Counter) system (Figure 4.3.2.1) enables the Fusion FPGA to support both standby and sleep modes, reducing power consumption. The RTC system comprises six blocks that work together to provide this increased functionality and reduced power consumption.

- RTC
- Crystal oscillator
- VCC33UP detector
- Voltage regulator initialization
- Voltage regulator logic
- 1.5 V voltage regulator

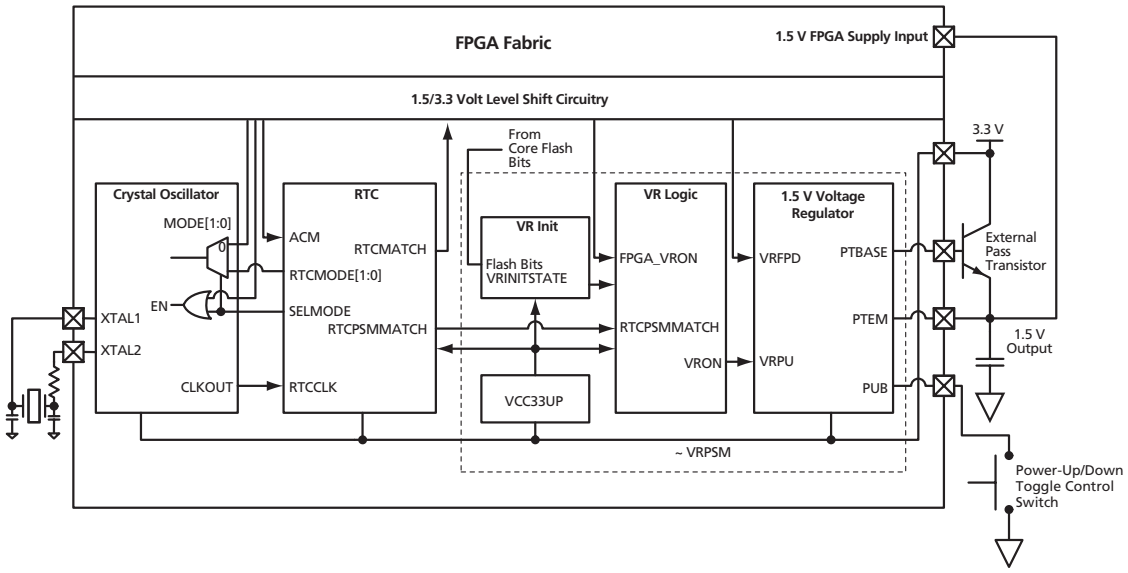


Figure 4.4.2.1 FPGA Fabric (Permission pending from Actel)

4.4.3 Embedded Memory

Fusion devices include four types of embedded memory:
- Flash block
- Non-Volatile FlashROM

- SRAM
- FIFO.

Flash Block Memory

Figure 4.3.3.1 shows a block diagram of the Flash Block Memory. The logic consists of the following sub-blocks:

- The Flash Array Contains all stored data, 64 sectors each containing 33 pages of data.
- Page Buffer is a a page-wide volatile register containing 8 blocks of data and an AUX block.
- Block Buffer contains the contents of the last block accessed. A block contains 128 data bits.
- ECC Logic The FB stores error correction information with each block to perform single-bit error correction and double-bit error detection on all data blocks.

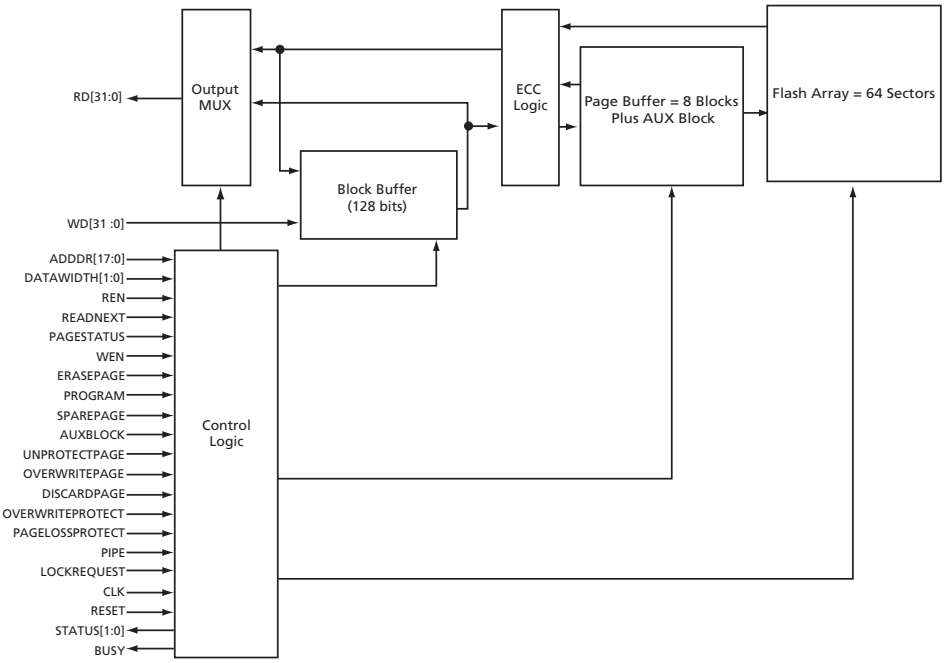


Figure 4.4.3.1 Control Logic Block Diagram
(Permission pending from Actel)

Specifications:

- Each block operates independently with a dedicated flash controller and interface.
- One to four flash blocks, each 2 Mbits in size
- Fast access times (60 ns random access and 10 ns access in Read-Ahead mode)

- Configurable 8-, 16-, or 32-bit data-path, enabling high-speed operation without wait states.
- Each memory block is organized in pages and sectors. Each page has 128 bytes, with 33 pages comprising one sector and 64 sectors per block. The flash block can support multiple partitions.

Methods of external access to the flash memory blocks.

1. A serial interface using the built-in JTAG-compliant port, allows for system programmability during user, monitor and test modes. This interface supports programming of an AES-encrypted stream. Secure data can be passed through the JTAG interface(See Figure 4.3.3.2 below), decrypted, and then programmed in the flash block.

2. FPGA logic can access flash memory through the parallel interface. The flash memory parallel interface provides configurable byte-wide (×8), word-wide (×16), or dual-word-wide (×32) data port options. Through the programmable flash parallel interface, the on-chip and off-chip memories can be cascaded for wider or deeper configurations.

The flash memory has built-in security. The user can configure either the entire flash block or the small blocks to prevent unintentional or intrusive attempts to change or destroy the storage contents. Each on-chip flash memory block has a dedicated controller, enabling each block to operate independently.

User Nonvolatile FlashROM

The Fusion device we are using has 1 kbit of user-accessible, nonvolatile FlashROM on the chip. The FlashROM is written using the standard JTAG programming interface (see Figure 4.3.3.2)
This memory has the following features:

- Pages can be individually programmed (erased and written).
- On-chip AES decryption can be used to load data such as security keys.
- The FlashROM can be programmed (erased and written) via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing.

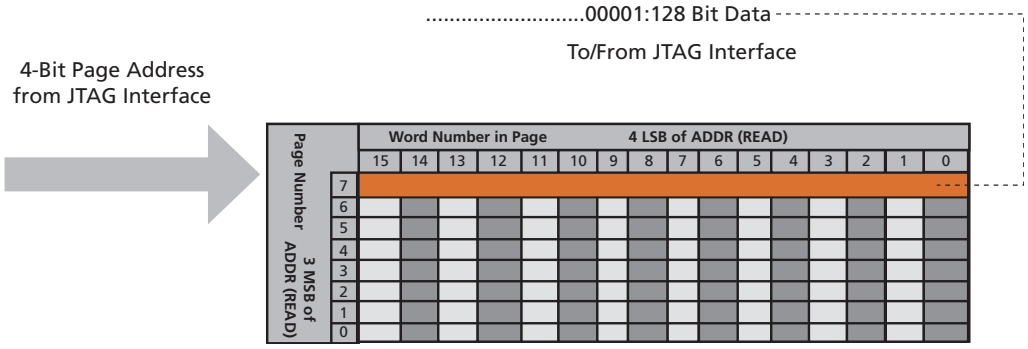


Figure 4.4.3.2 Address of JTAG Interface (Permission Pending from ACTEL)

SRAM and FIFO

Fusion devices have embedded SRAM blocks along the north and south sides of the device. Each variable-aspect-ratio SRAM block is 4,608 bits in size. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. The SRAM blocks can be initialized from the flash memory blocks or via the device JTAG port (ROM emulation mode), using the UJTAG macro. In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal EMPTY and FULL flags. The embedded FIFO control unit contains the counters necessary for the generation of the read and write address pointers. The SRAM/FIFO blocks can be cascaded to create larger configurations.

SRAM Features

RAM4K9 Macro

The RAM4K9 is the dual-port configuration of the RAM block (see Figure 4.3.3.3 **)**. The RAM block can be configured to the following aspect ratios: 4,096x1, 2,048x2, 1,024x4, and 512x9. The RAM4K9 is fully synchronous and has the following features:

- Two ports that allow fully independent reads and writes at different frequencies
- Selectable pipelined or nonpipelined read
- Active low block enables for each port
- Toggle control between read and write mode for each port
- Active low asynchronous reset
- Pass-through write data or hold existing data on output. In pass-though mode, the data written to the write port will immediately appear on the read port.

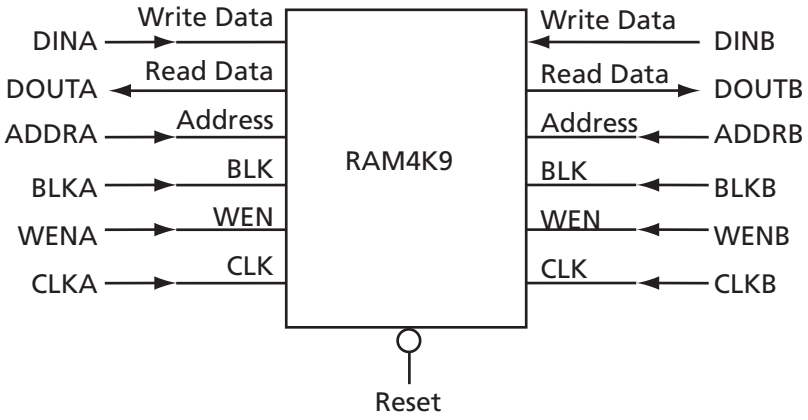


Figure 4.4.3.3 SRAM Ports (Permission pending from Actel)

FIFO (First in First Out)

Figure 4.4.3.4 shows the FIFO4KX18 macro. It is created by merging the RAM block with dedicated FIFO logic. Since the FIFO logic can only be used in conjunction with the memory block, there is no separate FIFO controller macro. As with the RAM blocks, the FIFO4KX18 nomenclature does not refer to a possible aspect ratio, but rather to the deepest possible data depth and the widest possible data width. The FIFO4KX18 can be configured into the following aspect ratios:

- 4,096x1
- 2,048x2
- 1,024x4
- 512x9
- 256x18

In addition to being, the FIFO4KX18 also has the following features:

- Four FIFO flags: Empty, Full, Almost-Empty, and Almost-Full
- EMPTY flag is synchronized to the read clock
- FULL flag is synchronized to the write clock Both Almost-Empty and Almost-Full flags have programmable thresholds
- Active low asynchronous reset
- Active low block enable
- Active low write enable
- Active high read enable
- Ability to configure the FIFO to either stop counting after the empty or full states are reached or to allow the FIFO counters to continue

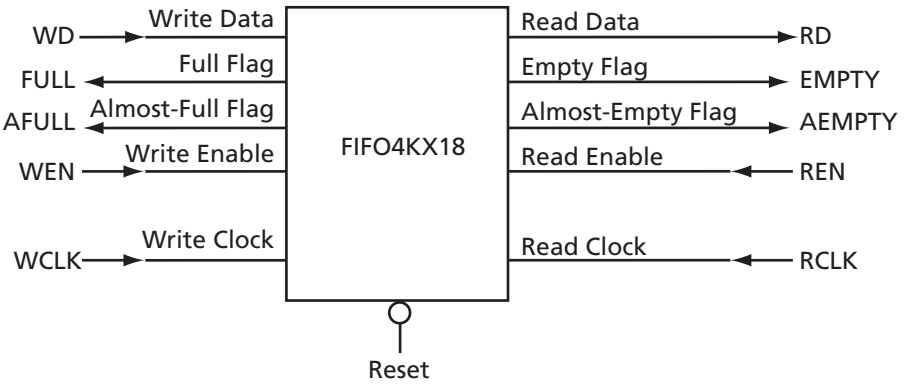


Figure 4.4.3.4 FIFO Ports (Permission pending from Actel)

4.4.4 Current Monitoring

AD590 Temperature Sensor

FEATURES

- Linear current output: 1 μA/K
- Wide temperature range: −55°C to +150°C
- Probe-compatible ceramic sensor package
- 2-terminal device: voltage in/current out
- Laser trimmed to ±0.5°C calibration accuracy (AD590M)
- Excellent linearity: ±0.3°C over full range (AD590M)
- Wide power supply range: 4 V to 30 V Sensor isolation from case Low cost

Applications include:

- Temperature measurement
- Temperature compensation or correction of discrete components
- Biasing proportional to absolute temperature
- Flow rate measurement
- Level detection of fluids and anemometry

The AD590 is a 2-terminal integrated circuit temperature transducer that produces an output current proportional to it's absolute temperature. See Figure 4.3.4.1 below. For supply voltages ranging from 4 V to 30 V, the device acts as a high impedance, constant current regulator passing 1 μA/K. Calibration of the device leads to a calibration factor where a 298.2 μA output corresponds to 298.2 K (25°C).The AD590 is particularly useful in remote sensing applications. The device is not insensitive to voltage drops over long lines due to its high impedance current output.

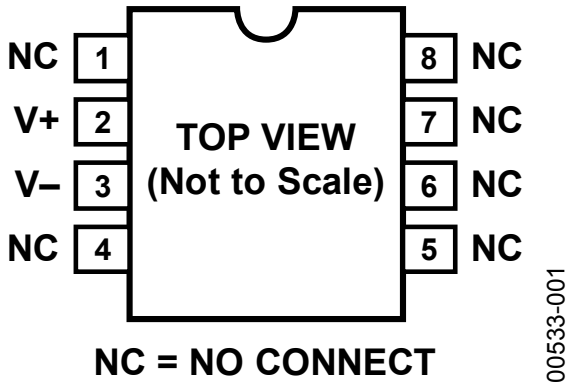


Figure 4.4.4.1 AD590 Pins (Pending approval from Analog)

Current Sense Resistors

Current sense resistors will be used in the system to monitor the 11A current and the external AD590 Temperature sensor. This voltage will then be read by one of the Analog Quad's on the FPGA and multiplied by 10x in the presence amplifier. Once compared to the reference voltage the current and temperature can be calculated. Table 4.4.4.1 shows recommended resistor values for the specified current that needs monitoring.

Recommended Resistor for Different Current Range Measurement	
Current Range	Minimum Resistor Value (Ohms)
> 5 mA – 10 mA	10 - 20
> 10 mA – 20 mA	5 - 10
> 20 mA – 50 mA	2.5 - 5
> 50 mA – 100 mA	1 - 2
> 100 mA – 200 mA	0.5 - 1
> 200 mA – 500 mA	0.3 - 0.5
> 500 mA – 1 A	0.1 - 0.2
>1A–2A	0.05 - 0.1

Recommended Resistor for Different Current Range Measurement	
>2A–4A	0.025 – 0.05
>4A–8A	0.0125 – 0.025
> 8 A – 12 A	0.00625 – 0.02

Table 4.4.4.1 (Permission pending from Actel)

The resistor values are calculated based upon the reference voltage to which the they will be compared. The internal reference voltage is 2.56 volts. This is post amplification so the input voltage will range from 0.00 - 0.256 volts at its maximum. Once the current sense resistor value is chosen it will be connected to the FPGA to the Fusion current monitor in differential mode, shown below in Figure 4.3.4.2. The accuracy of Fusion Current Monitor is ±2 mV minimum plus 5% of the differential voltage at the input.

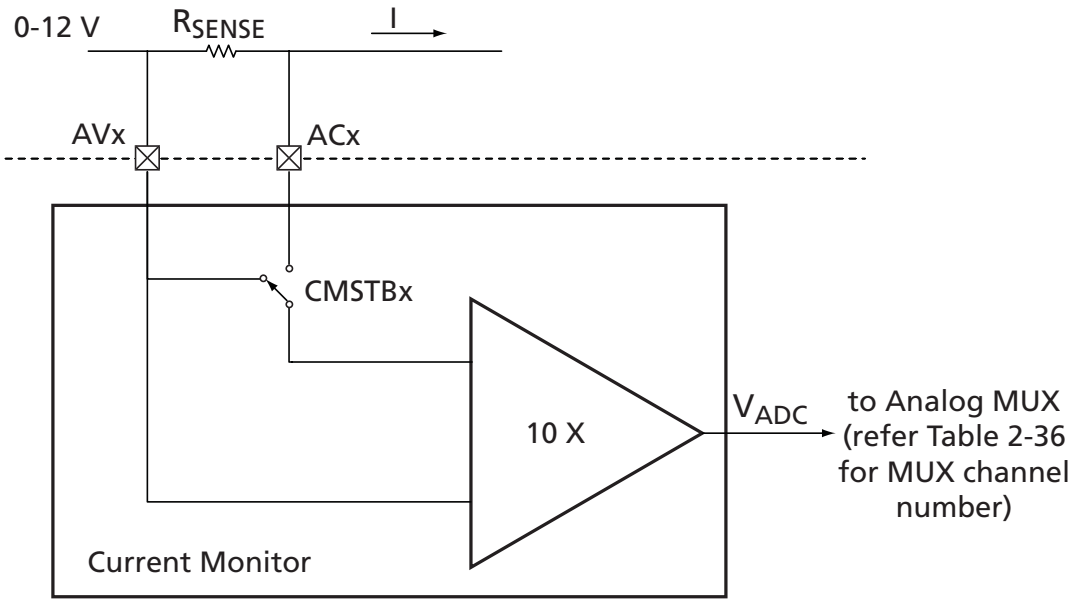


Figure 4.4.4.2 Current Monitor Block Diagram
(Permission pending from Actel)

4.4.5 Software

Development Environment

Once we decided on using the Actel Fusion family of FPGA's we needed to order the parts. One hurdle we found was that the lead-time on the AFS250-QNG180I was 13 weeks. Since this was going to put us near the deadline to finish the project it was crucial we order a development kit. We found the lead time on the AFS-EVAL-KIT was two weeks which would suit our needs and timeline. As seen in the picture below the kit included everything we needed to develop for the Actel fusion family.

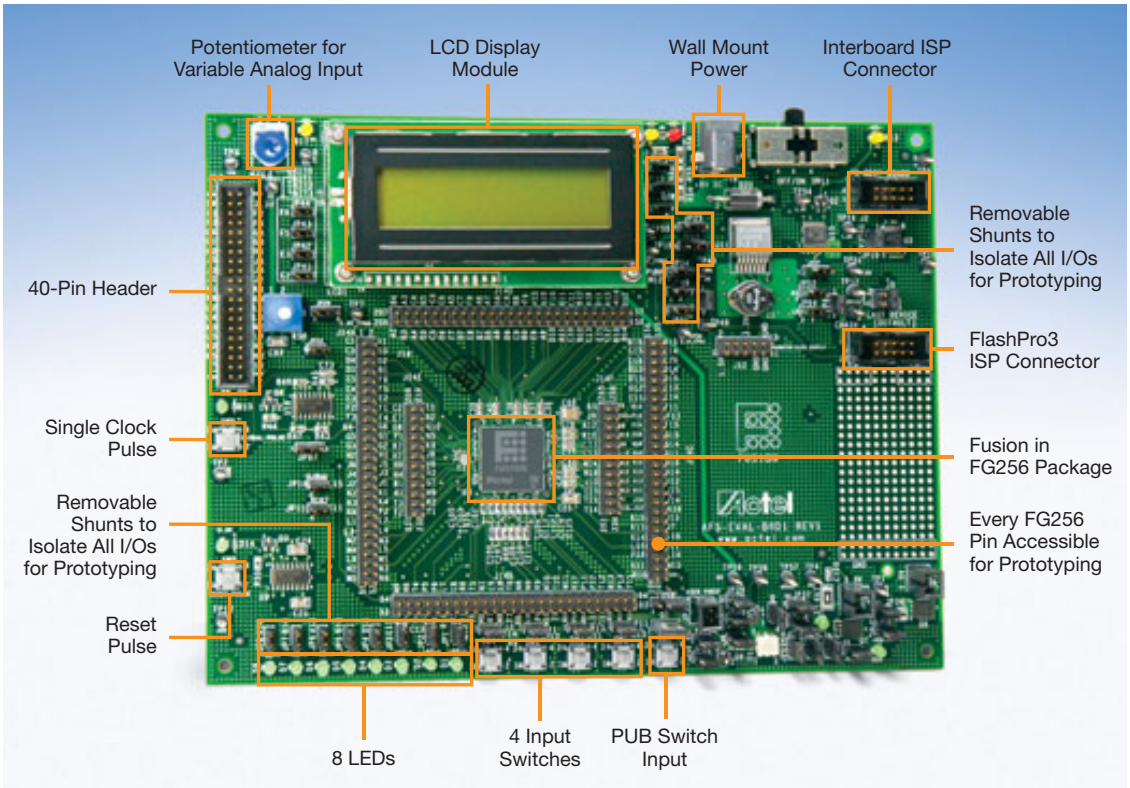


Figure 4.4.5.1 Photo of Eval-kit (PERMISSION PENDING)

The Fusion Starter Kit includes the following:

- Evaluation board with an AFS600-FG256 Fusion device
- Five I/O banks: two can be independently set to 1.5 V or 3.3 V; two are fixed at 3.3 V; and one is for high voltage analog I/Os that support direct connection to voltages ranging from –12 V to +12 V
- On-chip 1% RC oscillator, a crystal oscillator circuit, and Phase-Locked Loops (PLLs): Support system clock generation, manipulation, and distribution
- Eight LEDs and four switches:
- On-board LCD: Displays values of converted analog signals and flash memory contents
- Multi-color LED: Illustrates temperature changes and pulse width modulation (PWM) fan control by varying the brightness

- 40-pin daughter card connector: For use with system boards developed by FlashPro3 programmer
  - Portable and ultra-small form factor
  - Power source via USB 2.0 connection
  - IncludesFlashPro Software, user's guide, and programming cable
- Actel Libero IDE software DVD
  - Gold Edition with free 1-year license
  - Able to support system-on-chip designs with 600 K system gates
- Power supply
- User's guide and tutorial
- Printed Circuit Board (PCB) schematics
- Sample designs

The Actel Libero IDE (integrated development environment) came with an assortment of software design tools for us to work with. While we will not need all the tools, the full list included:

- Project Manager
  - *Dynamically organizes all project files and flows between Libero IDE tools.*
  - *Intuitive interactive dashboard for complete control of design flow.*
  - *Provides hierarchical design and file views and search function.*
  - *Catalog dial-up and configuration of SmartGen/DirectCore IP cores, HDL templates, macros, and busses.*
- SmartDesign
  - *An advanced graphical block-level platform for creating simple and complex designs, including processor and bus-based System-on-Chip (SoC) designs.*
- Soft Console
  - *The Actel development environment that enables rapid generation of C and C++ executables for DirectCore processors.*
- SNPLIFY PRO AE
  - *Industry-leading FPGA synthesis tool*
  - *Fully optimizes design quality of results and device utilization with low runtimes.*
- SYNPLIFY DSP
  - *Performs high-level synthesis and DSP optimizations within a Simulink® environment.*
- MODELSIM AE
  - Industry-leading FPGA simulation tool

- Designer
  - *Comprehensive suite of physical design implementation tools*
  - *Advanced floorplanning, pin assignment, and I/O attribute setting features*
  - *Timing- and power-driven layout*
    - Smarttime
      - *Minimum and maximum delay constraint editors for precise settings and direct steering to layout*
      - *Powerful timing analysis features provide multiple views, constraint scenarios, and reports.*
    - SmartPower
      - *Complete post-layout power analysis capability calculates static and dynamic power consumption*
      - *Power analysis on individual gates, nets, clock domains, I/Os, blocks, rails, or complete design*
- FlashPro Software
  - *Supports FlashPro programmers specifically designed for programming Actel flash products such as Fusion, IGLOO, ProASIC3, and ProASICPLUS families.*
- Synplicity Identity AE
  - Debug your flash design by probing internal signals in the programmed FPGA using a FlashPro programmer.
- Silicon Explorer II
  - *Verifies designs for Actel anti-fuse FPGAs. Internal probe circuitry within the FPGA is accessed by the Silicon Explorer II software. This enables a personal computer to fully emulate a functional logic analyzer.*

These tools along with the development board would allow us to develop the needed software for the timing and control unit. Since the portable development board was designed with standard computer interfaces this would allow us to work on the software outside the lab, which should allow us more learning and development time. When we first started the project we had assumed we would have to select a board from one of Actel's competitors because they offer free development software, but because Fusion has multi-signal capability the benefits of that out weighed the cost of the purchase of the development kit.

The other component needed for our development environment would be a Windows or Linux compatible computer with a USB port. This interface is necessary in order to interact with the development board. The system requirements are listed in FIG 4.3.2. Additional system requirements for the individual Fusion Board are listed in FIG 4.3.3.

Software/ Platform	Processor	File System	Disk Space*	RAM	Other
Libero IDE Windows	1.4 GHz Pentium	NTFS, FAT32	4 GB	See charts below	DVD ROM, HTML browser, 1024x768 resolution
Libero IDE Linux	1.4 GHz Pentium	N/A	2 GB	See charts below	HTML browser, 1024x768 resolution
Designer Windows	1.4 GHz Pentium	NTFS, FAT32	1.1 GB	See charts below	HTML browser, 1024x768 resolution
Designer Linux	1.4 GHz Pentium	N/A	1.3 GB	See charts below	HTML browser, 1024x768 resolution

Figure 4.4.5.2 Fusion Board System Requirements (**PERMISSION PENDING**)

Fusion

Device	RAM	Virtual Memory
AFS090	256 MB	512 MB
AFS250	384 MB	768 MB
AFS600, M1AFS600, M7AFS600	512 MB	1 GB
AFS1500, M1AFS1500, M7AFS1500	1 GB	2 GB

Figure 4.4.5.3 Fusion Memory (**PERMISSION PENDING**)

4.4.6 Clock Resources

Our FPGA has onboard Clocking resources. (see Figure 4.3.8.1 below) These on-chip resources enable the creation, manipulation, and distribution of clock signals. The integrated RC oscillator produces a 100 MHz clock source without the need for external components. The chip also has integrated PLL's which can use the RC oscillator, crystal oscillator, or other on-chip clock signal as a source. The PLLs offer a variety of capabilities to modify the clock source (multiply, divide, synchronize, advance, or delay).

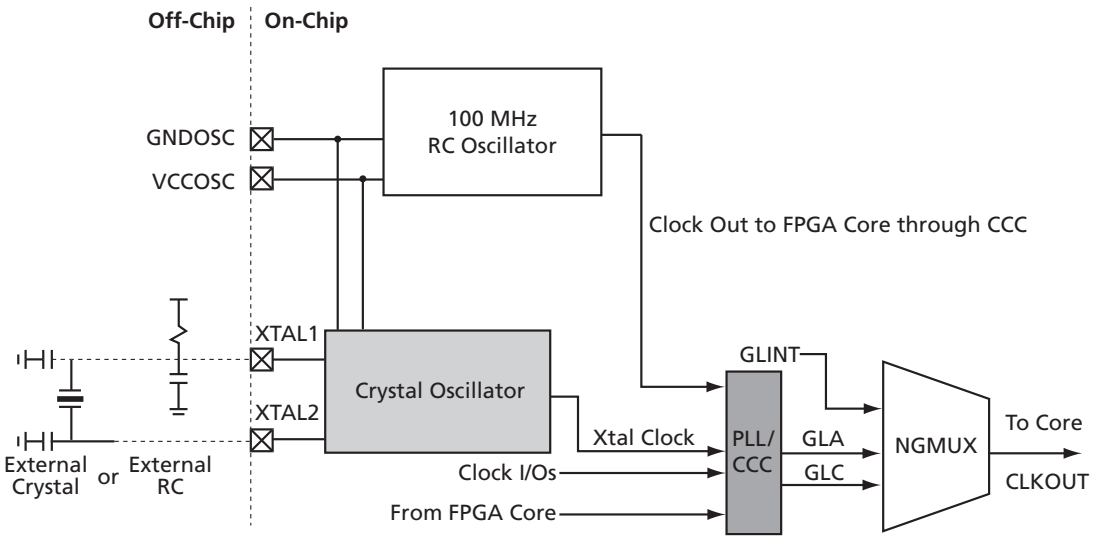


Figure 4.4.6.1 Clock resource block diagram
(PENDING PERMISSION FROM ACTEL)

Our FPGA also provides flexible clock conditioning circuits (CCC) (See Figure 4.4.6.2). Each member of the Fusion family contains six CCCs and at least one PLL. The inputs of the CCC blocks are accessible from the FPGA core or from one of several inputs with dedicated CCC block connections. The CCC block has the following key features:

- Wide input frequency range (fIN_CCC) = 1.5 MHz to 350 MHz
- Output frequency range (fOUT_CCC) = 0.75 MHz to 350 MHz
- Clock phase adjustment via programmable and fixed delays from –6.275 ns to +8.75 ns
- Clock skew minimization (PLL)
- Clock frequency synthesis (PLL)
- On-chip analog clocking resources usable as inputs:
  - 100 MHz on-chip RC oscillator
  - Crystal oscillator
- Internal phase shift = 0°, 90°, 180°, and 270°
- Output duty cycle = 50% ± 1.5%
- Low output jitter. Samples of peak-to-peak period jitter when a single global network is used:
  - 70ps at 350MHz
  - 90ps at 100MHz
  - 180ps at 24MHz
  - Worst case < 2.5% × clock period
- Maximum acquisition time = 150 µs
- Low power consumption of 5 mW

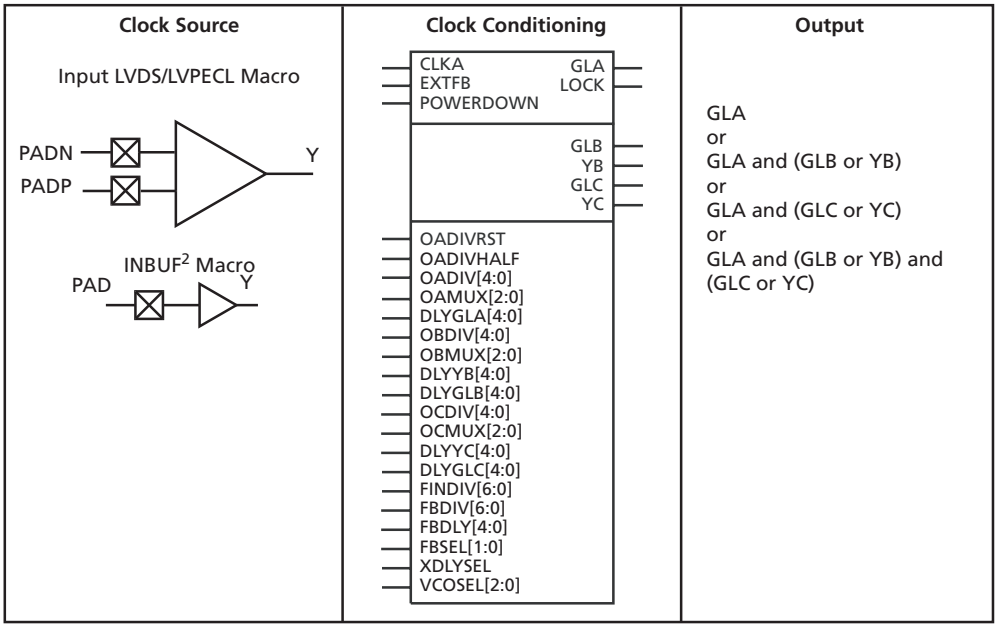


Figure 4.4.6.2 Clock conditioning and output
(PENDING PERMSSION FROM ACTEL)

Global Clocking

The FPGA also has support for multiple clocking domains. In addition to the CCC and PLL support, there are on-chip oscillators and a global clock distribution network. The integrated RC oscillator generates a 100 MHz clock. It is used internally to provide:

- A clock source to the flash memory read and write controls.
- A clock source for the PLLs

The crystal oscillator supports the following operating modes:

- Crystal (32.768 kHz to 20 MHz)
- Ceramic (500 kHz to 8 MHz)
- RC (32.768 kHz to 4 MHz)

RC Oscillator

The RC oscillator can be used as a source clock for both on-chip and off-chip resources. When used in conjunction with the Fusion PLL and CCC circuits, the RC oscillator clock source can be used to generate clocks of varying frequency and phase. The Fusion RC oscillator is very accurate at ±1% over commercial and industrial temperature ranges. It is an automated clock, requiring no setup or configuration. It requires only that the power and GNDOSC pins be connected;

no external components are required. The RC oscillator can be used to drive either a PLL or another internal signal. A more detailed description of the electrical characteristics are located below in Table 4.4.6.1.

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
FRC	Operating Freq.			100		MHz
	Accuracy	Temperature: 0°C to 85°C Voltage: 3.3 V ± 5%		1		%
		Temperature: –40°C to 125°C Voltage: 3.3 V ± 5%		3		%
	Output Jitter	Period Jitter (at 5 k cycles)		100		ps
		Cycle–Cycle Jitter (at 5 k cycles)		100		ps
		Period Jitter (at 5 k cycles) with 1 kHz / 300 mV peak-to-peak noise on power supply		150		ps
		Cycle–Cycle Jitter (at 5 k cycles) with 1 kHz / 300 mV peak-to-peak noise on power supply		150		ps
	Output Duty Cycle	Period Jitter (at 5 k cycles)		50		ps
IDYNRC	Operating Current			50		%
				1		mA

Table 4.4.6.1 Electrical Characteristics of RC Oscillator

4.4.7 Security

Security options can be categorized into the following three options:

- AES (Advanced Encryption Standard) encryption with FlashLock Pass Key protection
- FlashLock protection only (no AES encryption)
- No protection

AES Decryption in Fusion Devices

Fusion has a built-in 128-bit AES decryption core, which decrypts the encrypted programming file and performs a MAC check that authenticates the file prior to programming. An example of the utilization of AES is in the figure below. This will ensure the following:

- Correct decryption of the encrypted programming file
- Prevention of erroneous or corrupted data being programmed during the programming file transfer
- Correct bitstream passed to the device for decryption

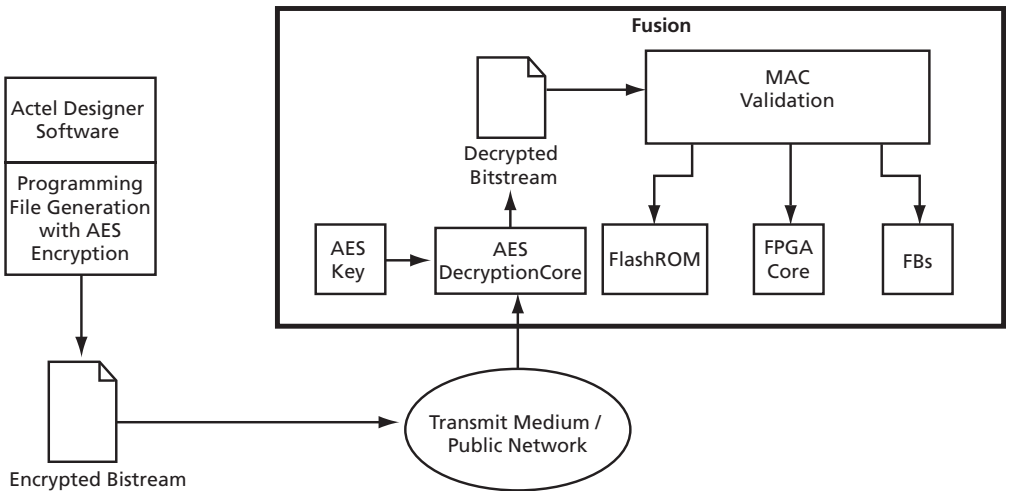


Figure 4.4.7.1 AES Decryption Core (Permission Pending from ACTEL)

AES decryption can also be used on the flash memory blocks. This allows for the secure update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

FlashLock

FlashLock provides a combination of reprogrammability and design security. Because the fusion is flash-based it requires no boot PROM, eliminating a vulnerability in the external bitstream. The 128-bit FlashLock feature works via a key mechanism. The user locks or unlocks the device with a user-defined pass-key. When locked, there is no access to the FPGA without the correct pass-key. By default, functions such as device write, verify, and erase are disabled.

4.4.8 Analog to Digital Converter

The Actel Fusion FPGA has an integrated ADC, which eliminates the need for an external ADC integrated circuit. The onboard ADC supports resolutions of up to 12 bits and sampling rates up to 600 ksps. Other design specifications include:

- Integrated A/D Converter (ADC) and Analog I/O
- Up to 12-Bit Resolution and up to 600 ksps
- Internal 2.56 V or External Reference Voltage
- ADC: Up to 30 Scalable Analog Input Channels •
- High-Voltage Input Tolerance: –10.5 V to +12 V •
- Current Monitor and Temperature Monitor Blocks •
- Up to 10 MOSFET Gate Driver Outputs
- P- and N-Channel Power MOSFET Support
- Programmable 1, 3, 10, 30 µA and 20 mA Drive Strengths •
- ADC Accuracy is Better than 1%

When using the calibration option with the Fusion device, we can achieve better than one percent accuracy, which will meet or exceed the level of accuracy that is required for our project.

Calibration Mode

Calibration Mode eliminates certain errors common to ADCs, such as offset and gain errors. If these errors were not adjusted for, the measurements would be inaccurate and could impact the overall system performance. External components could be used to eliminate the offset and gain errors however this would add extra design complexity, noise and additional inaccuracy that in turn need to be eliminated. An ideal solution would be an integrated device that provides this high accuracy without penalty. The Fusion FPGA has several features like the embedded flash, analog quad and flash memory, that can be used along with software calibration to provide better than 1 percent accuracy.

Analog Quad

The configuration of the analog quads is shown in Figure 4.4.1.1 What makes the Fusion ADC so useful is a series of 6-10 Analog Quads (depending on model) integrated directly into the chip. The AFS250, which we will be using, will have six of these. Each of these Analog Quads can be configured to support voltage, current, and temperature measurements. Any of the three inputs can be configured to provide a single-ended voltage measurement. Another voltage measuring method is to use the AV (Analog Voltage) and AC (Analog Current) inputs as a differential pair to measure the voltage drop across an external current sense resistor. The AT (Analog Temperature) input can be configured to supply a small oscillating current to an external diode to measure ambient temperature. Since we will be monitoring a given temperature sensor, this feature will most likely not be used.

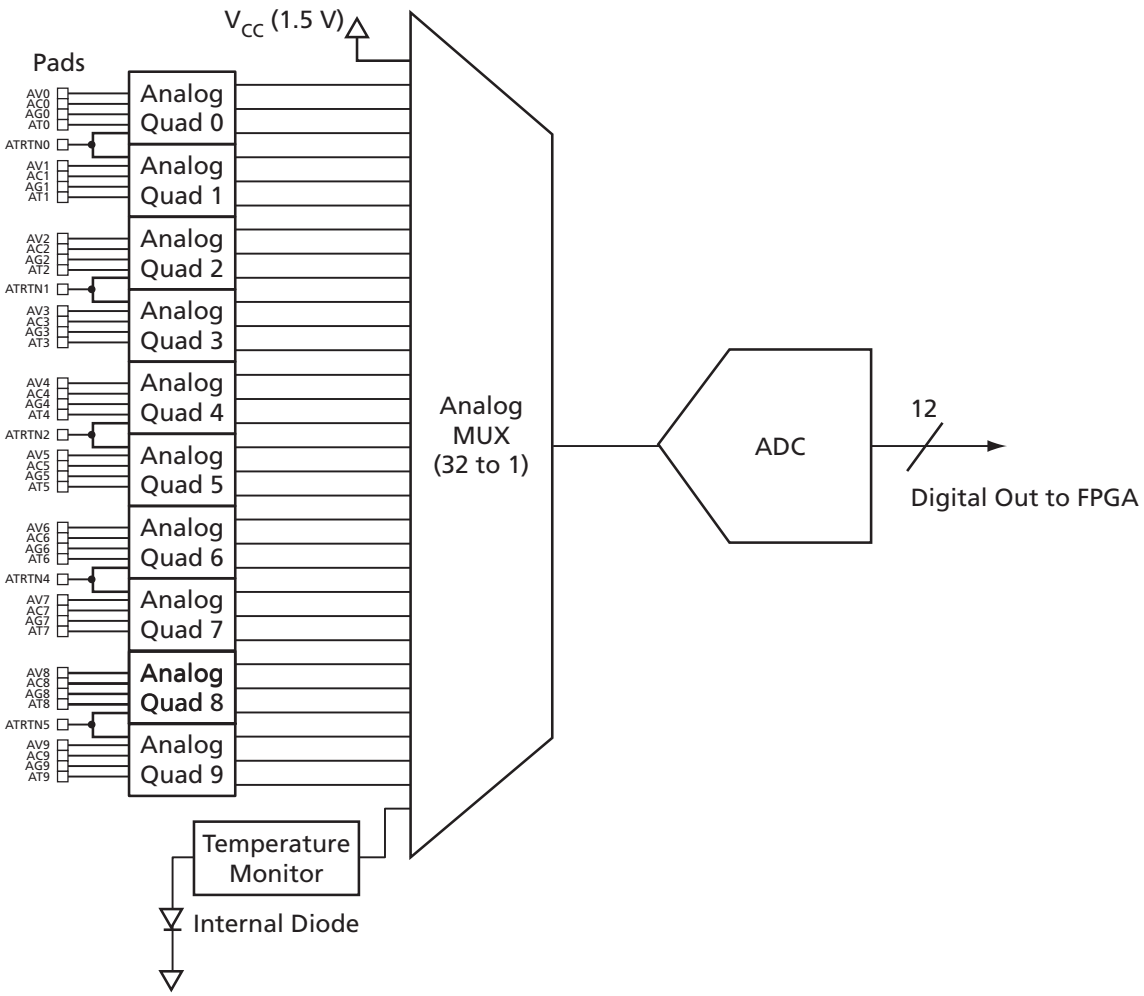


Figure 4.4.8.1 Analog Quad block diagram
(Permission pending from Actel)

Voltage Monitor

The maximum voltage tolerance of the analog inputs is ±12 V with respect to ground. Each input has a built-in pre-scale amplifier that can be configured to:

- provide 8, 10, or 12-bit sampling resolution over input voltage ranging from zero to 0.125, 0.250, 0.50, 1.0, 2.0, 4.0, 8.0, or 16.0 V.
- invert negative voltages with respect to ground into positive-sampling signals.
- 12-bit ADC in Actel Fusion FPGAs provides voltage measurements with 4 mV resolution and unadjusted accuracy of 25 mV
- The ability to scale input voltages eliminates external components and improve precision for voltage measurements.

Current Monitor

For current measurements and monitoring, a differential amplifier can measure the minute voltage drop across an external current sensing resistor. This amplifier has a fixed gain of 10X, so a voltage drop of 0.256 V corresponds to a 2.56 V input. Assuming that an internal reference voltage of 2.56 is used, this means that a 0.025 Ω resistor can measure up to 10 A of current with 2 mA resolution and total error of only 12 mA. Unlike voltage measurements for current measurements, AV must be at a greater voltage level than AC, so bidirectional current sensing requires two sense resistors and two Analog Quads, connected as shown in Figure 4.4.1.2

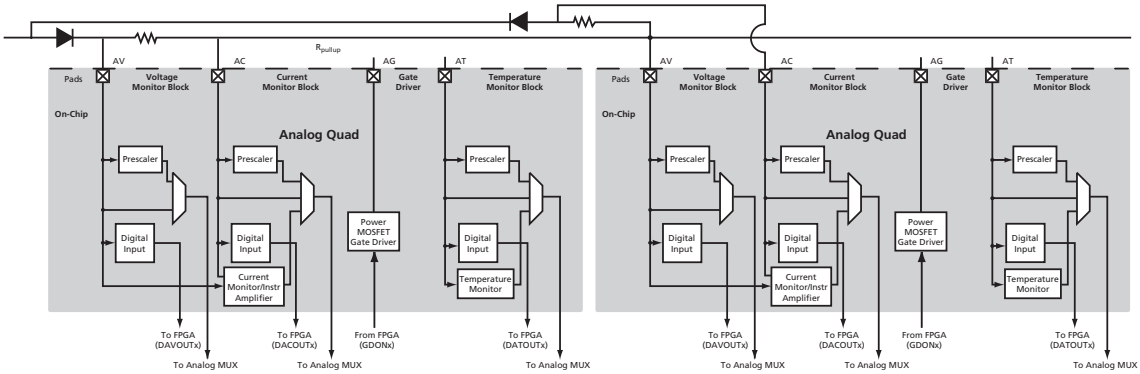


Figure 4.4.8.2 Bidirectional Current Sensing
(Permission pending from Actel)

Temperature Monitoring

Temperature is measured using an inexpensive bipolar silicon transistor connected to the AT input of the Analog Quad. When this quad is configured to monitor temperature, it provides two generated strobe currents to the diode connected transistor and then measures the difference between the resulting forward voltages. This method provides temperature measurements accurate to within 2°C.

Digital Functions

ADC resolution can all be directly controlled via a simple 8-bit interface available to user logic in the FPGA logic gates. To provide maximum flexibility for Fusion designs, the FPGA logic has complete access and control over:

- The entire analog block of the device
- Analog Quad configuration
- multiplexer selection
- Settling time
- ADC reference source

- ADC clock frequency

4.5 Schematics

The diagrams in this section display the values of the supporting passive parts of the power supply. The following diagrams are only schematics for the low power lines. The diagram below, Figure 4.4.1, is the schematic of the LT4612 and LT1963 that for the 9 volt line.

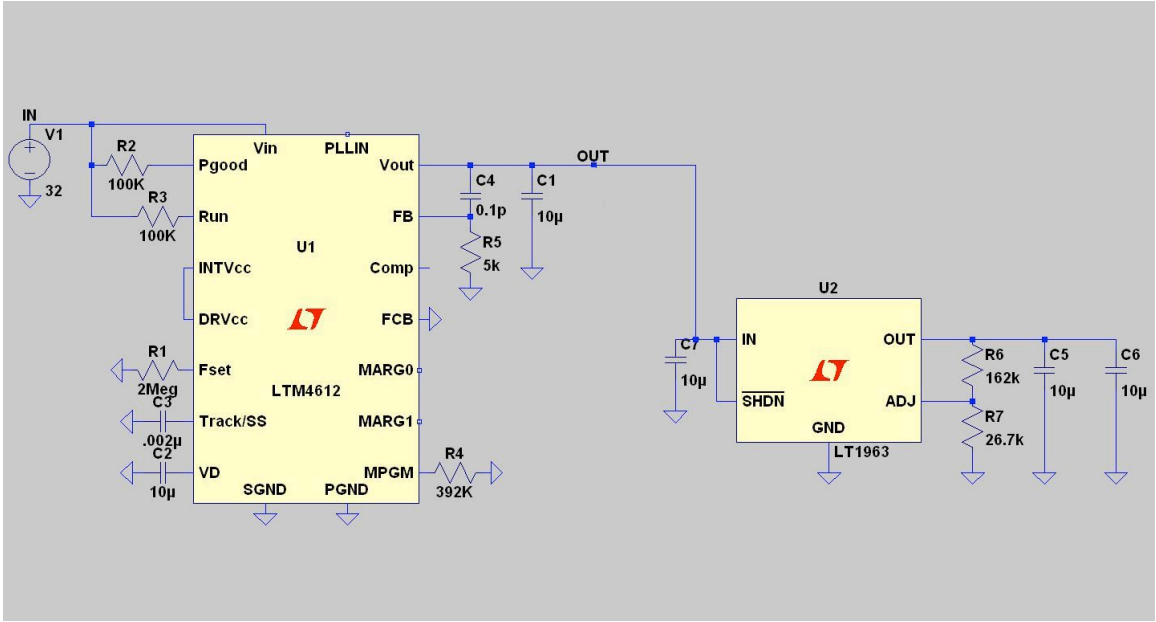


Figure 4.5.1 9V Low Power Line. Recommended circuit by Linear Technology

The next two diagrams are successive of each other. The LT4612 supports both -4V line and the +6V line. The first diagram, Figure 4.5.2, is the beginning of both lines. Ref.1 is designating that the line continues on to the next diagram, Figure 4.5.3, where the schematic for the negative voltage output is displayed.

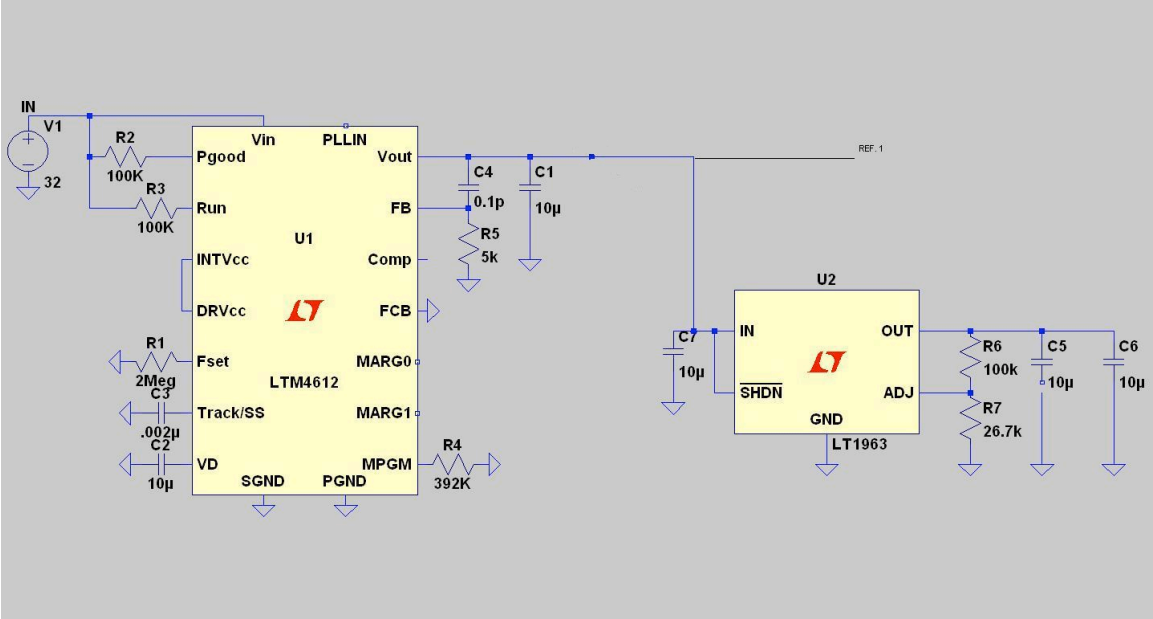


Figure 4.5.2 6V
Low power line. Recommended circuit by Linear Technology

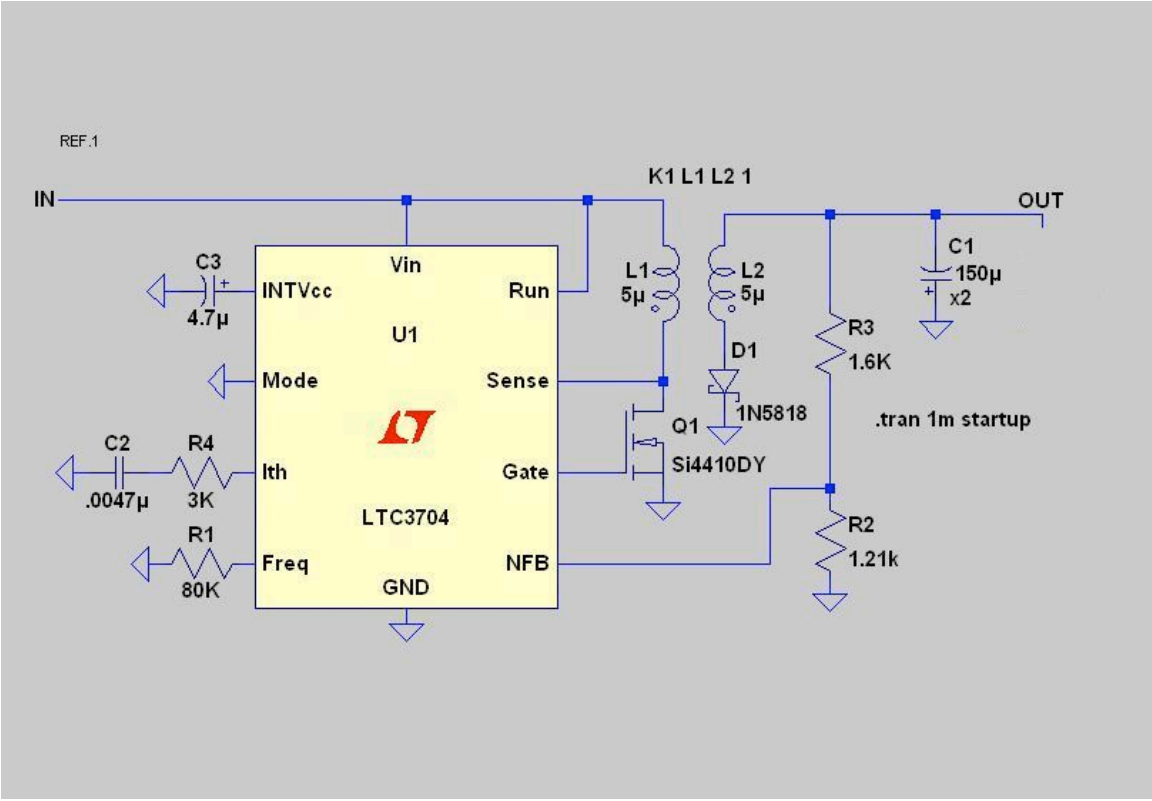


Figure 4.5.3
-4V power line continued from Figure 4.4.2.
Recommended circuit by Linear Technology

4.6 PCB Layout

The printed circuit board will have the functions of the timing control unit and power architecture. It will also serve as a test card for the low power signals and a filter for the 32Vin. As this is a prototype for the customer it is not necessary to have the test card separate from timing control unit and power architecture. This implementation will manufacturing, testing, and demonstration simpler because it will all be in one unit. The board will be allotted space for each function. The timing control unit and power architecture will remain in in an area of the board together. The dimensions allotted to these functions will stay strict to the specifications of 6 square inches. The remainder of the board will not have to be constrained to customer specifications. The middle of the PCB will have the timing control unit and power architecture with dimensions of 3 inches by 2 inches. The whole board will be 6 inches by 5 inches. This leaves 1.5 inches on all sides for the test card and filtering. The diagram below, Figure 4.6.1, displays the dimensions of the circuit card.

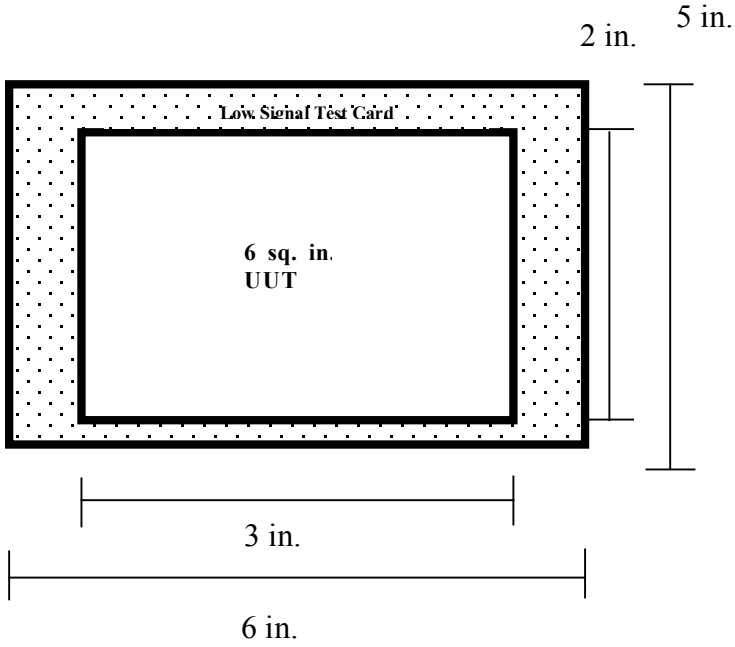


Figure 4.6.1 Dimensions of circuit board

There preliminary design will have 5 layers. As there is high power and small surface area for parts, multiple layers are needed to handle the traces. The diagram below, Figure 4.6.2, shows the padstack. The signal layers have their traces running perpendicular to each other. The top most signal layer has traces running into the page, while the lower signal layer has traces running along the page.

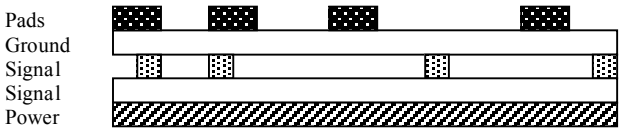


Figure 4.6.2 Padstack

Copper traces will be at least 50 mils (0.05 inches) from any edge of the circuit board. As well, the timing control unit and power architecture area of the board will have to follow that the copper traces are at least 50 mils from the designated edge. All parts will be surface mounted except for the power connector. The power connector will be through-hole. The top surface of the board will have all the parts. The following table , Table 4.6.1 displays the surface area of each part.

Part #	Amount Used	Area	Total Area
LTM 4612	3	675	859.622854
LT1963	2	65.28	130.56
HMC-VVD104	1	3.67155	3.67155
LTC3704	1	15.671304	15.671304
Fusion	1	100	100
TOTAL AREA			1109.525708

Table 4.6.1 Surface Area of each part. Values are in mm.

5 - Testing

The testing phase is an important process that will determine if the prototype design will function. Given the magnitude of this phase, a careful test plan must be followed and implemented in order to assure the success of the prototype. Many times in engineering the desired specs given to the engineer cannot be met for various reasons, and therefore negotiation between the designer and the customer or boss ensues. Depending on the importance of the given spec, a compromise can be made or further design will have to be made in order to meet the spec. The group is very aware of this fact, and as a result communication between the sponsor of the group and the group members has been an important factor throughout the semester and will be until the prototype is finally put together. At the time of this documentation, only simulations of the power modules have been done successfully meeting the given requirements. However, the step between simulation and implementation brings unknowns to

the table and therefore the only way to know if the prototype works is by proving it. This chapter will serve as a guideline for the test procedure of the power supply and its controller.

5.1 Introduction

Without having the true transceiver and gimble system a load will have to be used to simulate it. The supply voltage, 32 volts, and 3.3 volts for the FPGA will have to be provided in the test setup. This will have to be considered for demonstrations purposes as well. The output voltages will have to be pulled out to a test card to be more readily accessible. Testing will include voltage readings, current readings, temperature readings, correct timing for pulsing from FPGA to high power signal line, and testing of other timing signals. The FPGA will have to have different loads for different test scenarios, including failed power up sequence. The failed power up sequence will force the FPGA to go into power down sequence. A non-failure test scenario will also have to be loaded to demonstrate successful power up sequence. The readings from the temperature sensor will have to be demonstrated also. There will also be onboard available test points. Materials needed for testing will include an oscilloscope with 4 channels, dual power supply for 32 volts and 3.3 volts, resistors for the simulated load, JTAG interface for FPGA to computer, and computer to load different sequences to the FPGA.

5.2 Safe To Turn On Test Plan

Before any power is applied to the board safe to turn on tests must pass. The power to ground must be tested for all parts on the board. Also, 32Vin and 3.3Vin must be verified that they are shorted.

5.3 6XMIT Test

The 6XMIT is used to drive the transceiver. It has to supply a load for durations of 1 to 100 µS and shall not exceed 50 % duty cycle. As a result, a switching element has to be designed in order to imitate the load. In addition, the load has to be resistive which will be provided by either Lockheed Martin or Diego Rocha. Diego Rocha works at Electrodynamics Associates where high power generators and motors are designed and tested. He is in charge of testing and designing the controllers for generators and motors and as a result he has a 200 kW resistive load available. The advantage of using the resistive load bank is that its temperature will not change by the power supplied by the 6XMIT module. This is because the power supplied by the dc/dc converter is very small relative to the rating of the load bank and therefore the resistance of the load will not change. In contrast, using the resistive load provided by Lockheed Martin will have the effect of having a resistive load whose resistance will vary as the heat dissipated by the load increases. The disadvantage of having a resistive load that changes with time is that the current drawn by the load will vary which may lead to

erroneous conclusions. Either way, one of the two loads will be chosen in the future and precautions will be taken in order to get accurate results.

As mentioned before, once the prototype is ready to be tested a load that mimics the transceiver will have to be used. A resistive load will be used and the pulse interval repetitions that the transceiver will draw will be commanded by an n channel MOSFET. The frequency and duty cycle will be controlled by the F2808 DSP board from Oztek. The schematic below shows the set up for testing the 6XMIT power supply.

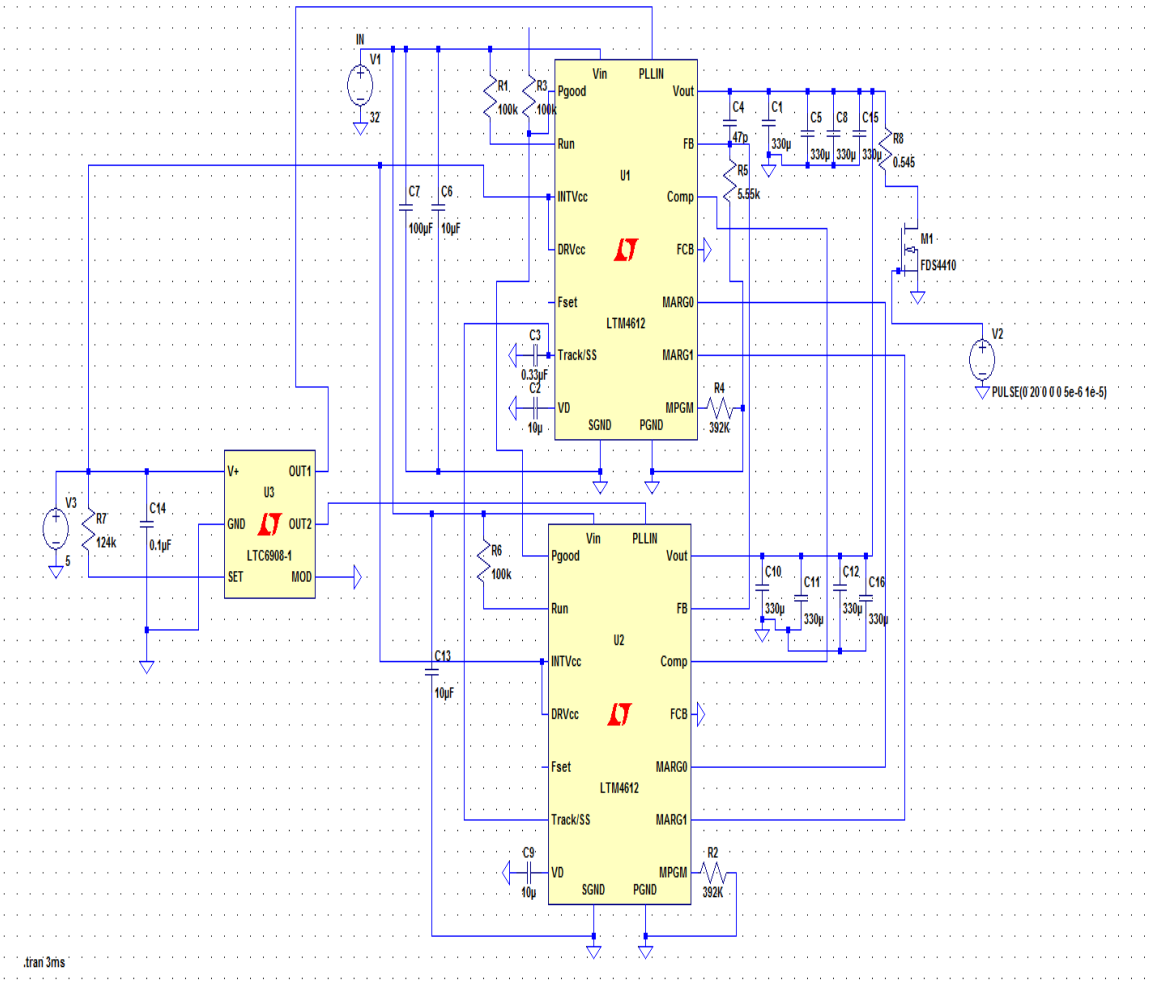


Figure 5.3.1
6XMIT power supply

The circuitry in figure 5.1 has a pulse source that connects to the gate of the n channel MOSFET. The pulse source acts as the driver for the MOSFET and the resistor R8 serves as the resistive load. These two devices are not part of the design but they are for testing purposes.

Texas Instruments F2808 DSP

In order to test the 6XMIT power supply, a load that draws a pulsed current with a frequency ranging from 1 kHz to 100 kHz with a duty cycle no greater than 50 percent has to be design. This is why the F2808 DSP was selected as the micro-controller that will generate a PWM signal that will drive the MOSFET shown in the system in figure 5.1. The driver is depicted in the figure 5.3.2 below.

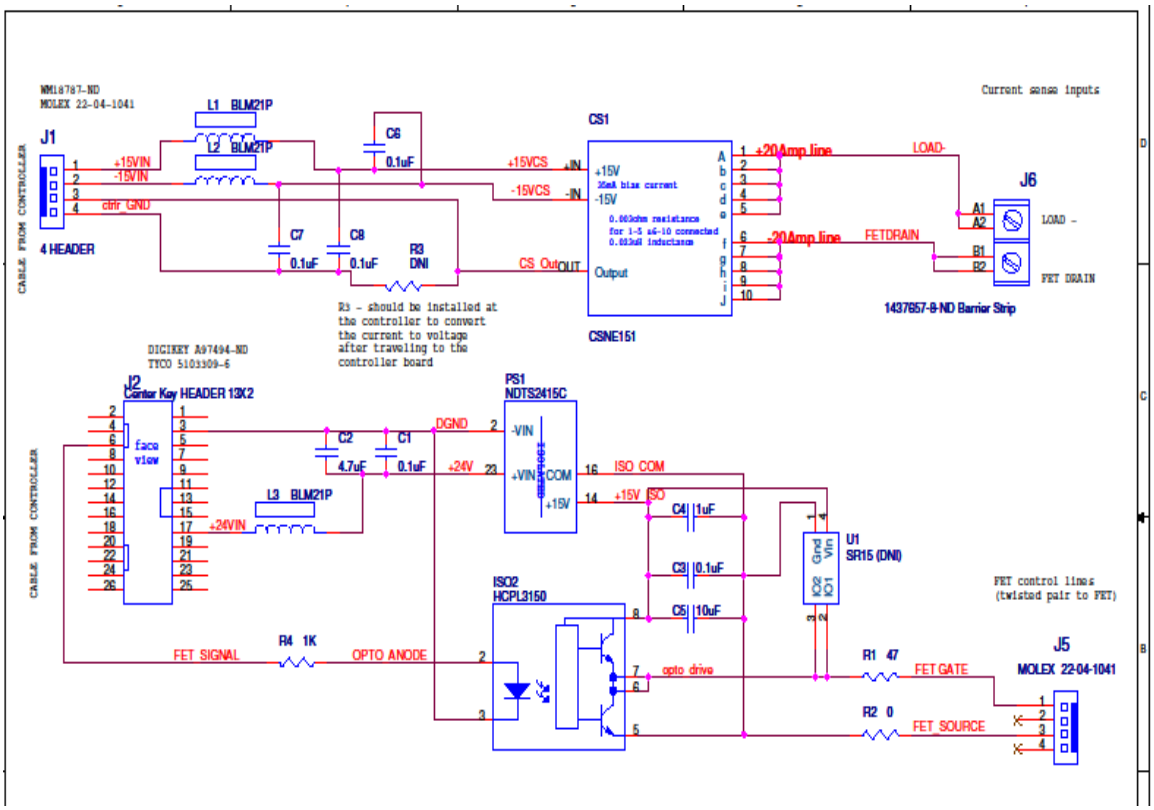


Figure 5.3.2.
Driver circuitry for the MOSFET

The 13x2 header is a ribbon cable that connects to the microcontroller where pin number 6 is the PWM signal that goes to the gate of the MOSFET in figure 5.1. Pin 17 and 3 provide a +24 V dc that feeds to an isolated dc/dc buck converter that steps down the voltage to +15Vdc. The +15Vdc volts is used to turn on the HCPL3150 module which is an optocoupler that provides isolation between the load and the microcontroller. The isolation circuitry was chosen in order to protect the microcontroller and computer in case a failure occurs. In addition, the optocoupler steps up the voltage coming from pin 6 from +5Vdc to +15Vdc which is what the MOSFET needs to turn on. The U1 is a test point for the signal going to the MOSFET for debugging purposes. J1 is used to power up the current sensor by providing the +15 Vdc and -15Vdc needed by the current sensor, and pin 3 receives the feedback from the current sensor. The 6XMIT is going to be

controlled in an open loop mode where a duty cycle will be commanded at a given frequency. The module could also be tested in closed loop mode by regulating the current going to the load. This is not going to be implemented because it adds more complexity to the test plan. That said, the current going to the load will be monitored across the resistor R3 by looking at the voltage across it. The current sensor provides 1mA per amp, so by knowing the voltage across R3, the current can be found.

5.3.1 Test Plan for the 6XMIT

Purpose

The purpose of this test is to show that the high power supply or the 6XMIT works under different frequencies and duty cycles no greater than 50 percent. The test will be conducted under different frequencies and the duty cycle will be varied from 10% up to 50% in steps of 10. The microcontroller will be program to send a PWM signal at a set frequency and at that frequency different duty cycles will be commanded as mentioned before. Once this is done, the frequency will be set to another value and the same test will be performed.

Test equipment

Item	Manufacturer	Description	Purpose
1	Fluke	Digital Multimeter	Verify voltages in the circuit
2	Oztek Corp.	DSP Board	Controller for the system
3	Texas Instruments	Code Composer Studio	Source Code Editor
4	Vector	CANalyzer	GUI for controller
5	PicoLog Recorder	PicoScope	Measure Temp of 6XMIT
6	Tektronix	Oscilloscope	Display waveforms
7	TBD	Spectrum Analyzer	Noise Analysis
8	N/A	Load Bank	Resistive Load
9	Newton	Power Analyzer	Efficiency of power supply
10	Spectrum Digital	Emulator	Download Code to DSP
11		Power supply	Power for Microcontroller

Table 5.3.1 displays a tentative list of equipment that will be used during testing.

Most of the equipment shown in table 5.2 is available at Electrodynamics Associates. The president of the company, Jay Vaidya has agreed on letting the group members use the equipment. The only equipment needed is the spectrum analyzer which is not an issue because the department of Electrical Engineering at UCF will provide spectrum analyzers at the senior design lab next semester. As a result, the tests will be conducted at the senior design lab and at the Electrodynamics Associates lab. However, the majority of the test will be

conducted at the Electrodynamics lab, the only part of the test to be conducted at the senior design lab will be the noise analysis. Because of this, the resistive load provided by Lockheed Martin will be used at the senior design lab.

Procedure

1. Connect the positive lead of the 6XMIT power supply to the resistor load bank as shown in figure 5.3.3. The other side of the resistor then goes to the source of the MOSFET, and the drain of the MOSFET goes to the return of the power supply and the return of the controlled signal coming from the driver (pin 3 in figure 5.3.2).
2. Connect the driver circuitry to the gate and source of the MOSFET.
3. Open up Code Composer Studio on the laptop.
4. Open up the senior design program under workspace.
5. Connect the emulator to Code Composer Studio.
6. Load the program under load, the program should automatically pop up in the window, click ok.
7. Click real time and then ok under the debug option.
8. Right click under the watch window and turn on the continuously refresh option.
9. Click the run icon on the left side of the window.
10. Power up the system; current shouldn't be flowing out of the 6XMIT power supply because the driver is not sending a signal to the MOSFET yet.
11. Make sure that the voltage out of the dc/dc converter is +6Vdc. So far all the components should be connected as shown in figure 5.3.
12. Write 1 for 'run' under the watch window, this will send a pulsed signal with a duty cycle as commanded on the watch window to the MOSFET and the power supply will start supplying power to the load now.
13. Vary the duty cycle under the watch window; the duty cycle cell lets you do this.
14. Measure output voltage and current that the 6XMIT supplies by connecting the positive side to the power analyzer and the negative coming from the power analyzer to the positive rail of the load. Note that the maximum rating of the power analyzer for measuring current that is directly connected to the device is 30 A.
15. In order to stop the current flow to the load, the run option on the watch window has to be set to 0.

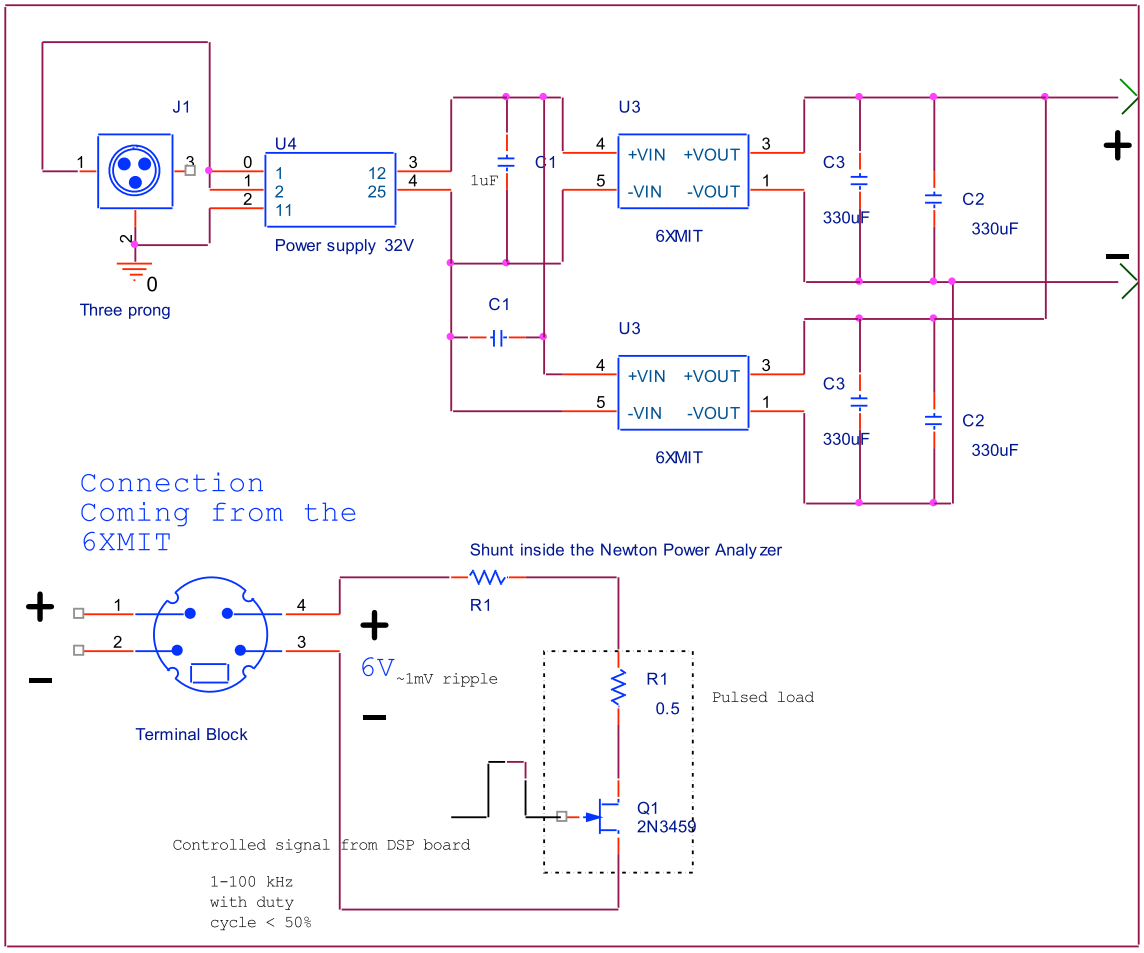


Figure 5.3.3
Schematic showing set up for testing the 6XMIT module.

Precautions

Since the accuracy of the signals that have to be measured on the 6XMIT power is critical, long wires coming from the 6XMIT to the load have to be kept as short as possible. This will minimize parasitic inductances coming from the wires which could result in erroneous measurements. As of right now, the distance from the power supply to gimbal on the transceiver is unknown; however, upon knowledge of the distance between the two, a wire with the same gauge as that used in the real application and distance will be chosen to connect the power supply to the load bank.

The temperature of the power module will be monitored via thermocouples. One thermocouple will be placed between the bottom part of the module and the PCB. Another thermocouple will be placed on the top of the module. The temperature measured by the two thermocouples will be recorded on a picologger and

transferred to the computer where it will be plotted. The purpose of doing this is to ensure that the module is not overheating.

Results

Load Frequency	Duty Cycle	Vout ripple	IL	Noise
kHz	%	V	A	dB
1	10			
1	30			
1	50			
5	10			
5	30			
5	50			
10	10			
10	30			
10	50			
30	10			
30	30			
30	50			
60	10			
60	30			
60	50			
80	10			
80	30			
80	50			
100	10			
100	30			
100	50			

Table 5.3.2 shows the data that will be collected in order to prove that the high power module or the 6XMIT functions properly

5.4 Low Power Signals Test

The low power signals need to be tested by a safe to turn on procedure before the board is powered. Also, the card must be tested for demonstration purposes. The test card will pull out signals to be more readily accessible for testing. The test card will also serve as the simulated load for the low power signals and will also filter the 32 incoming voltage signal. The incoming voltage, as per the specifications, must have a ripple voltage of no more than 100uV. The power supplies that will be used to power the board will not give this clean of a signal. The unit under test, UUT, and low power signal test card will be built as one PCB for easy demonstration purposes. There will be a specific amount of space allotted on the board that will be dedicated solely to the power supply and control

unit. This allotted space will strictly constrain to the specifications. The remainder of the PCB will not have to be confined to strict real-estate because it is only for testing purposes. The following diagram, Figure 5.4.1, displays the concept of the test card and UUT integration on one board.

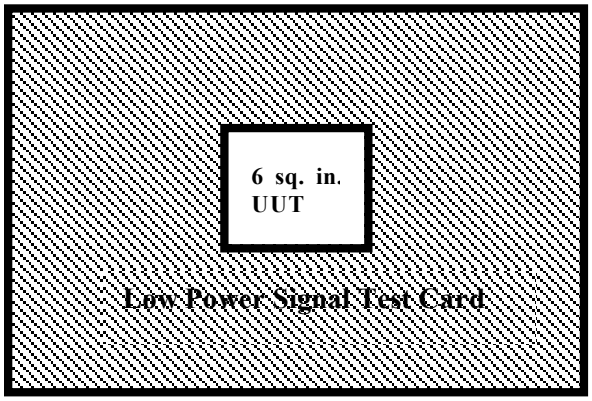


Figure 5.4.1 UUT and Test card Integrated

Purpose

The low power architecture needs to generate three different voltages from one source. The test will verify that the 32 volts is a clean signal as it would be in the seeker. The test will also verify that the correct voltages are being generated. An oscilloscope will be used to verify tolerances and ripple voltage.

Test equipment

Item	Manufacturer	Description	Purpose
1	Fluke	Digital Multimeter	Verify voltages in the circuit
2	TBD	Spectrum Analyzer	Noise Analysis
3		Power supply	32Vin
4	Agilent	Oscilloscope	Ripple voltage/ tolerances
5		32V Cable	Power from test card to UUT
6		JTAG	Interface FPGA with computer

Table 5.4.1
Displays a tentative list of equipment that will be used during testing.

All the equipment will be available in the Senior Design Lab, except the power supply. The means to acquire the power supply is TBD.

Procedure

Oscilloscope Test

1. The UUT must be set on an ESD approved surface.
2. Attach 32 volt cable from P1 to J1. Refer to Figure 5.4.2.
3. Attach 32 volt cable from power supply to J2. Refer to Figure 5.4.2.
4. Attach 3.3 volt cable to J3. Refer to Figure 5.4.2.
5. Attach JTAG to J4. Refer to Figure 5.4.2.
6. Apply power only for 3.3 volts.
7. Load FPGA test load 1.
8. Apply power for 32 volts.
9. Measure voltage with oscilloscope at test points T1, T2, T3, T4, T5. Refer to Figure 5.4.3. Record in log, found below Table 5.2.6.1, results for voltage and ripple voltage.
10. Measure noise with spectrum analyzer. Record images on external media.
11. Shut off 32 volts.
12. Load FPGA test load 2.
13. Use oscilloscope. Attach channel 1 probe to T1. Attach channel 2 probe to T2. Set to trigger on rising edge. Refer to Figure 5.4.3.
14. Apply power for 32 volts.
15. Measure time between power ON and rising edge. Record results in log found below, Table 5.4.3.
16. Shut off 32 volts.
17. Use oscilloscope. Attach channel 1 probe to T3. Attach channel 2 probe to T4. Attach channel 3 probe to T5. Set to trigger on rising edge. Refer to Figure 5.4.3.
18. Measure time between power ON and rising edge. Record results in log found below, Table 5.4.3.
19. Turn off 3.3 volts.
20. Turn off 32 volts.

Logic Analyzer Test

1. Attach logic analyzer cable to P2. Refer to Figure 5.4.2.
2. Apply power for 3.3 volts.
3. Apply power for 32 volts.
4. Set up logic analyzer. Set each channel according to the table below, Table 5.4.2.

Signal	Pin
SWPS2	1
SWPS3	2
LDO1	3

Signal	Pin
LDO2	4
Pos-Neg Converter	5

Table 5.4.2 Pin assignment for logic analyzer

5. Run FPGA.
6. Record results in log found below, Table 5.4.4.

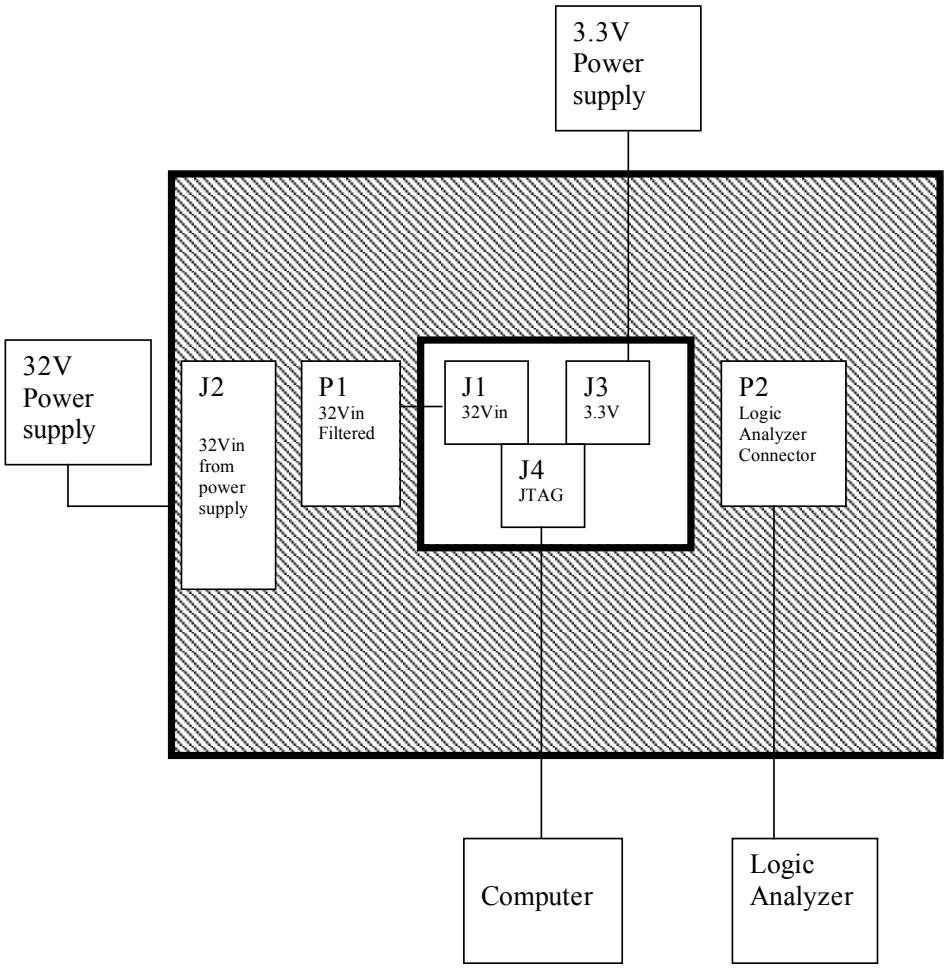


Figure 5.4.2 Test Setup

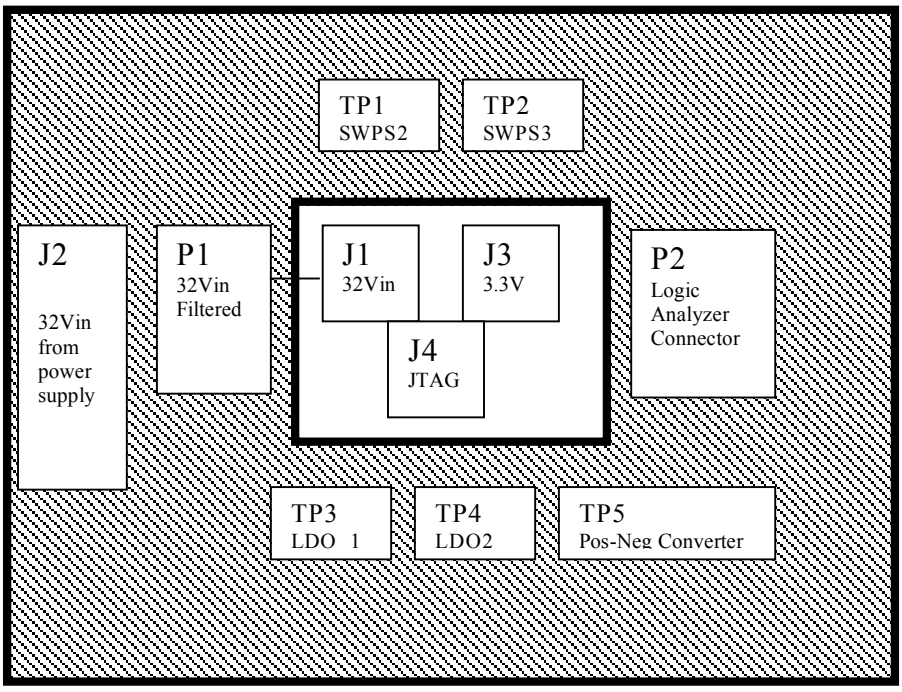


Figure 5.4.3 Test Points

Results

Record results from above tests

Test Point	T1	T2	T3	T4	T5
Voltage					
Ripple Vol.					
Rise time					

Table 5.4.3 Oscilloscope Test Results

Signal	Time when Logic 1
SWPS2	
SWPS3	
LDO1	
LDO2	
Pos-Neg Converter	

Table 5.4.4 Logic Analyzer Test Results

5.5 Demonstration

For demonstration purposes the timing of the power sequence will be longer in order to visually see the change in sequence. The power signals will be wired to LEDs on the test card. The LEDs will turn on sequentially. Each LED will indicate a different power line. A logic analyzer will be difficult to take out of the lab to use for demonstration. The logic analyzer when in the lab will prove that the power sequence is following the specified timing.

6 - Facilities

The Senior Design Lab will be the primary location for designing and testing the equipment and circuit board. The PCB will be manufactured at Lockheed Martin. Specific parts will be mounted at the facility as well. Remaining parts will be mounted in the Senior Design Lab. A spectrum analyzer, oscilloscope, and power supplies will be available in the lab. The remaining equipment that will be needed will be provided by Electrodynamics Associates and Lockheed Martin. Below is a list, Table 6.1.1, of equipment that will be used for testing and using for support in running the board.

Equipment
Oscilloscope
Logic Analyzer
JTAG FPGA interface
Power supplies
Computer
ESD mat

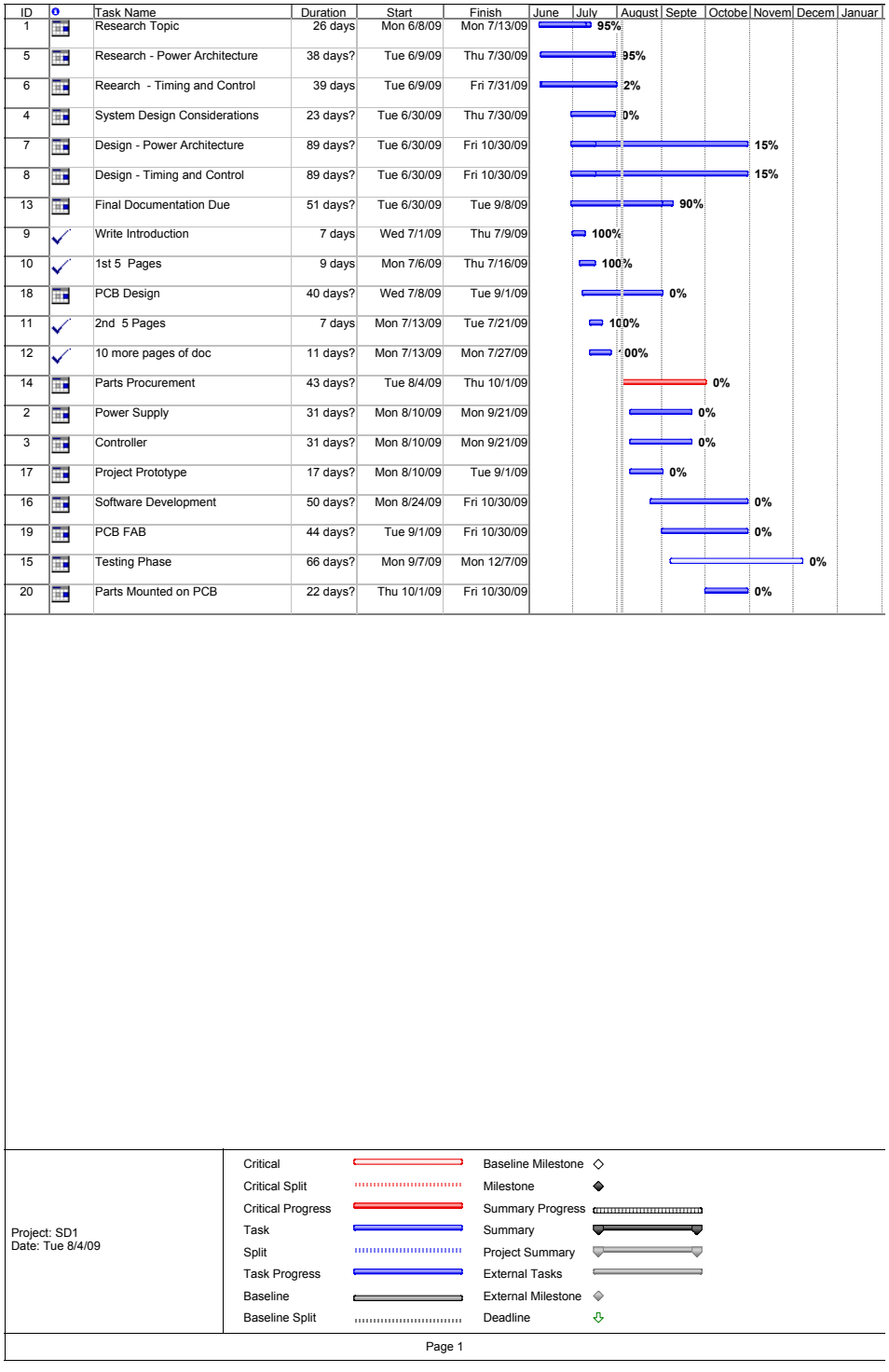
Table 6.1.1 Equipment for testing

7 - Budget and Milestone Chart

7.1 Budget

Description	Qty	Unit Price	Cost
Linear Technologies LT1963 Linear Regulator	4	$10.00	$40.00
Linear Technologies LT4612 Switching Power Supply	3	$60.00	$180.00
FPGA Actel Fusion AFS250-QN180I	1	$70.40	$70.40
Actel Fusion Starter Kit	1	$500.00	$500.00
Resistors	15	$5.00	$75.00
Capacitors ST205C276MAJ03 TTI Inc 1 PKG	1	$15.00	$15.00
Connectors	2	$30.00	$60.00
EMI Filter	1	$20.00	$20.00
Voltage Attenuator	4	$20.00	$80.00
Capacitor Convertor	2	$2.00	$4.00
			$0.00
		Total	**$1,044.40**

7.2 Milestone Chart



ID	Task Name	Duration	Start	Finish
1	Research Topic	26 days	Mon 6/8/09	Mon 7/13/09
5	Research - Power Architecture	38 days?	Tue 6/9/09	Thu 7/30/09
6	Reearch - Timing and Control	39 days	Tue 6/9/09	Fri 7/31/09
4	System Design Considerations	23 days?	Tue 6/30/09	Thu 7/30/09
7	Design - Power Architecture	89 days?	Tue 6/30/09	Fri 10/30/09
8	Design - Timing and Control	89 days?	Tue 6/30/09	Fri 10/30/09
13	Final Documentation Due	51 days?	Tue 6/30/09	Tue 9/8/09
9	Write Introduction	7 days	Wed 7/1/09	Thu 7/9/09
10	1st 5 Pages	9 days	Mon 7/6/09	Thu 7/16/09
18	PCB Design	40 days?	Wed 7/8/09	Tue 9/1/09
11	2nd 5 Pages	7 days	Mon 7/13/09	Tue 7/21/09
12	10 more pages of doc	11 days?	Mon 7/13/09	Mon 7/27/09
14	Parts Procurement	43 days?	Tue 8/4/09	Thu 10/1/09
2	Power Supply	31 days?	Mon 8/10/09	Mon 9/21/09
3	Controller	31 days?	Mon 8/10/09	Mon 9/21/09
17	Project Prototype	17 days?	Mon 8/10/09	Tue 9/1/09
16	Software Development	50 days?	Mon 8/24/09	Fri 10/30/09
19	PCB FAB	44 days?	Tue 9/1/09	Fri 10/30/09
15	Testing Phase	66 days?	Mon 9/7/09	Mon 12/7/09
20	Parts Mounted on PCB	22 days?	Thu 10/1/09	Fri 10/30/09

Project: SD1
Date: Tue 8/4/09

Critical		Baseline Milestone	◇
Critical Split		Milestone	◆
Critical Progress		Summary Progress	
Task		Summary	
Split		Project Summary	
Task Progress		External Tasks	
Baseline		External Milestone	◆
Baseline Split		Deadline	⇩

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8 - Design Summary

Lockheed Martin needed a more efficient and smaller power supply for their JAGM missile. As there are always room for improvement in any system, they wanted to challenge this group of seniors in anticipation that they would come up with a better design than what is existing. With limited knowledge, the group may be able to think “outside the box.” Often, engineers in a company concentrate on only one aspect of the project. In this instance, the students would be challenged to cover all boundaries themselves. This gives them a chance to see loopholes between sections of the project that were possibly not seen previously. The initial challenge was to divide and conquer the project amongst the senior design group members. There were two main aspects of the project, timing control and the power architecture. The main goal between the two aspects was to be able to fit all the parts onto one card . This goal was met and new parts that are more advanced were introduced to the new power supply, making the circuit card more advanced than the previously designed.

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10.2 Permissions

Linear Technology

Priscilla Wilson to Debbie show details Jul 31 (6 days ag

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Senior Product Marketing Engineer
Power Products Group
Linear Technology Corporation
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information contained in or attached to this transmission is STRICTLY
PROHIBITED. If you have received this transmission in error, please
immediately notify me by reply e-mail, or by telephone 408-432-1900

Actel

I: Out of Office: Usage rights Inbox | X

Keith Weston to me show details Aug 6 (2 days ago) Reply

egin forwarded message:

From: "Miglioranzi, Minta E." <Minta.Miglioranzi@actel.com>
Date: July 28, 2009 4:45:40 PM EDT
To: Keith Weston <keith.weston@knights.ucf.edu>
Subject: Out of Office: Usage rights

I will be out of the office on July 27th and 28th. I will not be checking emails during this time. I will respond to you once I return on Wednesday, July 29th.

Thanks,
Minta