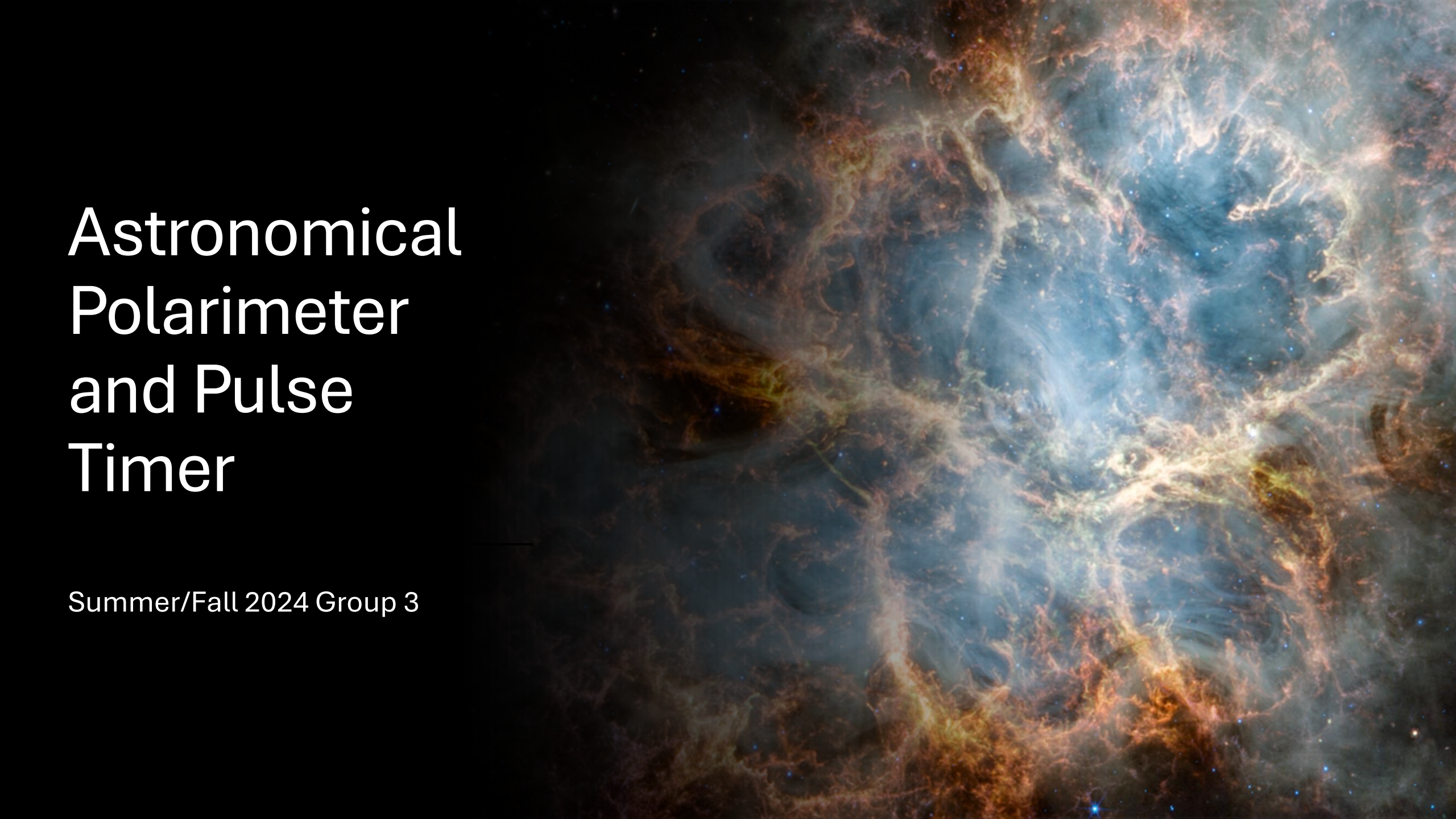
Astronomical Polarimeter and Pulse Timer



Summer/Fall 2024 Group 3

Introductions

Vincent Miller
Photonics Engineering

David Patenaude
Computer Engineering
Photonics Engineering

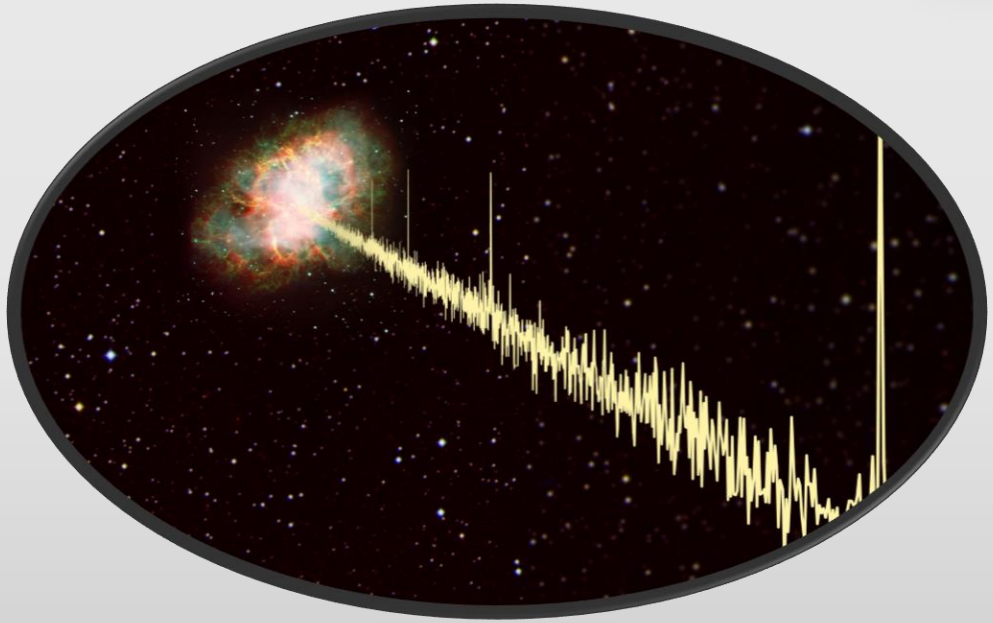
Ethan Tomczak
Electrical Engineering

David Urrego
Computer Engineering

Vincent
PSE

Project Context and Scope

- Pulsars are spinning, which changes the intensity of the emitted radiation periodically with time.
- Most are in non-visible spectrums, but some – most notably the Crab pulsar – pulse in the visible spectrum
- Their pulsing behavior remains a mystery, but by measuring the polarization, astronomers may be able to learn more about them. Primarily using the data to understand the magnetic and gravitational field dynamics.



Motivation

David U.
CpE

- The Crab Pulsar, located 7,000 light years away, provides a unique opportunity to study extreme space conditions.
- Measuring its polarization and pulse timing helps us understand its magnetic fields and rotation.
- Unlike most pulsars, it emits visible light, making optical polarimetry essential.
- Our project will capture and analyze this light, contributing to future discoveries about pulsars.

The Crab Pulsar

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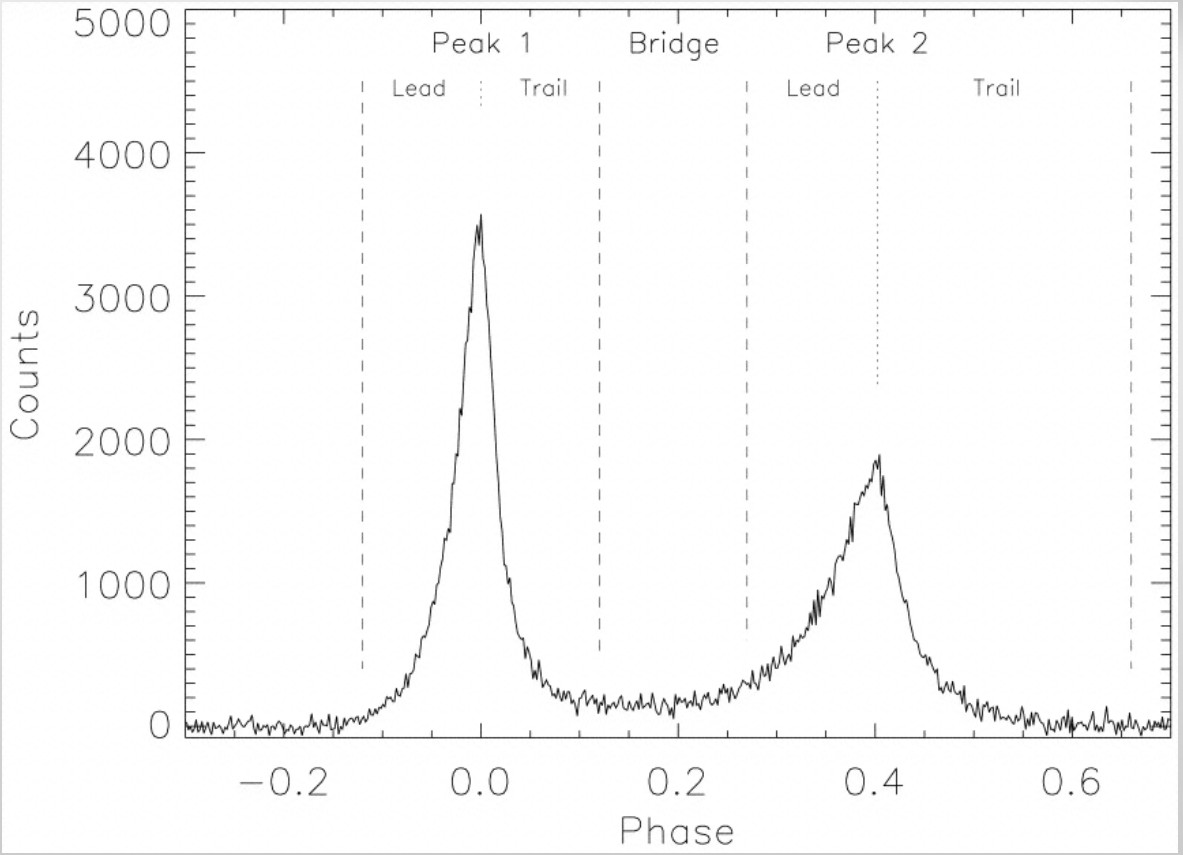
- Located in the Crab Nebula
- The brightest optical pulsar (m = 16.5), but dimmer than most regular stars
- Two distinct peaks per pulse period, and each pulse is approximately 33ms.



Crab Pulsar Pulse Profile

Our Goals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Project Goal: Our goal is to enable further study of visible-spectrum pulsars (specifically the Crab Pulsar) by creating an instrument to measure the polarization and pulse timing concurrently of the incident light.

Hierarchy of goals:

<u>Basic:</u>

- High-efficiency optical coupling and minimized power loss
- Near diffraction-limited aberrations for imaging systems
- Count pulses at 1kHz sampling
- Design and implement a power supply unit
- Implement peripherals with microcontroller

Goals


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Advanced:

- Design exit pupil imager for better telescope alignment
- Increase sensitivity of polarimeter to 1% accuracy
- Implement adjustable sampling frequency and duration with physical and software control
- Handle sampling at 250kHz in terms of data output and storage

Stretch:

- Utilize optics to minimize power loss to 5% or less
- Improve polarization measurement to 0.1% accuracy
- Full GUI program and utilize additional connections to MCU

Objectives

David P.
CpE & PSE

- To minimize light loss, capture full aperture of telescope output
- Utilize fold mirrors that move to image the telescope's pupil
- Minimize number of optics and use AR-coated optics to reduce power loss
- Use Wollaston prisms to separate light with high extinction ratio
- Implement sensitive, single-photon photodetectors to achieve high-temporal resolution
- Create regulator schemes for multiple voltages needed
- Use BNC connectors to accept detector output
- Implement a fast, large storage solution for storing samples
- Provide a HW interface for the user to adjust parameters
- Implement MCU peripherals to accomplish sampling and user input
- Make software package for processing data and providing a user interface

Overall Block Diagram

David P.
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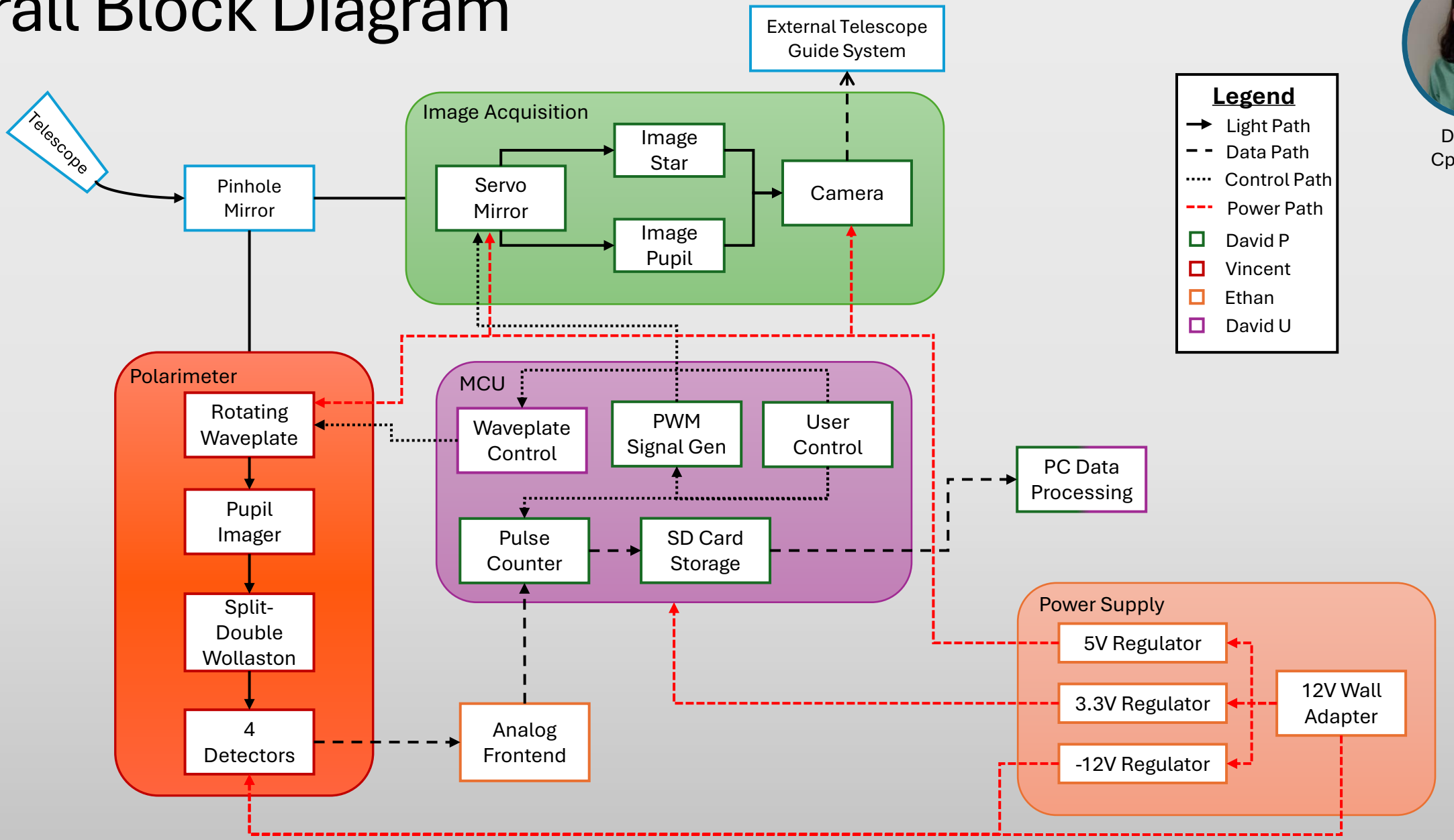

Specifications

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Number	Description	Specification
1	**Optical Power Sensitivity**	Single Photon Detection
2	**Down time between samples**	15 seconds or less*
3	**Imaging System Magnification**	Magnifications of 0.8 and 0.018
4	4 Output PSU	3.3V, 5V, ±12V
5	Sample rate of pulse counting	500 kHz
6	Minimum sample duration/time	100ms
7	Polarization Measurement	Accurate to 1°
8	External memory size	≥4GB
9	Instrument size	20”x20”x10”
10	Internal data rate capacity	At least 4 MB/s
11	Analog Frontend Speed	1 GHz or better

* Depends on sample duration

David P.
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Optical Technology Comparisons

Lookahead topics: lens types, beamsplitter types, waveplates

Lens Type Comparison

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- Singlets – single material, different shape factors
  - Cheapest, but also most aberrations
  - Good for multi-element systems where chromatic aberration not a concern
- Achromats – usually doublets, air-spaced or cemented
  - 2 materials to counteract chromatic aberration (dispersion)
  - Air-spaced has better performance, but cost goes up substantially
- Aspheric lens – non-spherical shape, harder to manufacture
  - Uses arbitrary conic constant/shape
  - Corrects spherical aberration
  - Doesn't counteract dispersion → chromatic aberration present
- Custom-designed lens
  - Paraxial lens prescription optimized in *Zemax*
  - Prescription is sent to manufacturer for custom order
  - Benefit is lens will have custom focal length, magnification, etc.
  - Downside is increased cost and time to manufacture

Lens Type Comparisons

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Common lens parameters:

Fields: 0°, 0.033° (1 arc-minute), and 0.5°
Wavelengths: F, d, C spectral lines, or 486 nm, 588 nm, 656 nm, respectively
$f = 50$ mm
$f/\# = 2$, Diameter = 25 mm
Infinite conjugate (object at infinity)

	Singlet (Plano-Convex)	Achromatic	Aspheric
RMS Spot Size (on-axis)	140 µm	13.295 µm	46.661 µm
Spherical Aberration	58.974 λ	15.848 λ	0.0532 λ
Coma Aberration	0.650 λ	0.046 λ	1.482 λ
Chromatic Aberration (Chromatic Focal Shift)	754.89 µm	151.63 µm	754.25 µm
Cost	$38.60	$89.10	$277.98
Product # (Thorlabs)	LA1255-A	AC254-050-A	AL2550-A

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Beam-Splitting Technologies

- Beamsplitter cube
  - Non-polarizing or polarizing with different split ratios
  - 10%:90% reflected/transmitted
  - AR-coated, $R_{avg} < 0.5\%$

Cube Beamsplitter
Image Credit: Thorlabs

- Beamsplitter plate
  - Non-polarizing or polarizing, various splitting ratios
  - 10:90 R:T ratio
  - AR-coated back surface, $R_{avg} < 1\%$

Plate Beamsplitter
Image Credit: Thorlabs

Beam-Splitting Technology – Pinhole Mirror

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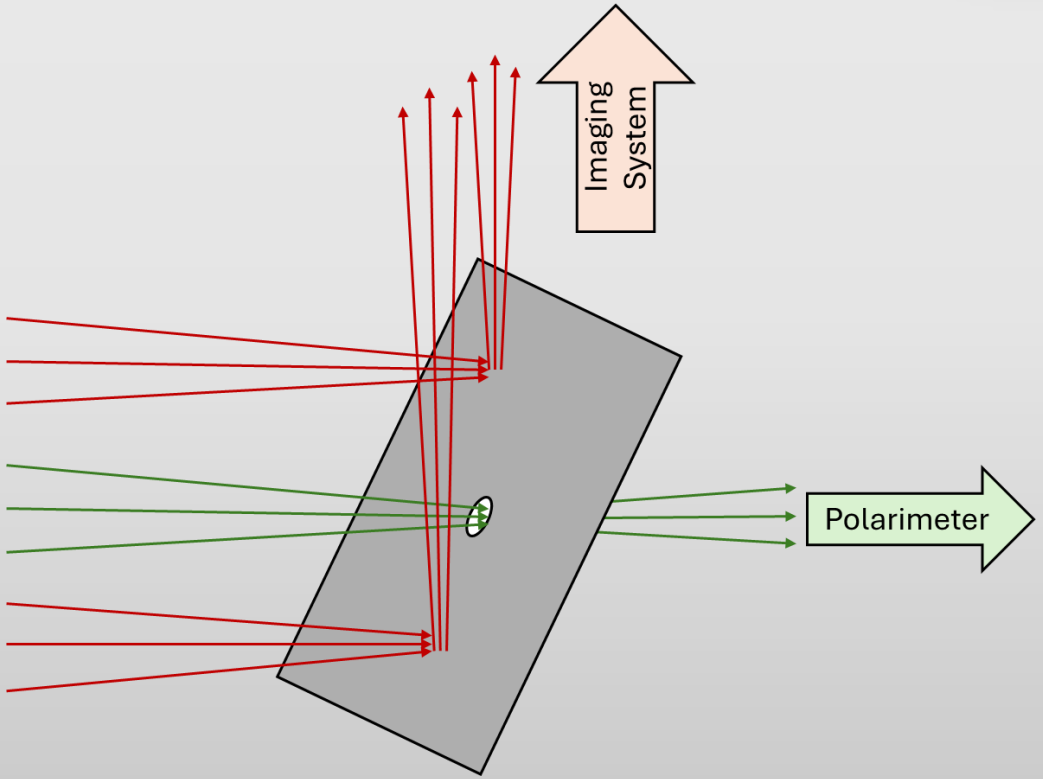
- A metallic mirror with a pinhole etched into the center, to allow a specific object to pass through (green).
- All other light is reflected (red)
- Splits light between guiding and polarimetry systems with minimal loss.



Beamsplitter Technology Comparison

David P.
CpE & PSE

Commonalities between technologies:

- Same splitting ratio: 10:90 reflection/transmission (R:T)
- Same size / form factor

	Cube	Plate	Pinhole Mirror
Angle of Incidence	0°	45°	45°
Power Loss	< 15%	< 1%	< 1% (or zero)
Polarization Deviation	$\lvert T_s - T_p \rvert < 10\%$ $\lvert R_s - R_p \rvert < 10\%$	$\lvert T_s - T_p \rvert < 35\%$ $\lvert R_s - R_p \rvert < 35\%$	None*
Cost	$205.50	$140.17	Materials
Part Number (Thorlabs)	BS037	BSN10	-

*Note: the pinhole in a mirror is empty space (air), so on-axis light passes through unimpeded, experiencing no change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Waveplate Technologies

- Wavelength dependent retardance error is a critical issue, so we must use an achromatic waveplate. Must work for the full visible spectrum.
- Products of the chosen technology were all roughly equal in price and spectral range. Retardance error determined the final decision.

	Liquid Crystal Variable	Multi-Order	Achromatic
Retardance Error (Single Wavelength)	λ/20	λ/4	λ/300
Retardance Error (Wavelength Dependent)	>λ	>λ	λ/20
Spectral Range	350 – 700nm	Single Wavelength	350 - 850nm
Cost	$1,300	$500	$1,000
Can Be Electrically Modulated	Yes	No, requires mechanical rotation	No, requires mechanical rotation
Part Number (Thorlabs)	LC1611-A	WPMQ05M-633	AHWP10M-580


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Photodetectors

- Imaging:
  - Monochromatic CCD
  - 4µm pixel size

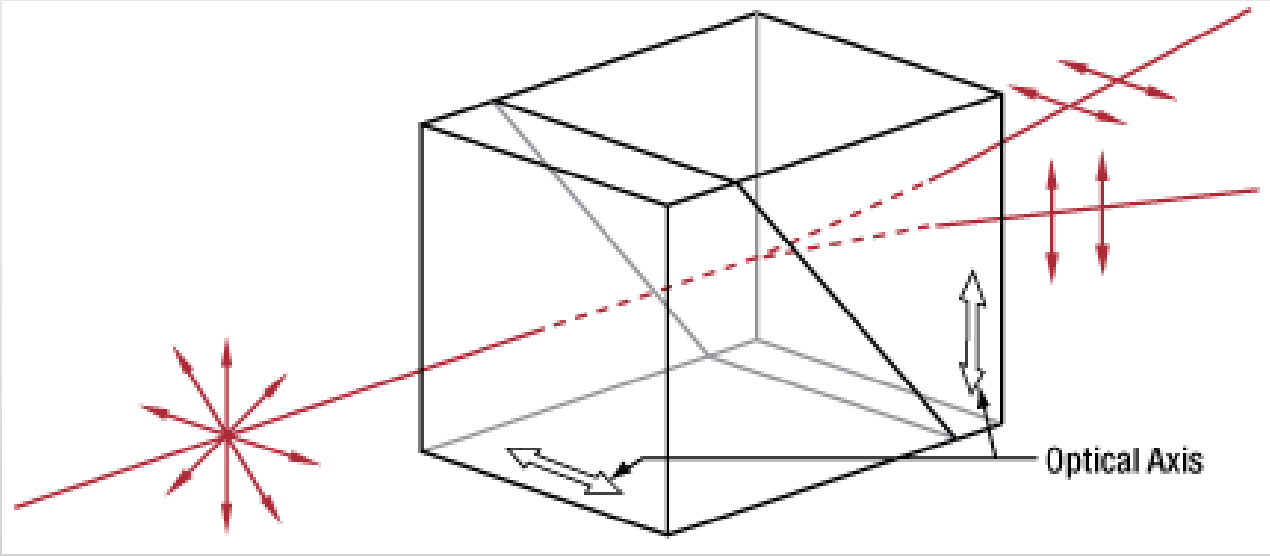
- Polarimeter:
  - Silicon Photomultiplier single photon counters
  - Cost was the primary determining factor
  - 1.3mm active area

ASI220MM Mini(mono)

PDA44

Wollaston Prisms

- Two Calcite wedges with optic axes perpendicular to each other.
- Produces O and E rays from a singular input beam.
- We've chosen these as a replacement for our original design choice, which was unavailable.



Ethan
EE

Hardware Comparisons

Lookahead topics: regulators, MCU, storage

Hardware Design: Component Selection and Comparison

Ethan
EE

Main HW components required:

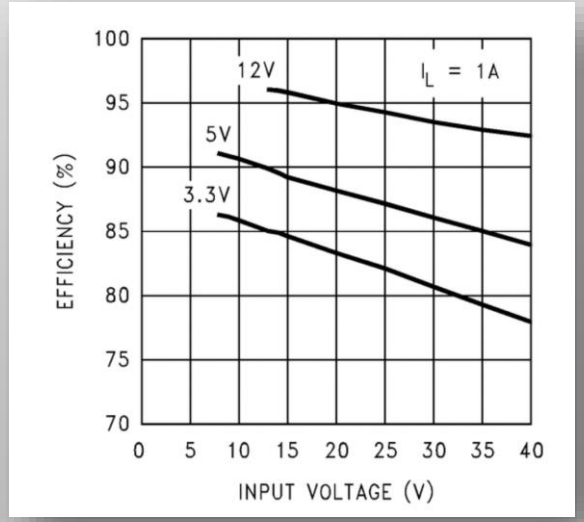
MCU for control & data acquisition; must have clock and ADC sampling rate that meet performance requirements

(>1 MHz clock frequency & >1MSPS ADC frequency). MCU processor we found was the ESP32_MINI-1U

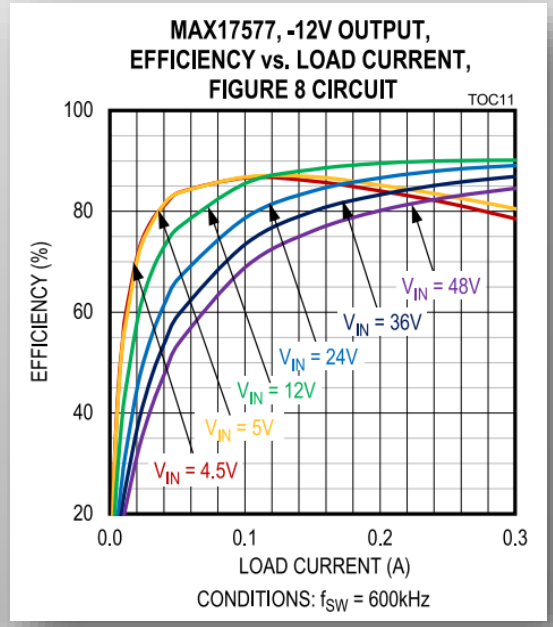
- 40 MHz internal crystal oscillator (Stable)
- ADC up to 2 MSPS (Plenty of headroom)

Use switching regulator to achieve all required voltages needed by system, 3.3V for MCU, 5V for servo & rotation mount, and ±12V for sensors and OA scheme.

- 3.3V and 5V utilize LM2675-ADJ (low frequency switching regulator with 1A max o/p current)
- -12V utilize MAX17577 (meant for inverting and provides sufficient 0.3A max o/p current)



LM2675-ADJ typical performance



Hardware Selection and Comparison

Ethan
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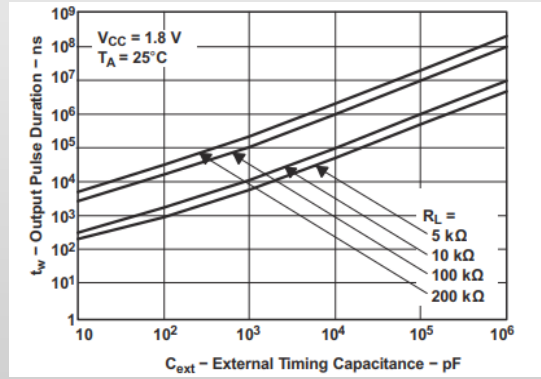
Additional hardware requirements:

- Controls and Display; start and menu select buttons, & rotary encoder
- Sensor input and analog processing; Op-Amps(OA): Going for low-noise and precision op-amps. Tested with TL084, project will utilize OPA140 for the prototype. Op-Amps used for the pulse counter in the final version were the OPA837, which is a GHz bandwidth amplifier allowing for our small signal 4ns pulse at 5 kHz. Additionally, the pulse counter includes a LMV7219 High-speed comparator for noise filtering, and a SN74LVC1G123 Schmitt Trigger to create pulse extension.

Supply Voltage (V_S)	±5 or 10	V
Input Offset Voltage	±0.5 (typ), ±3.5 (max)	mV
Input Bias Current	0.8 (typ), 3 (max)	µA
Input Voltage Noise Density	0.85	nV/√Hz
Input Current Noise Density	2.5	pA/√Hz
Gain Bandwidth Product	3.9	GHz
Slew Rate	480	V/µs

OPA847 Specs



SN74LVC1G123 Pulse width extension chart

t_r	Output rise time	10% to 90%	2.5	ns
t_f	Output fall time	90% to 10%	2	ns

LMV7219 Output signal Rise and Fall time

FPGA vs. MCU Technologies

David U.
CpE

- FPGA
  - Highly customizable and support parallel processing
  - Great for real-time signal processing and low latency tasks
  - Complex development (HDLs), higher power consumption, and cost
- MCU
  - Low power consumption, ideal for use in remote locations
  - Easier and faster development with high-level languages (*C*)
  - Cost-effective with built in peripherals (ADCs, timers, etc..)
  - Suitable for real-time data acquisition with sufficient performance for our needs.
- Conclusion :
  - MCU selected due to power efficiency, cost, simplicity, and integrated peripherals, providing an optimized solution for real-time data processing

MCU Selection

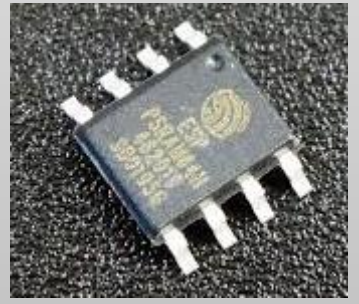
David U.
CpE

- ESP32
  - High speed ADC (2 MSPS)
  - Integrated peripherals (ADC, UART, I2C)
  - Power Management (deep sleep mode)
  - Flexible communication options (USB, UART)
  - Dual core processor (240 MHz)
- MSP430 or other MCU

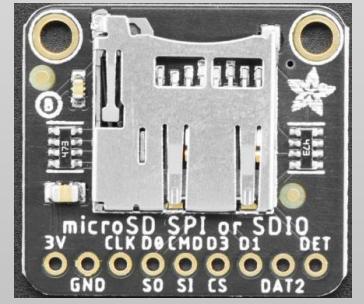
Storage: Flash vs. PSRAM vs. SD Card

David P.
CpE & PSE

- Write speeds with MCU
- Must be fast enough to handle 4MB/s of data
  - Embedded flash is slow, external flash chip likely slow as well
  - Not enough RAM to store long enough samples. External PSRAM limited to 4MB, or 1 seconds of data
  - MCU supports 4-pin SDIO protocol, exploiting parallelism. Offers plenty of removable SD card storage



PSRAM Chip
Credit: ProtoSupplies



SD Card Reader
Credit: Adafruit

Comparison of Storage Technologies

David U.
CpE

Specs	Built-in Flash	ESP-PSRAM64H (PSRAM)	MicroSD Card
Storage Size	4MB	8 MB	64 GB
Speed	40-80 MB/s	~200-400 MB/s (QSPI)	Up to 50 MB/s write (U3-rated)
Effective speed	4-8 MB/s	~50-100 MB/s	Target: 10-50 MB/s (based on 40 MHz clock with 4 lines: ~160 Mbps)
Integration method	Built-In	External (SPI/QSPI interface)	External via SDIO or SPI (removable from reader)
Cost	Included in MCU	$0.75	$12 (for two cards)

Software Technology Comparisons

David U.
CpE

- Dev environments
  - ESP-IDF : Main framework for development, providing low level hardware control and FreeRTOS integration.
  - Arduino IDE : Used for quick prototyping and basic functionality during early development
- Software Used
  - Python : Used for data analysis, visualization, and interfacing with hardware via UART.
  - C : Core language for embedded programming, memory and hardware management

Software Used

David P.
CpE & PSE

- Developer Environments:
  - Arduino IDE for simple test sketches
  - VSCode with ESP-IDF extension for native ESP32 development (in C)
  - GitHub for source control
- Design Software:
  - *Zemax* (optical design)
  - *SOLIDWORKS* (3D parts and assemblies)
  - *Fusion 360* (PCB schematics and layout)
  - *LTSpice* (circuit simulations)
- Other Software:
  - Microsoft Office
  - OneDrive
  - Discord

*Programming Languages

David U.
CpE

- Common languages: *C*, *C++*, *Java*, *Python*, *JavaScript*

Language	HW Level	Formal Structure	Object-Oriented	Scripting
C	Low	✓	✗	✗
C++	Low	✓	✓	✗
Java	High	✓	✓	✗
Python	High	✗	Can be	✓

Optical & Hardware Design

A detailed look at the polarimeter, image acquisition system, and PCB design

David P.
CpE & PSE

Optical Design

- The optical design can be broken into two parts:
    1. The Polarimeter
    2. Image Acquisition and Guide

The polarimeter separates the light into orthogonal polarizations, that can be measured to reconstruct the incoming light's polarization angle with respect to the instrument.

The image acquisition and guide system will image the object to a guide camera and feature a toggleable pupil imaging path.

Design Calculations

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- The goal is to utilize 1 camera but image 2 paths.
- Mirrors attached to servos are used to toggle which path the light takes.
- One path will image the celestial object, the other the telescope's pupil

- Gaussian lens equation, magnification, and Gullstrand's equation:

$$\frac{1}{f} = \frac{1}{u} + \frac{1}{v}$$

$$m = \frac{v}{u} = \frac{h_2}{h_1}$$

$$\frac{1}{f} = \frac{1}{f_1} + \frac{1}{f_2} - \frac{d}{f_1 f_2}$$

Paraxial Design Constraints

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- Magnification constrained to ensure images fit onto detector:
  - For object imaging path, $m = 0.863$
  - For pupil imaging path, the 1st lens $m_1 = 0.0276$, 2nd lens $m_2 = 0.6848$, giving a total of $m = m_1 \cdot m_2 = 0.0189$
- The 2 optical paths were distance constrained so that their image planes aligned at the detector.
- Focal lengths found from magnification and total distance.
- After being constrained, *Zemax* is used to optimize RMS spot size.

Zemax Layouts of the Imaging System

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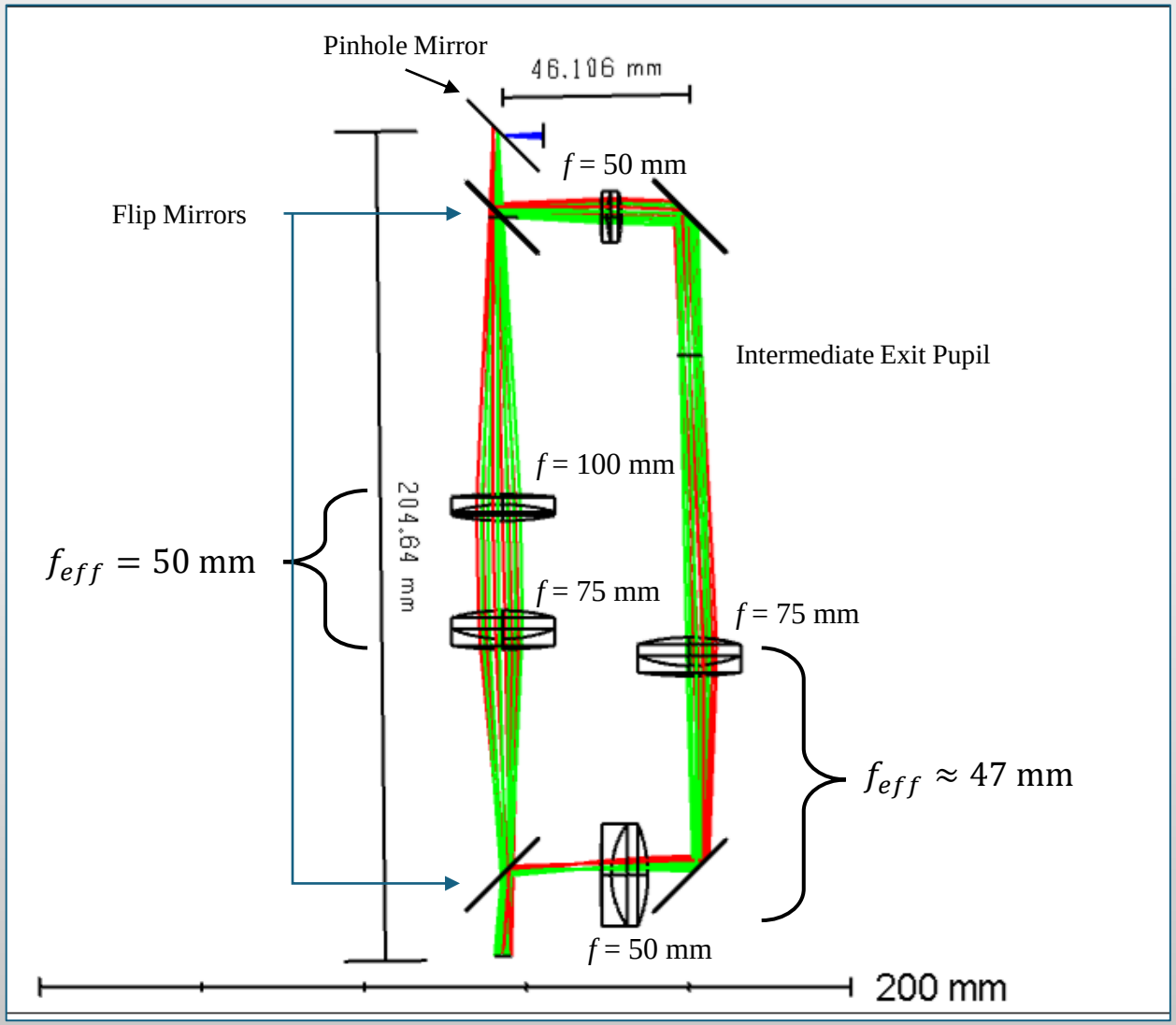
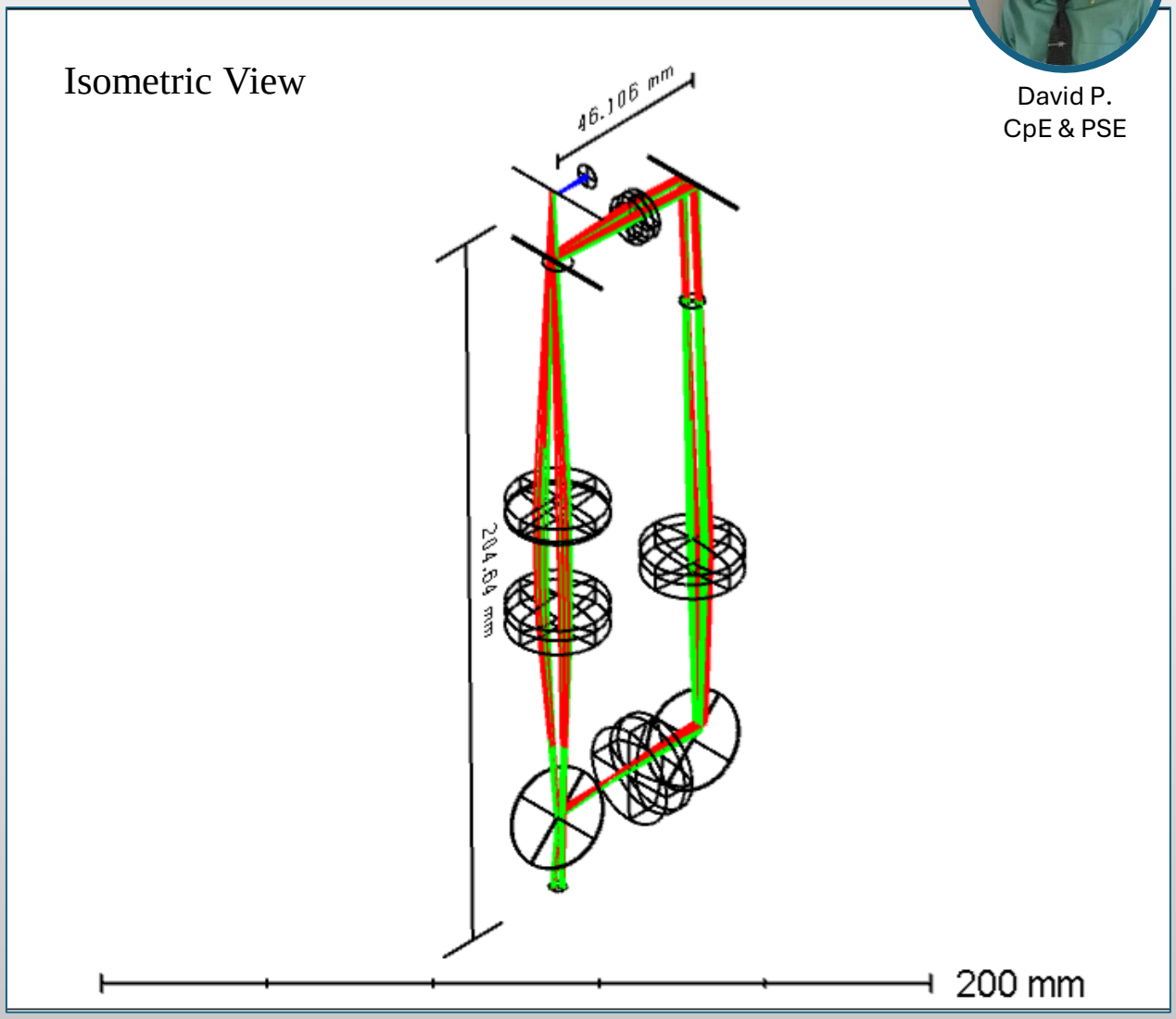


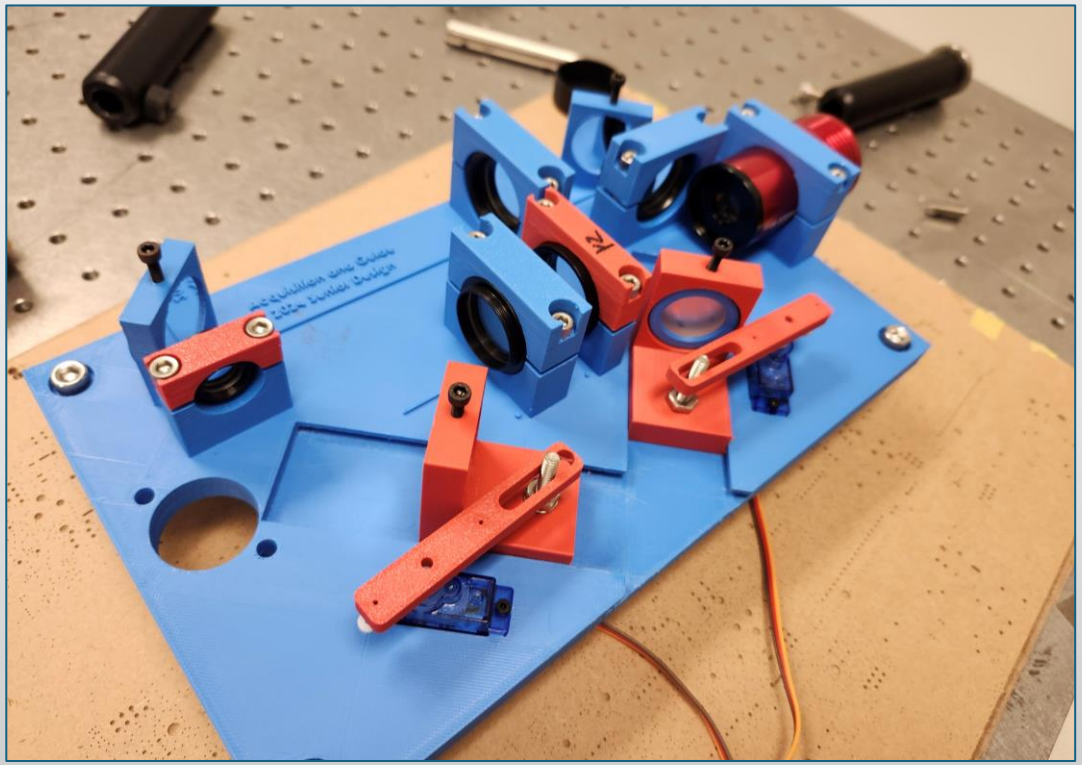


The green and red rays are the off-axis 1 and 2 arcminute fields, respectively, while the blue on-axis rays pass through the pinhole mirror.

Assembled Imaging System

David P.
CpE & PSE

Shown to the right is the 3D printed assembly for the Image Acquisition system. The base is printed so the distances can be controlled. The mounts work by compressing the mounted optics down with two M8 screws with a nut countersunk into the bottom of the plate.



Polarimeter


Vincent
PSE

- Stokes polarimeter that measures the linear polarization state of light.
- Key Components:
  - Photodetectors
  - Wollaston Prisms
  - Rotating Half Wave Plate

- The Wollaston prisms separate incoming light into two pairs of orthogonal polarization components. The photodetectors read the energy in each component.
- Rotating half wave plate used to negate instrumental polarization.

Polarimeter System Design


Vincent
PSE

- Bi-Telecentric optical system, each lens is one focal length away from the system pupil.

- System pupils are positioned at each of the four photodetectors, along with pupil splitting mirrors. Additionally, must leave enough space for all beam paths.

- Pupils must be positioned at the mirrors for precise beam splitting, and detectors for consistency in measurements.

Polarimeter Schematic

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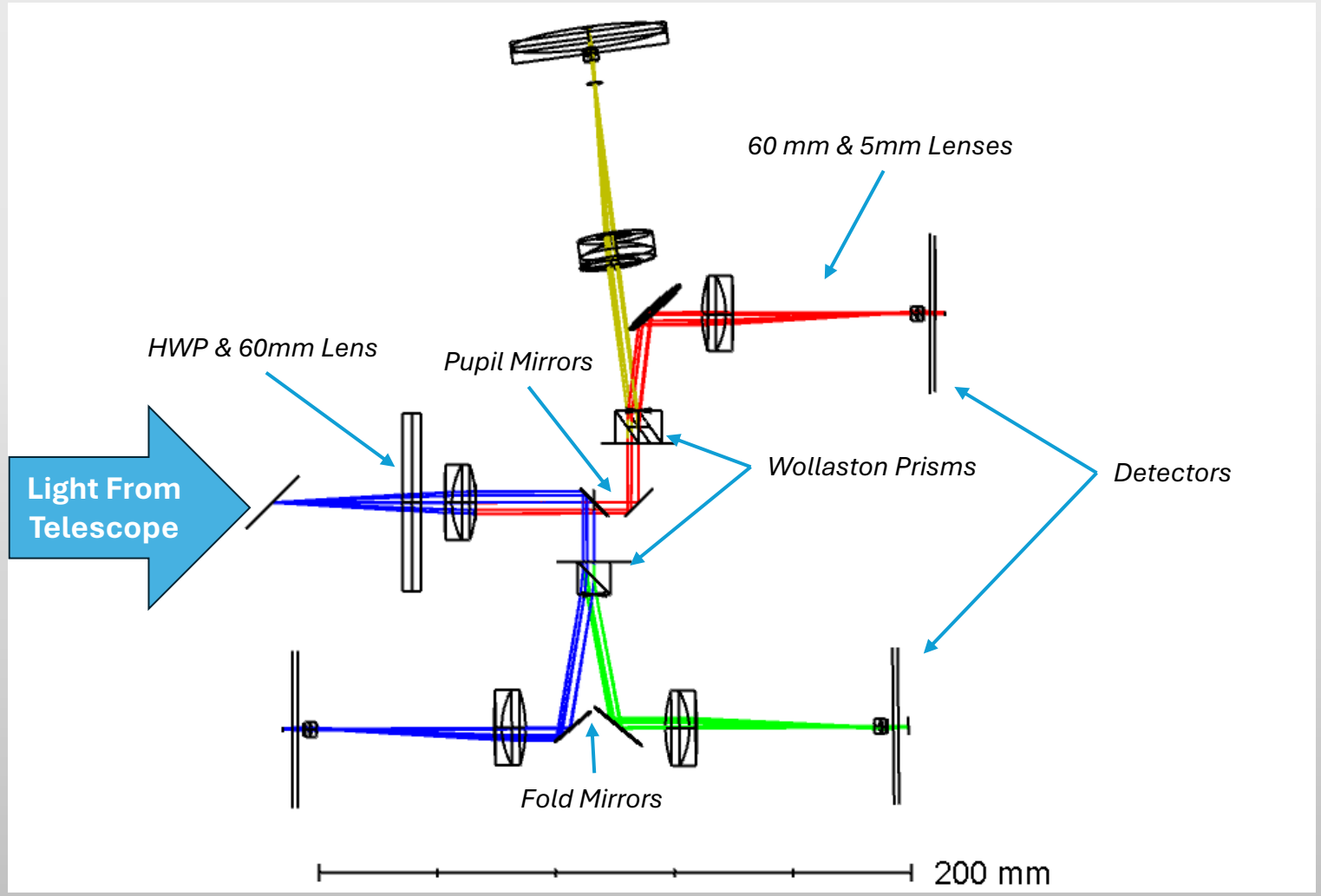
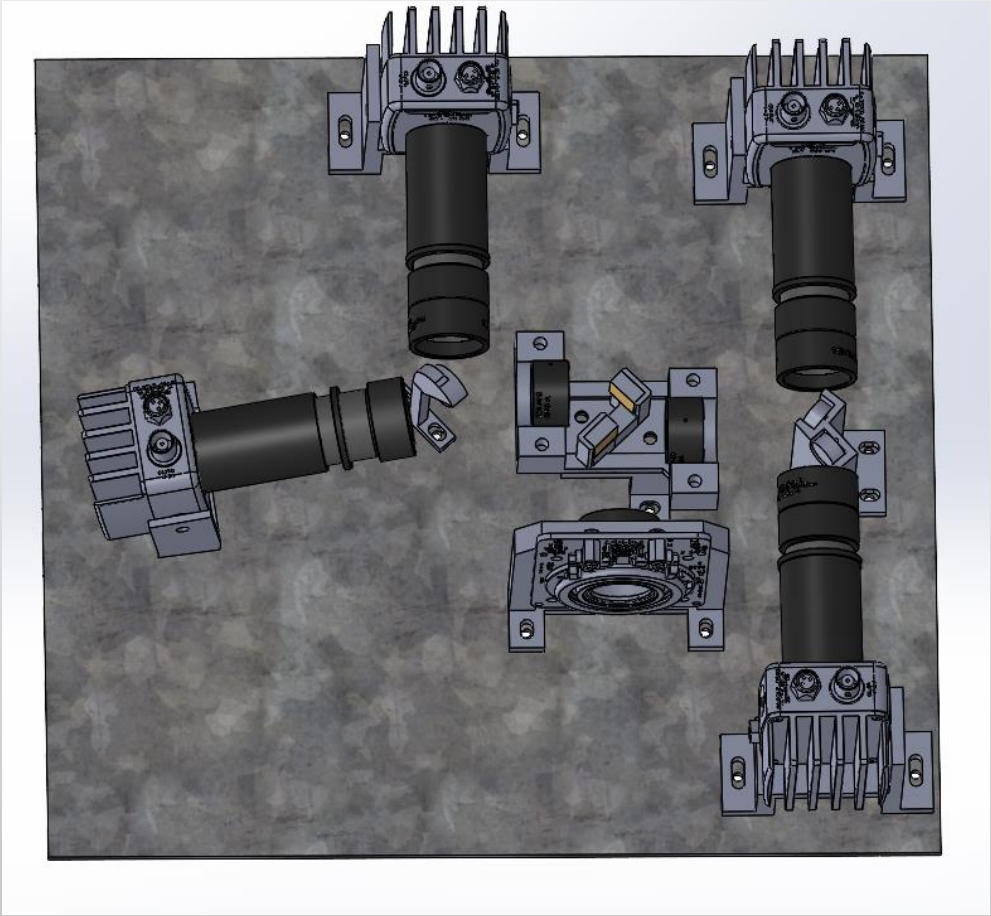
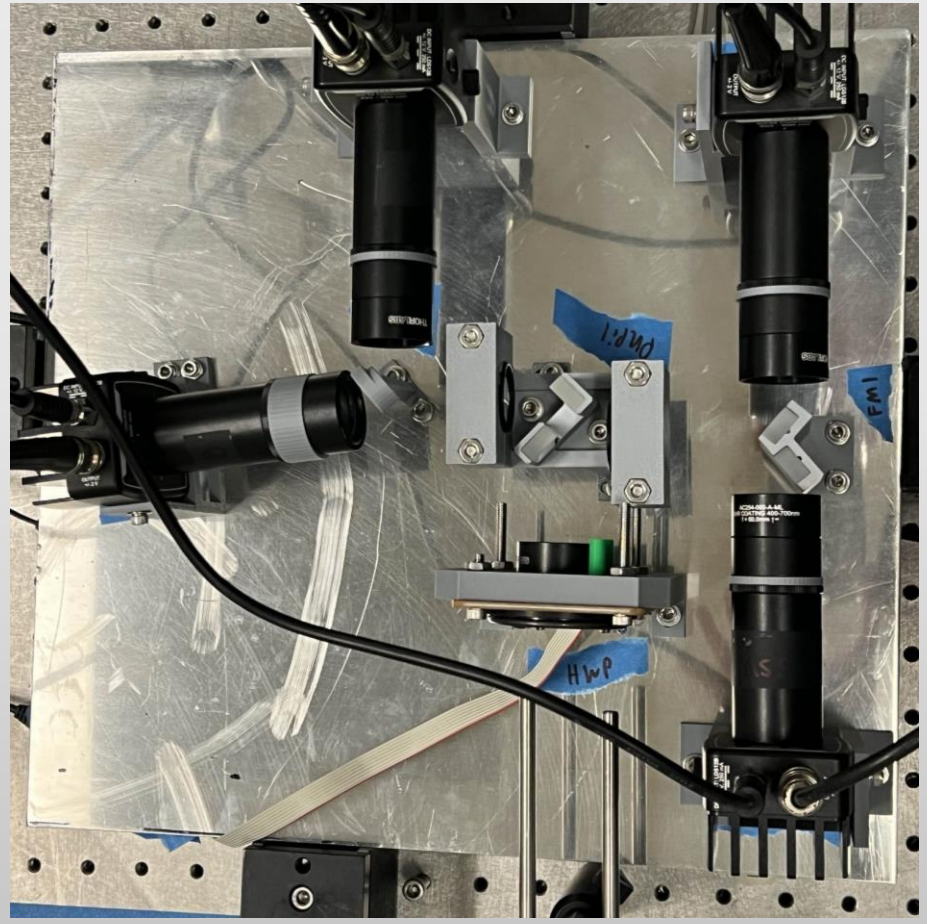


Assembled Polarimeter





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*Optical Block Diagram

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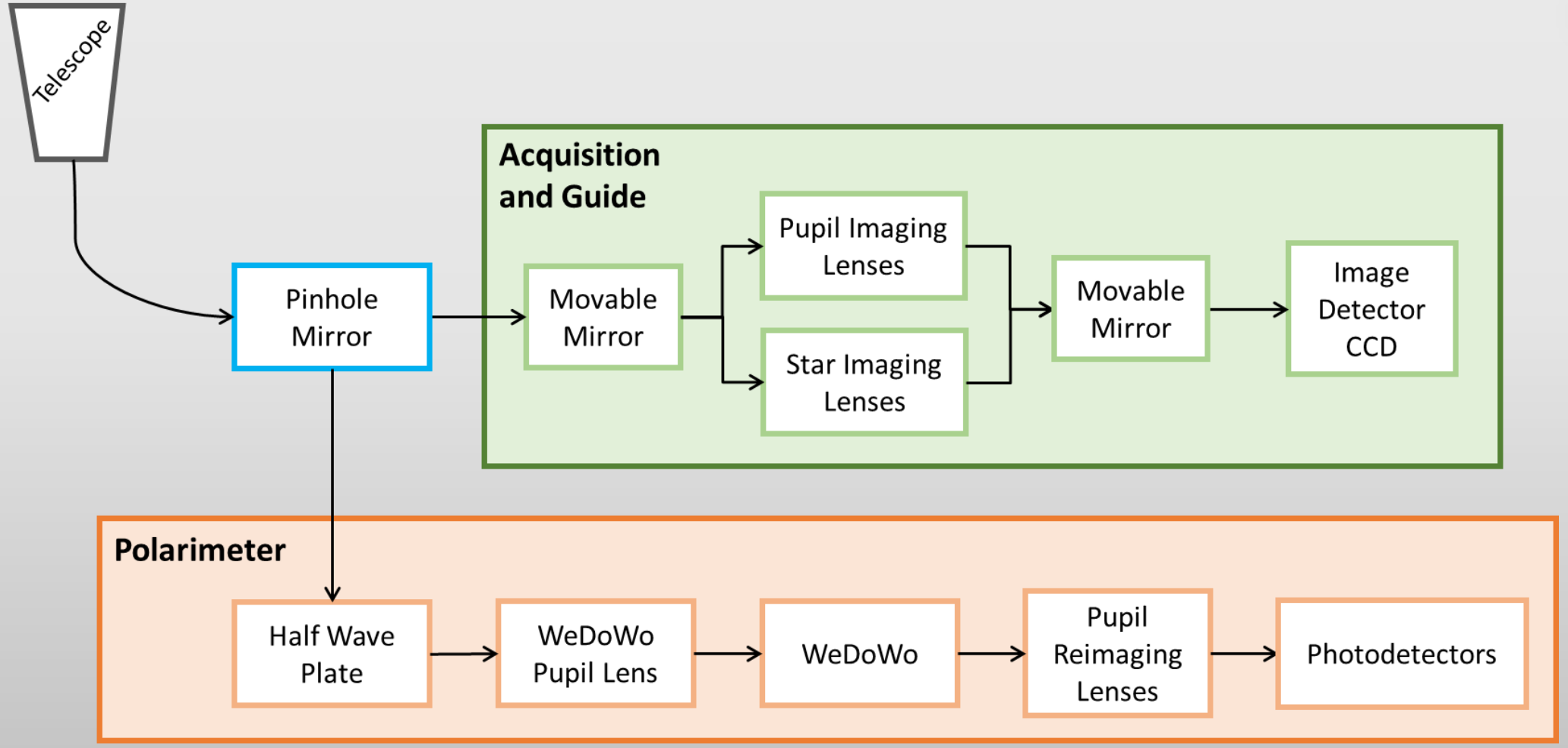


Hardware Design: Power Supply Unit (PSU)

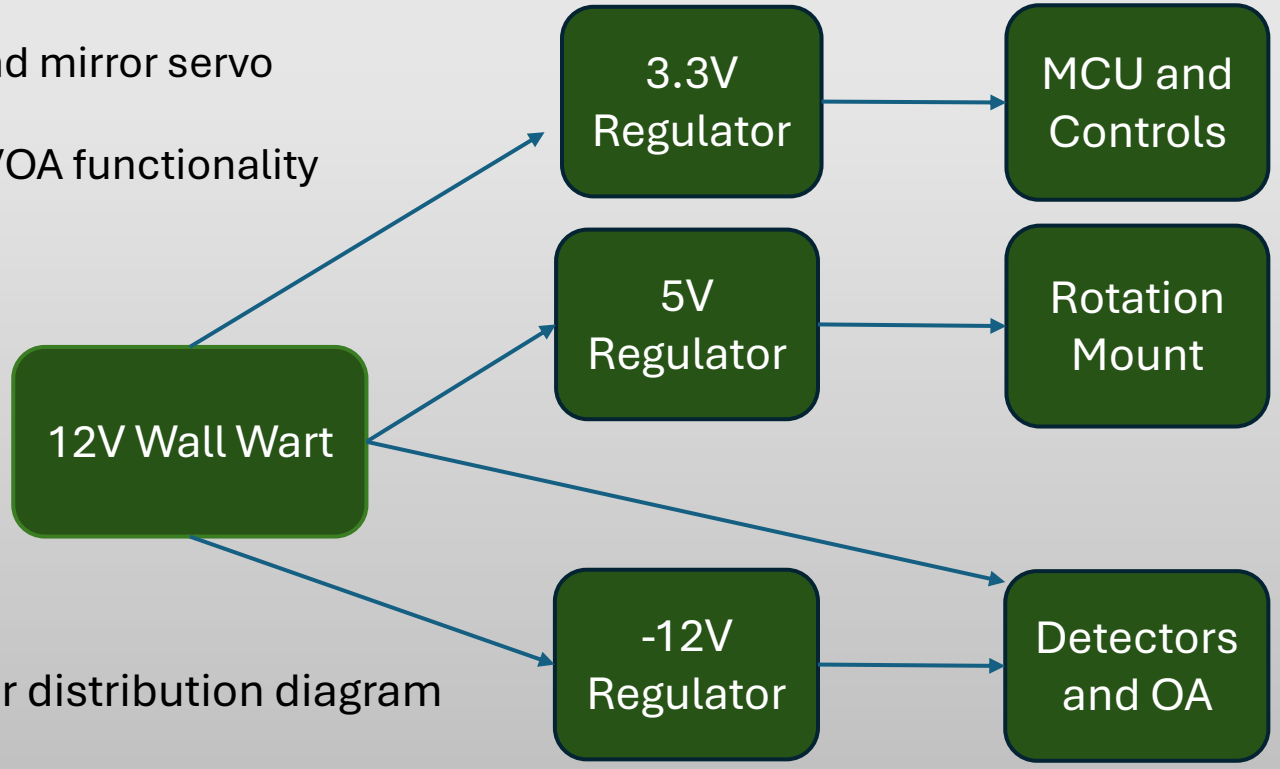
Ethan
EE

Design is to utilize a 3.3V regulator, 5V regulator, and three ±12V regulators.

All power is sourced from a 12V DC wall wart which can provide 5A max current output.

Required Voltages:

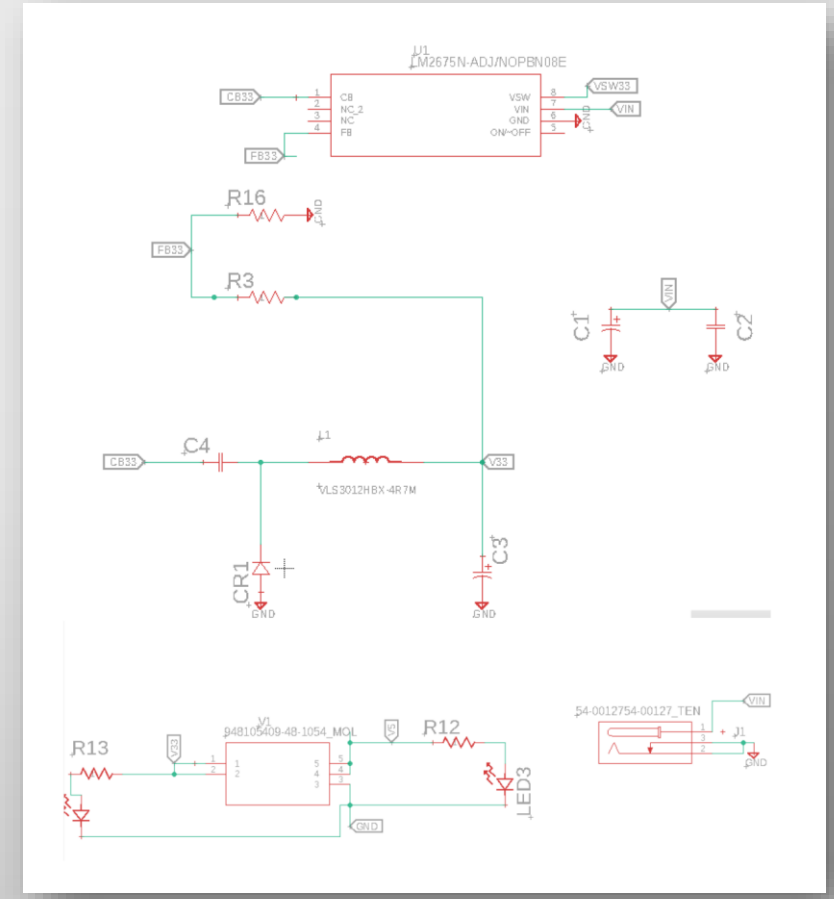
- 3.3V @ 250 mA for MCU functionality
- 5V @ 800 mA for waveplate mount and mirror servo functionality
- ±12V @ 250 mA/detector & <500 µA /OA functionality



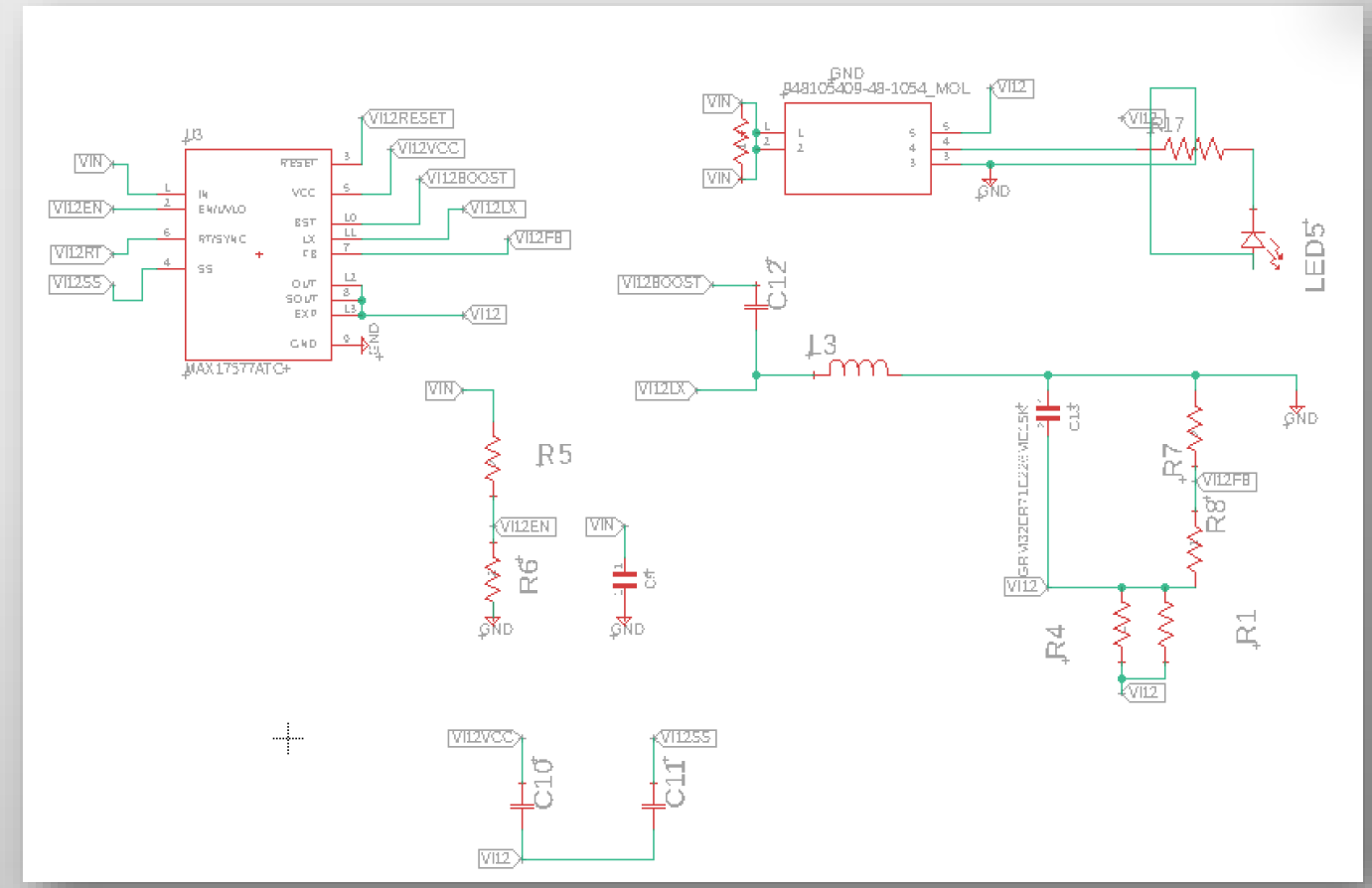
Power distribution diagram

Hardware Design: PSU Schematics

Ethan
EE



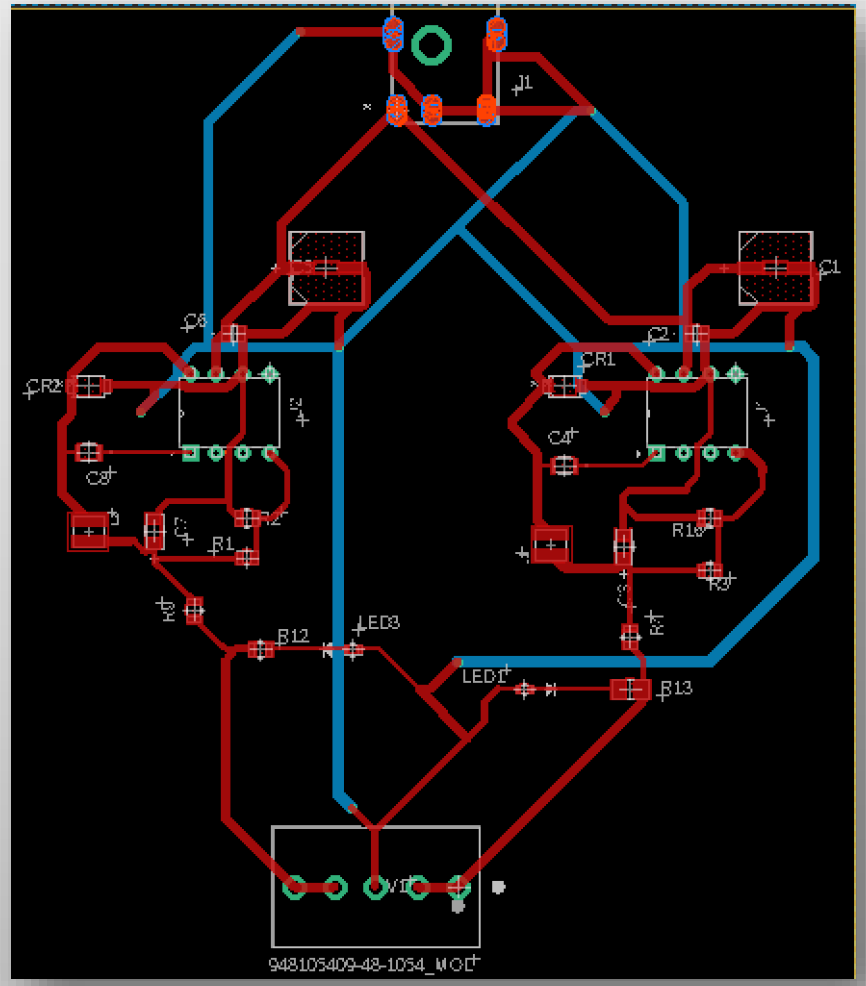
3.3V and 5V regulator scheme using LM2675-ADJ (Same topology, different feedback resistances)



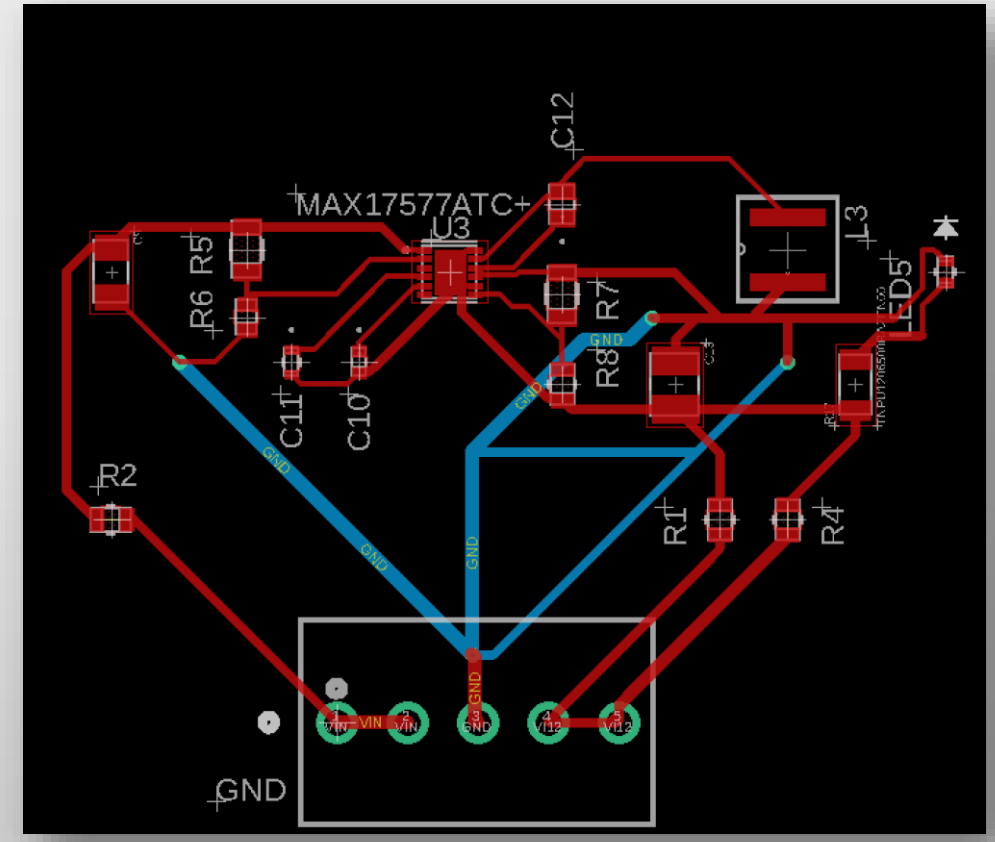
-12V regulator scheme using MAX17577

Ethan
EE

Hardware Design: PSU Layout



5V and 3.3V regulator layout

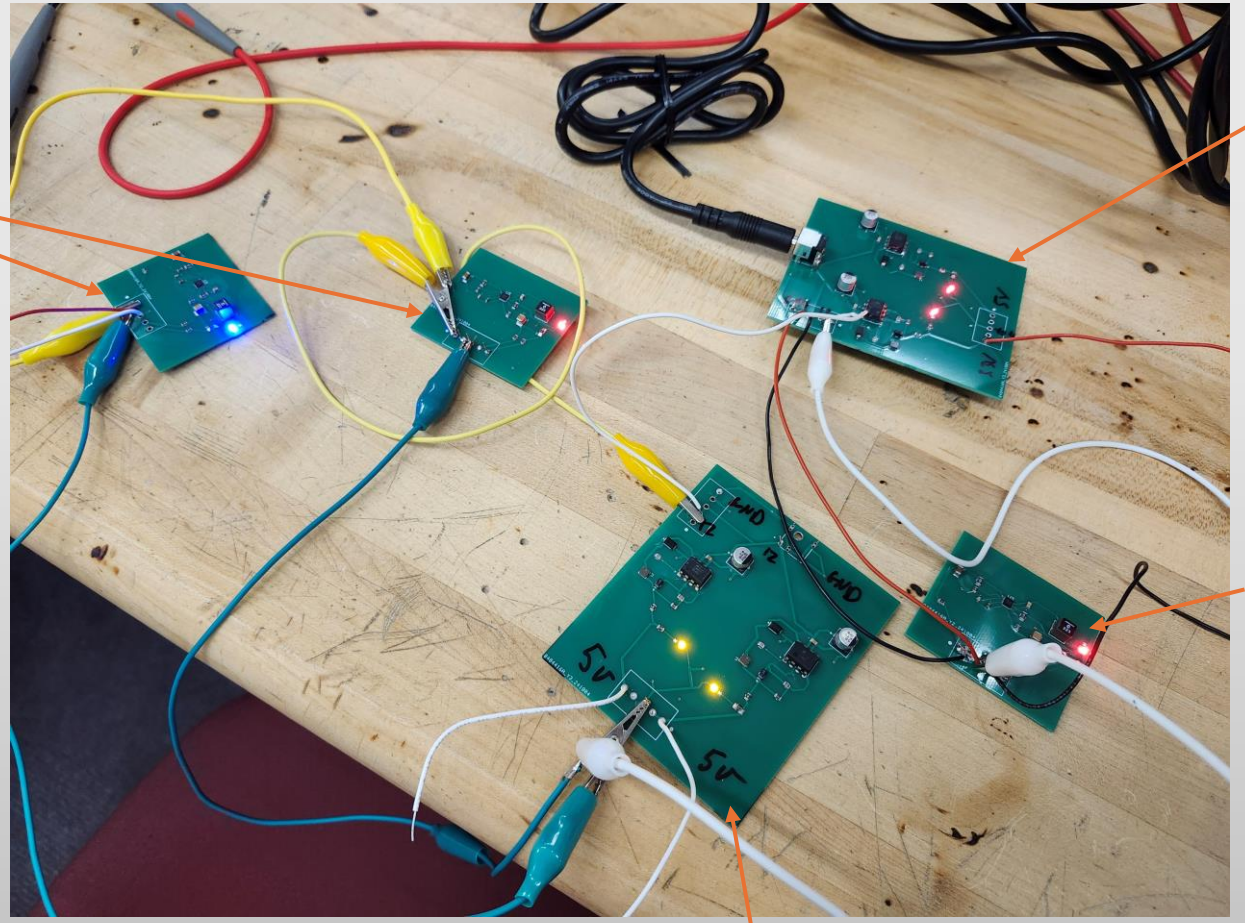


-12V inverting regulator layout

Ethan
EE

Assembled PSU PCBs

-12V Inverting Regulators



3.3V and 5V Regulators

-12V Inverting Regulator

Two 5V Regulators

Hardware Design: MCU and Peripheral Boards

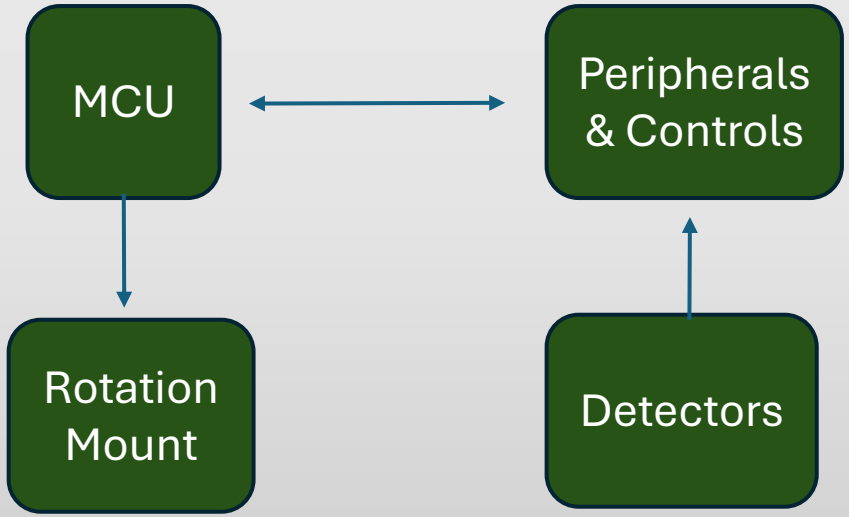
Ethan
EE

Design of the MCU board was to create a breakout board to make prototyping easier to troubleshoot. The MCU will be placed on a board which will include the following:

- USB port to serial communication using a bridge (CP2102)
- BOOT and EN buttons for flashing and start-up debugging
- Jumpers/Connection to GPIO used for sensor input to ADC, I2C communication for display, UART for terminal and waveplate communication, and rotary encoder and button controls.
- Power input

Design of external peripherals board is separate for same reason. Peripheral board must include:

- Sensor input and analog front-end (AFE)
- Start and menu buttons, rotary encoder for sampling adjustment
- Connection for rotation mount rs232 communication.
- Power Input



MCU and peripheral board implementation

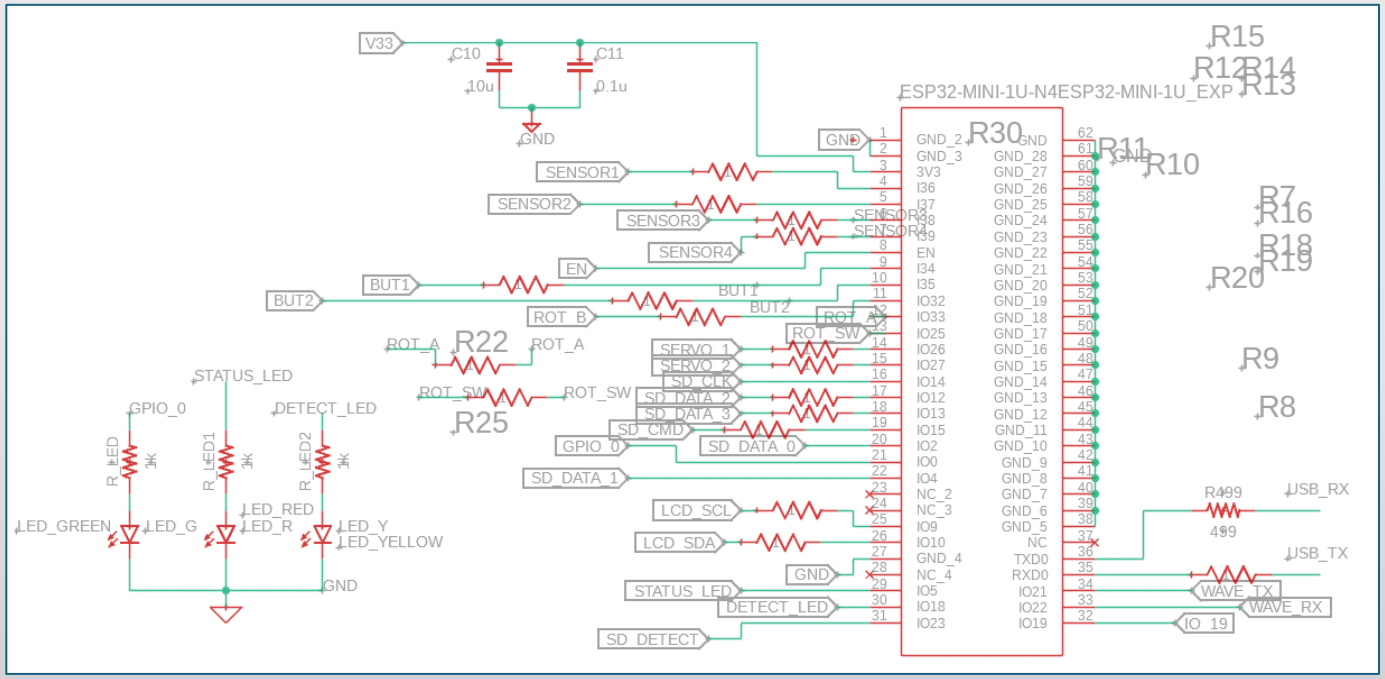
Hardware Design: MCU Breakout Board

Ethan
EE

MCU is going to be placed on separate board for troubleshooting.

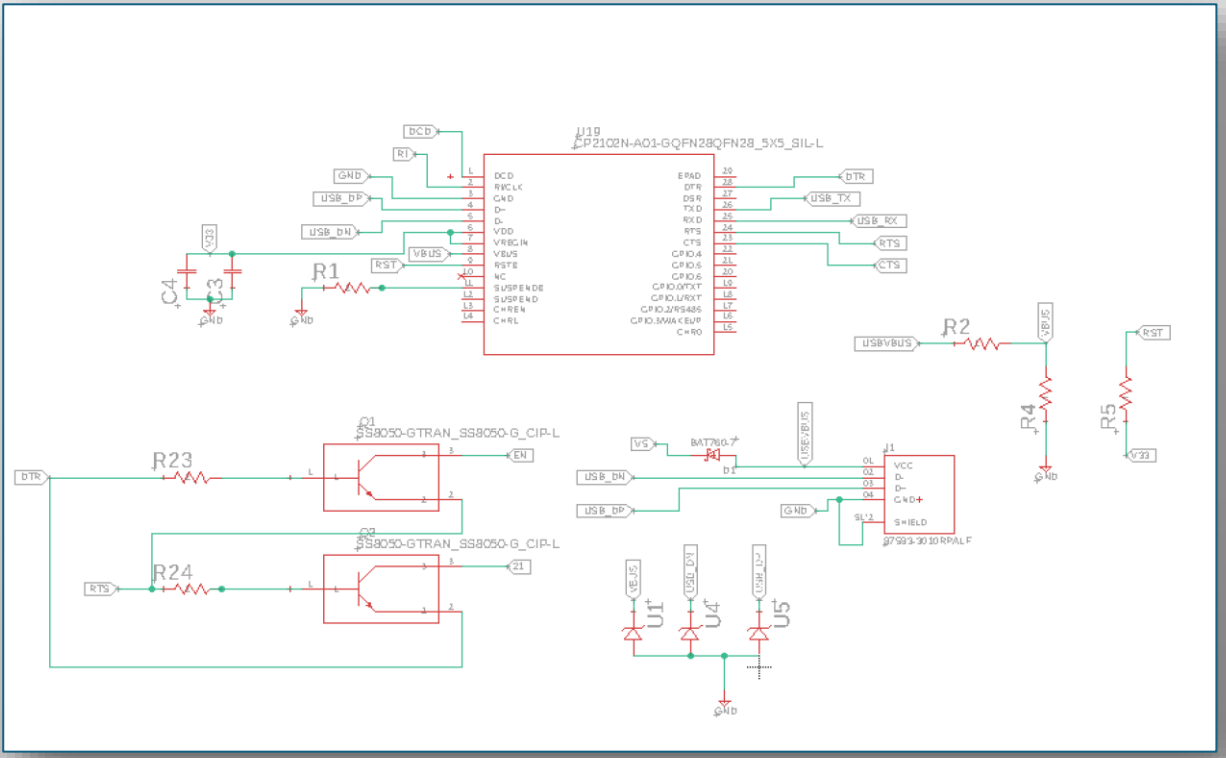
<u>MCU Breakout board must include</u>:

- USB communication for data TX/RX
- BOOT and EN buttons installed for flashing
- GPIO, power, and ground jumper ports.
- GPIO pins must have 0Ω resistor for isolation
- Connection to 3.3V power from PSU

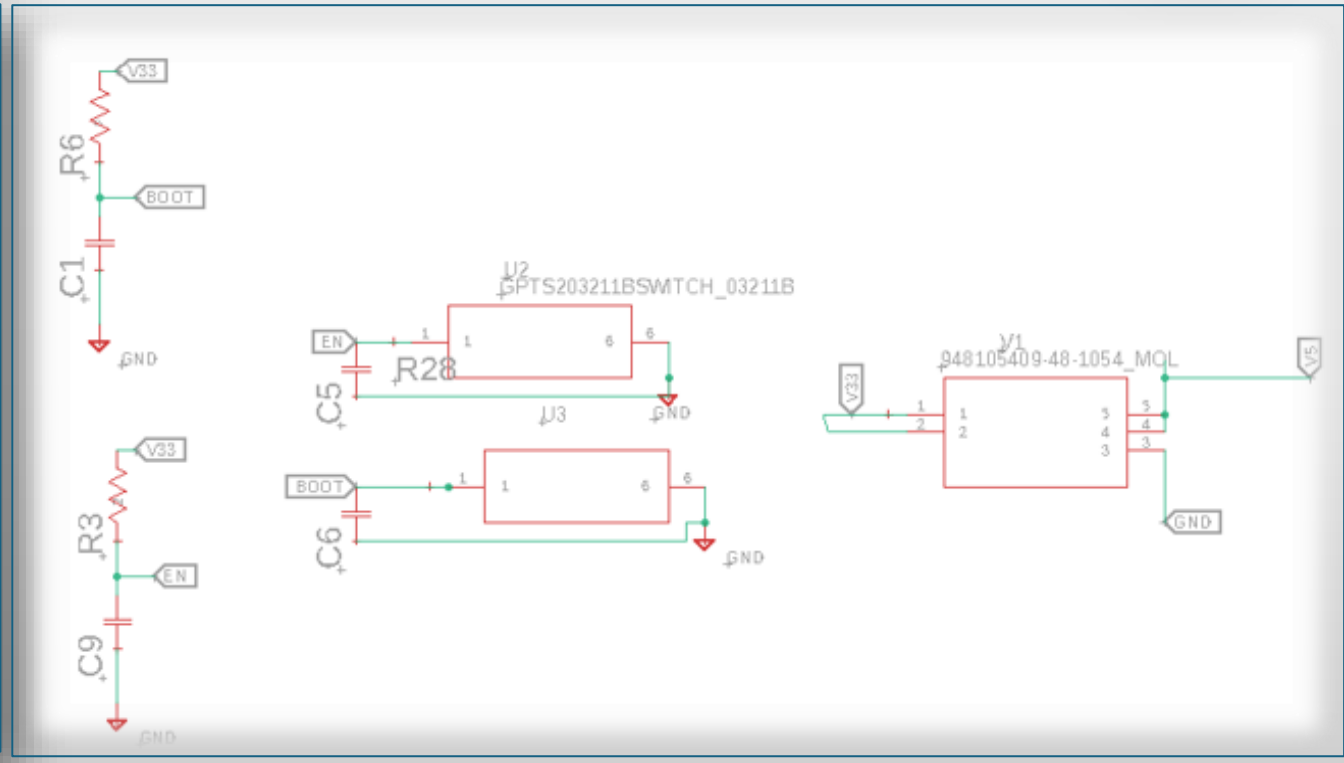


Hardware Design: MCU Breakout Board

Ethan
EE



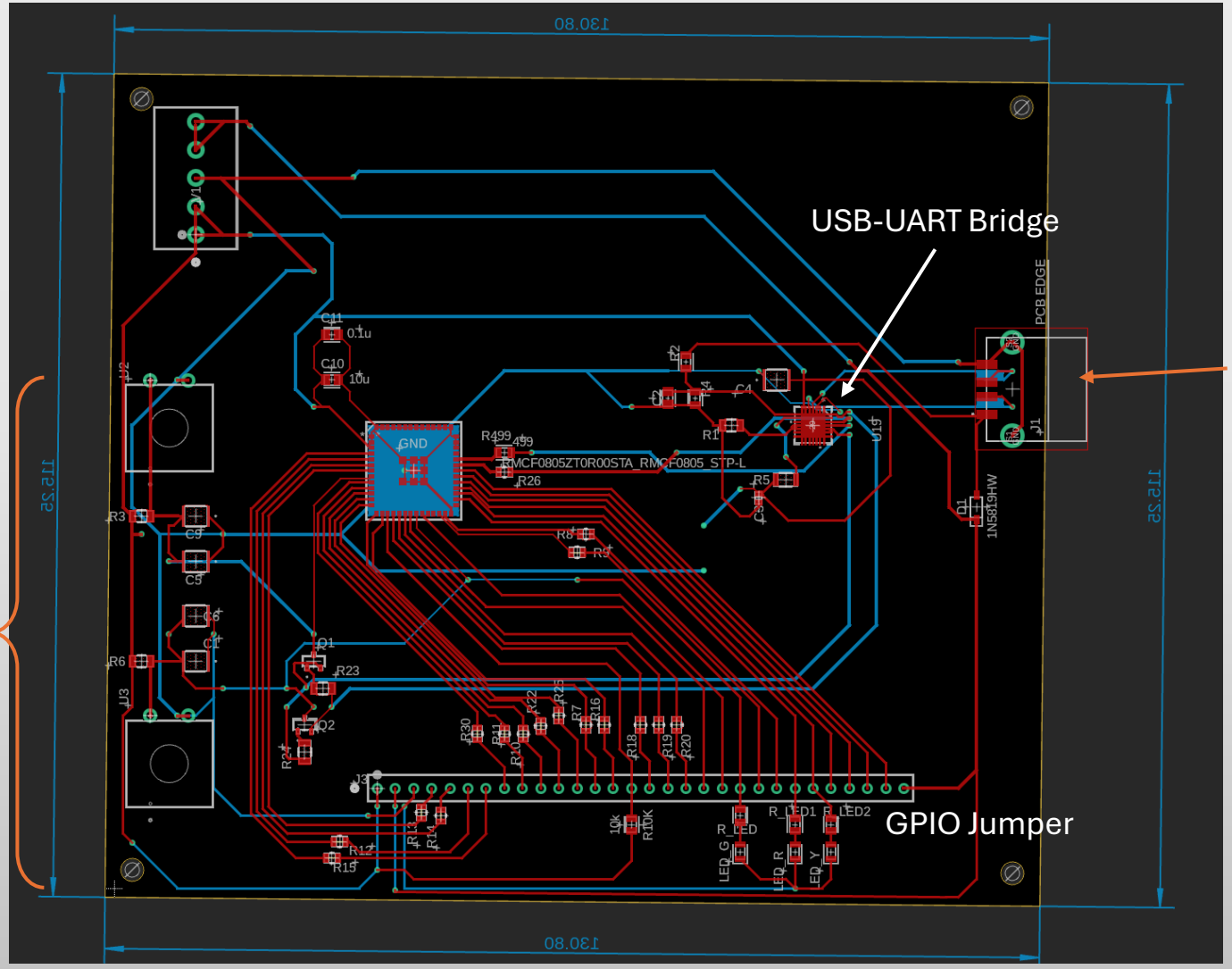
USB to serial bridge CP2102



BOOT and EN buttons for MCU flashing

Hardware Design: MCU Breakout Board Layout

Ethan
EE



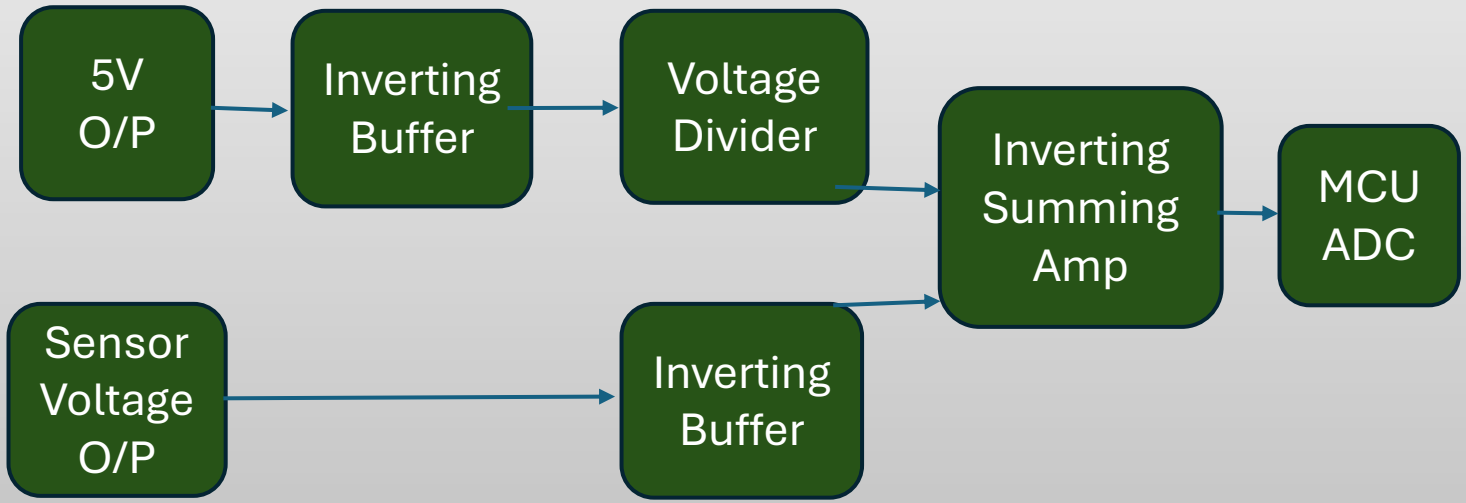
Breakout board with GPIO pin jumpers and USB connection

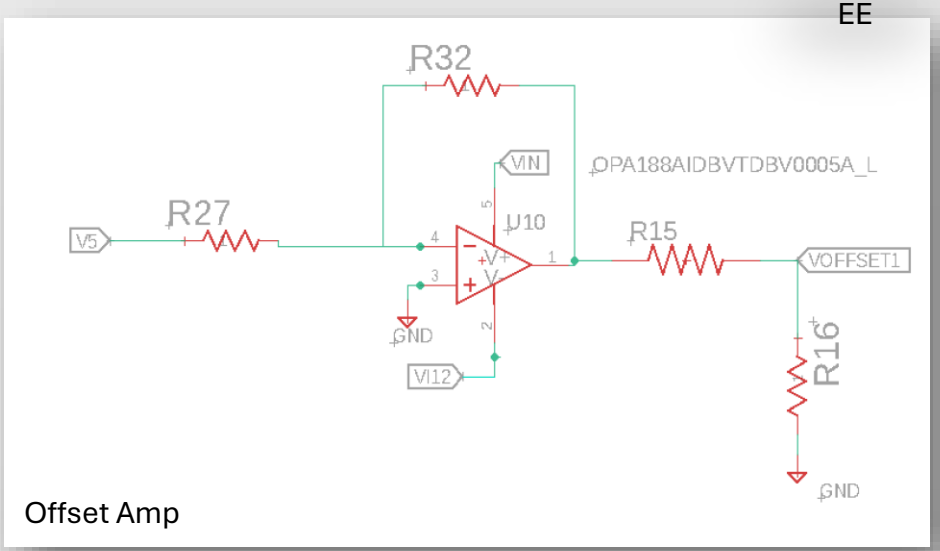
Ethan
EE

Hardware Design: Original AFE

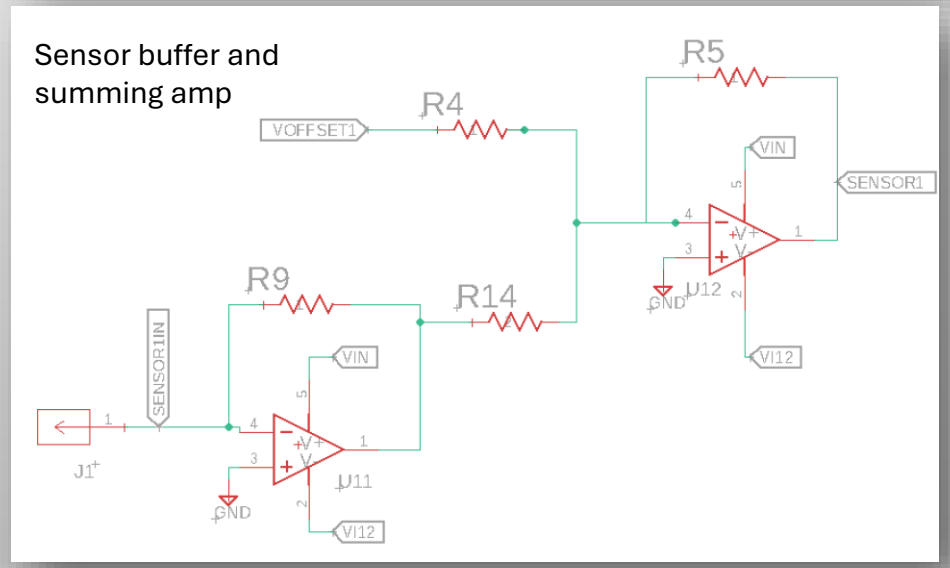
An analog front-end (AFE) module must be attached to every sensor output (O/P max ±2V) such that the ADC module can sample the signal within its sampleable range (0-1V ideally, 0-2V practically). Each detector signal must go through their own analog processor/AFE unit.

The testing source will be low intensity therefore our predictable output range is in the hundreds of millivolts, which the ADC module can sample with precision. The signals simply need to be buffered, and DC offset before being sampled by the ADC





Offset Amp



Hardware Design: AFE Redesign

Ethan
EE

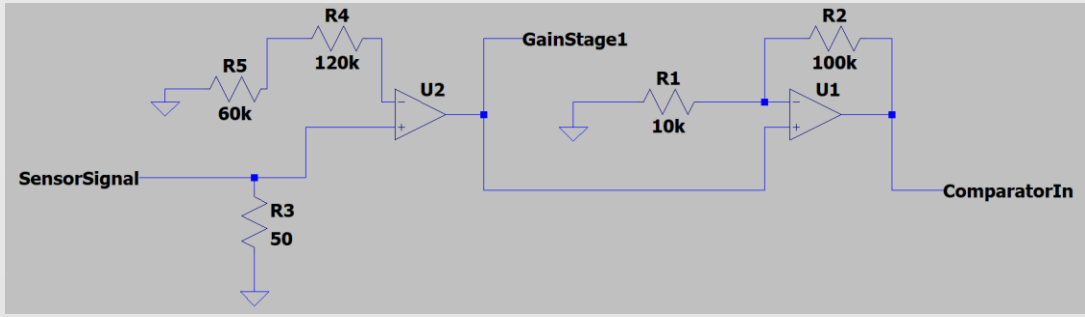
$$4\ \text{ns} \rightarrow f_{\text{harmonic}} = \frac{1}{t_{\text{pulse}}} = 250\ \text{MHz}.$$

To preserve the pulse shape, you need at least the 5th harmonic:

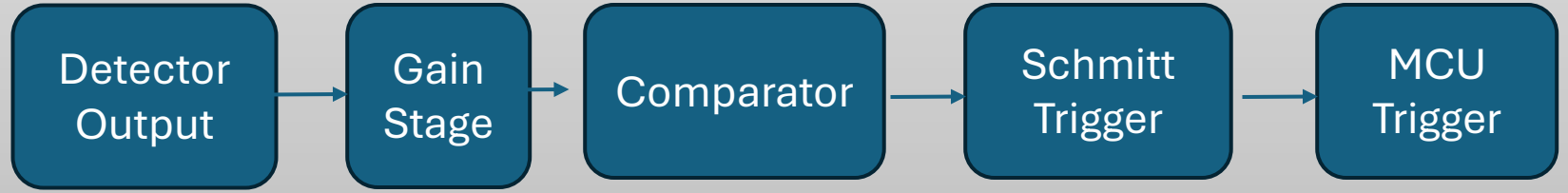
$$f_{\text{required}} = 5 \times 250\ \text{MHz} = 1.25\ \text{GHz}$$

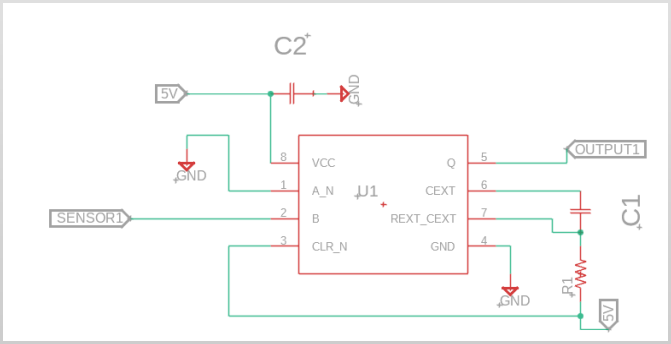
Signal Characterization and Bandwidth requirement

- AFE purpose and design: The analog front end (AFE) amplifies the photodetector's small signal (50–100 mV, 4 ns duration) using a 3.9 GHz GBW op-amps, ensuring compatibility with the ESP32. Next, the signal is fed into a high-speed Comparator which will limit any dark count noise. Proceeding, A Schmitt trigger lengthens the amplified pulse for a clean square wave output, while a comparator removes unwanted noise. This processed signal enables the ESP32 to accurately count pulses which represent incident photons.



Op-Amp Buffering input signal from BNC, Signal gain is 35.6 dB



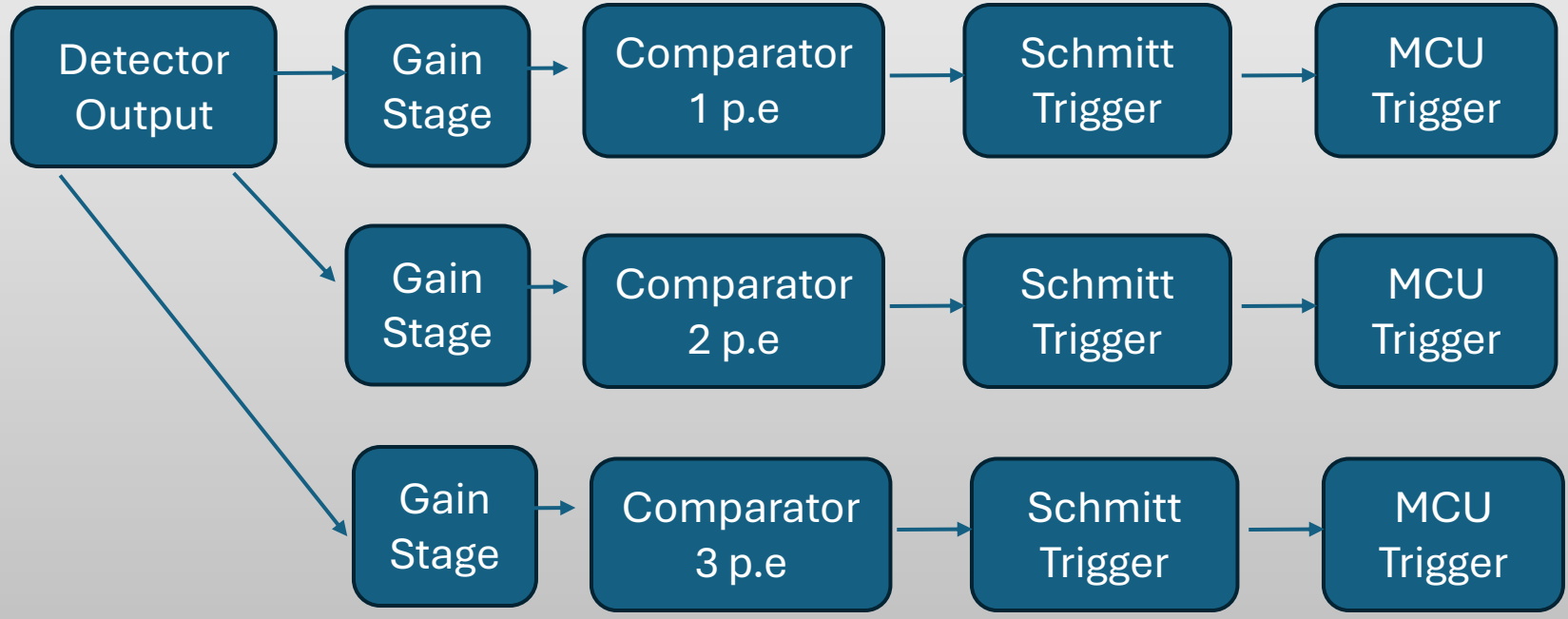


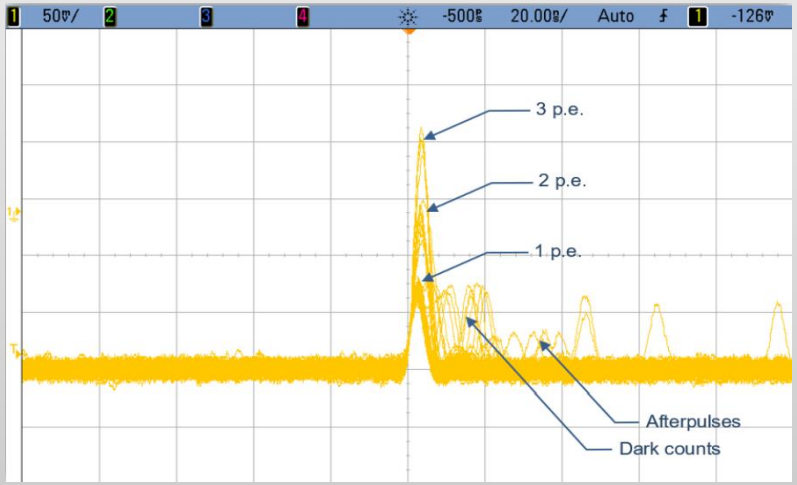
Schmitt trigger with adjustable pulse width

Hardware Design: Expansion (Not Implemented)

Ethan
EE

- Using the previous pulse counter scheme, we can retain amplitude information by setting the comparator's reference voltage to that of 1p.e (90 mV), 2p.e (190 mV), and 3p.e (290 mV). This design requires more channels per detector and software adjustments for a desired output format.



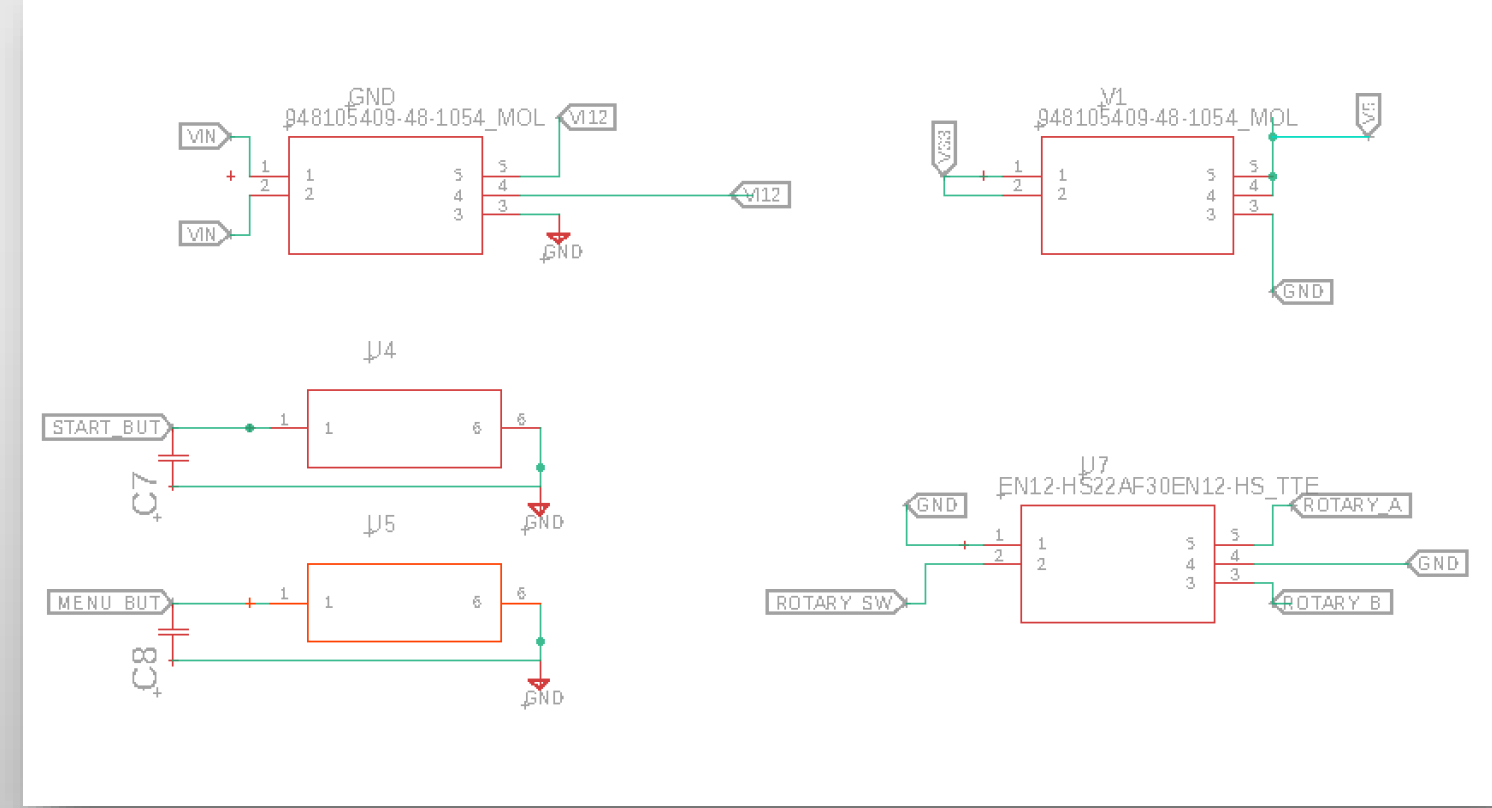


Hardware Design: Peripheral Board

Ethan
EE

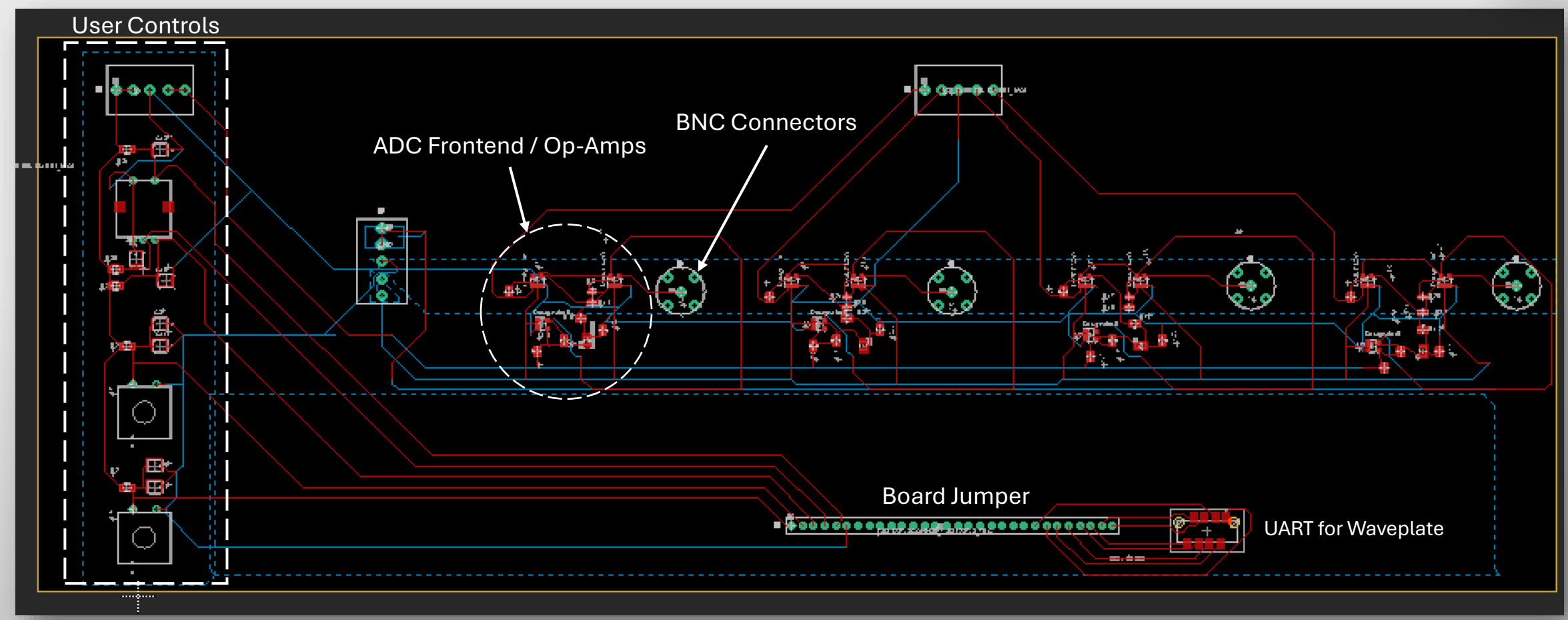
<u>Controls, display, & power connection</u>:

- Rotary Encoder for sampling duration adjustment (bottom right)
- Buttons for sampling start & menu select (bottom left)
- 3.3V, 5V , ±12V, and GND connection (top left and right)



*Hardware Design: Peripheral Boards

Ethan
EE

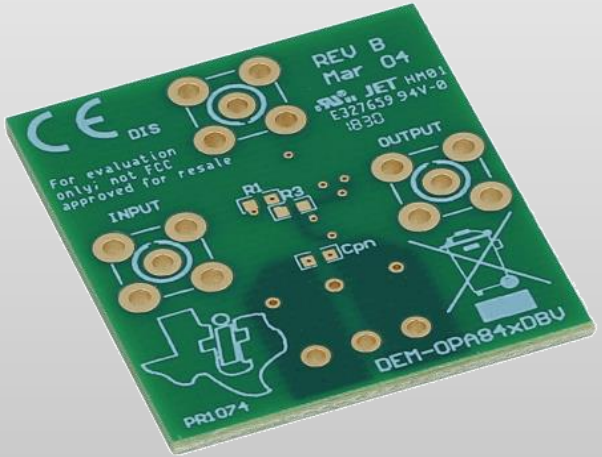


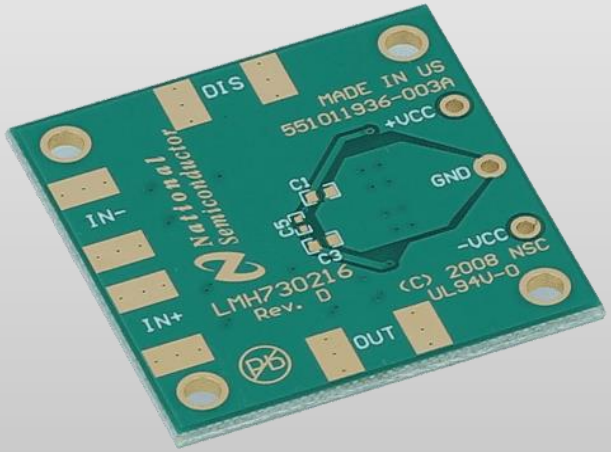
AFE and Controls implemented in conjunction on peripherals board

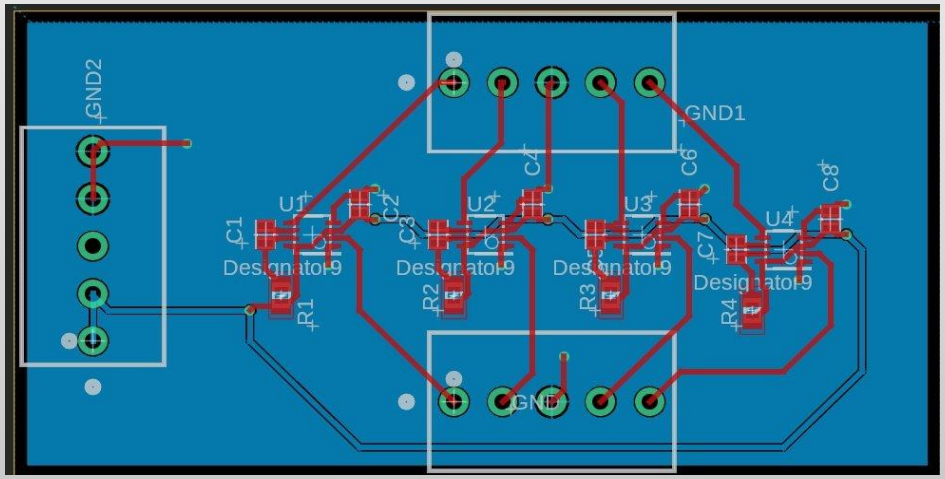
Hardware Design: Pulse Counter

Ethan
EE

- To create the pulse counter AFE we utilized evaluation boards to host the op amps and the comparators. A custom PCB was made to host the Schmitt triggers.







Software Design

Looking at the specific choices we took to accomplish our goals.

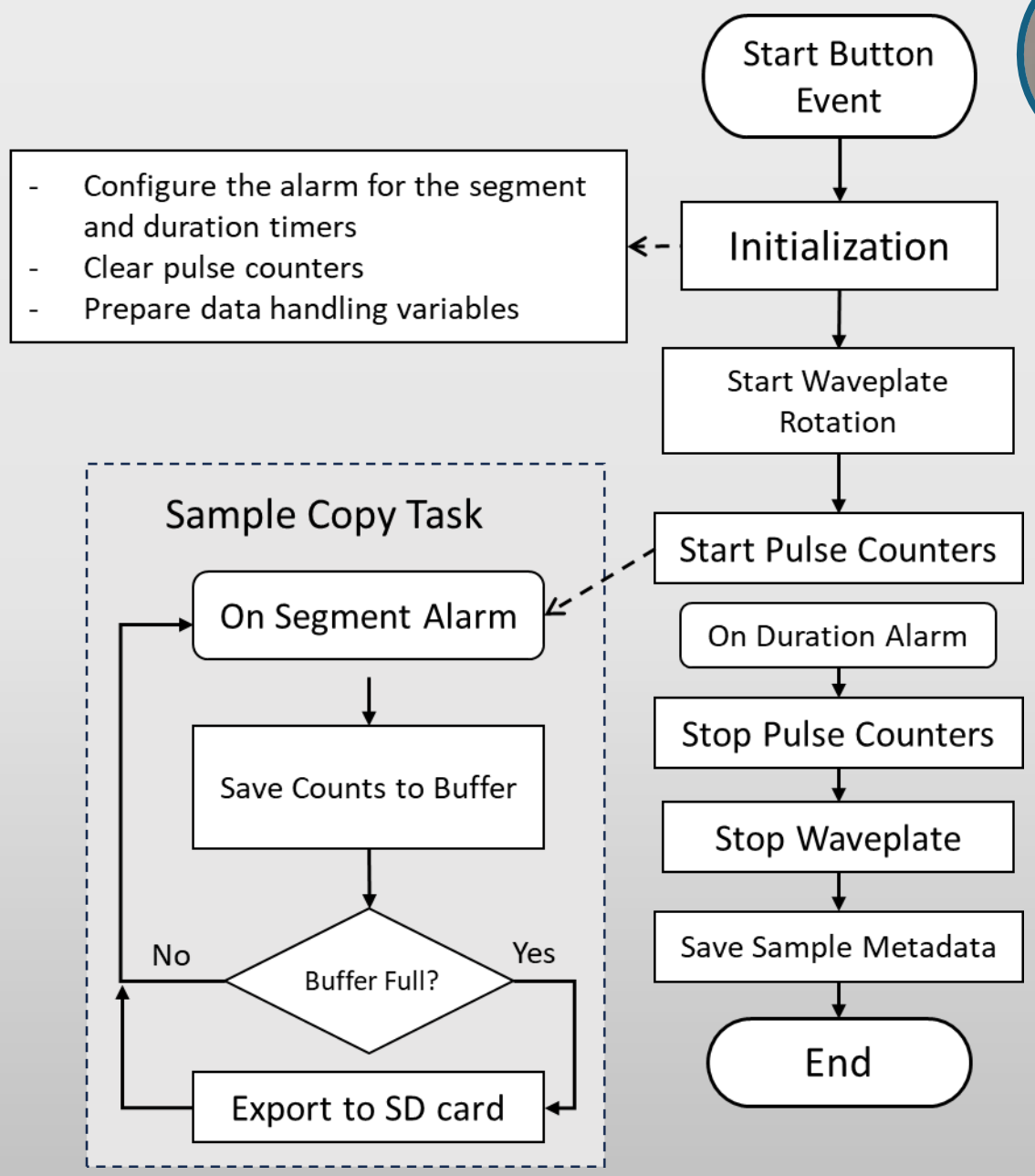
Software Design

David U.
CpE

- Native ESP32 developer environment
- Peripherals used:
  - Pulse Counter (PCNT) – Rotary Encoder Dial and Pulse/Edge Counting
  - Motor PWM (MCPWM) – Servo Control
  - UART – Waveplate and PC communication
  - LCD I2C Library
  - SD Card
- Python data processor
  - Get and store data
  - Find polarization
  - Find pulse time

Sampling Flow

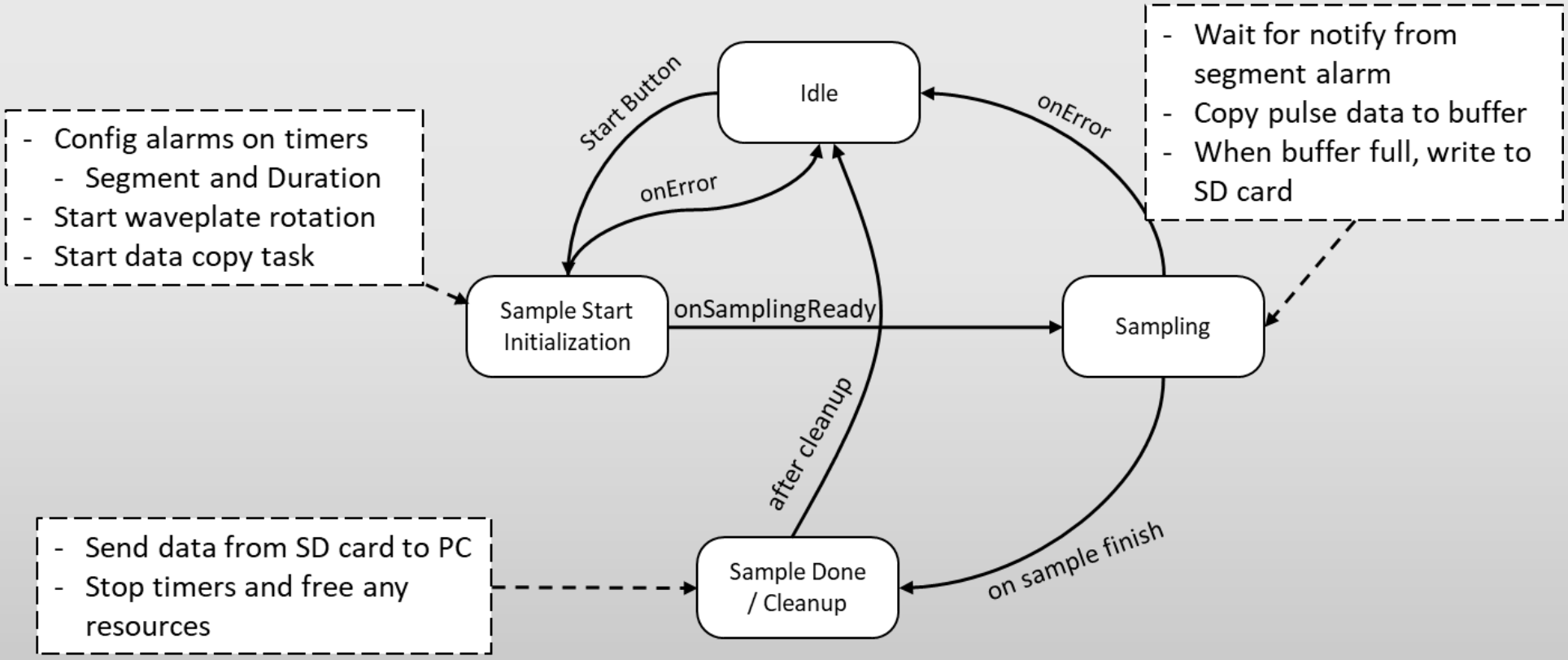
- Sampling starts on button press
- User-defined parameters used for configuration
- Counts pulses during sampling “segment”
  - This is just the period of the sampling frequency
- Stops using a timer
- Starts waveplate for sampling, stops when done



David P.
CpE & PSE

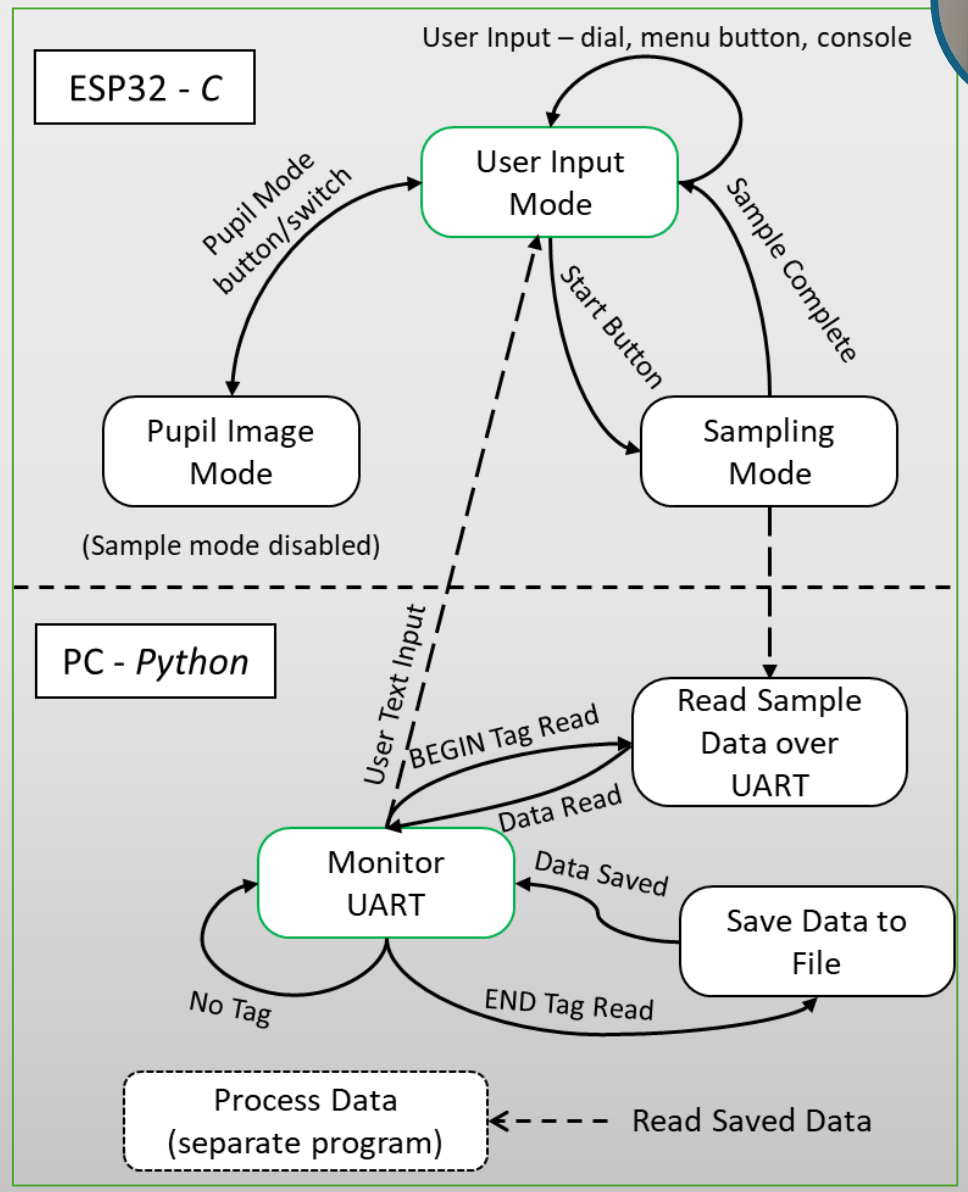
Sampling State Machine

David P.
CpE & PSE



Broad State Diagram

- Green border is starting state
- Top section are states for ESP32
- Bottom section are states for Python
- Communicates occurs through UART to USB bus

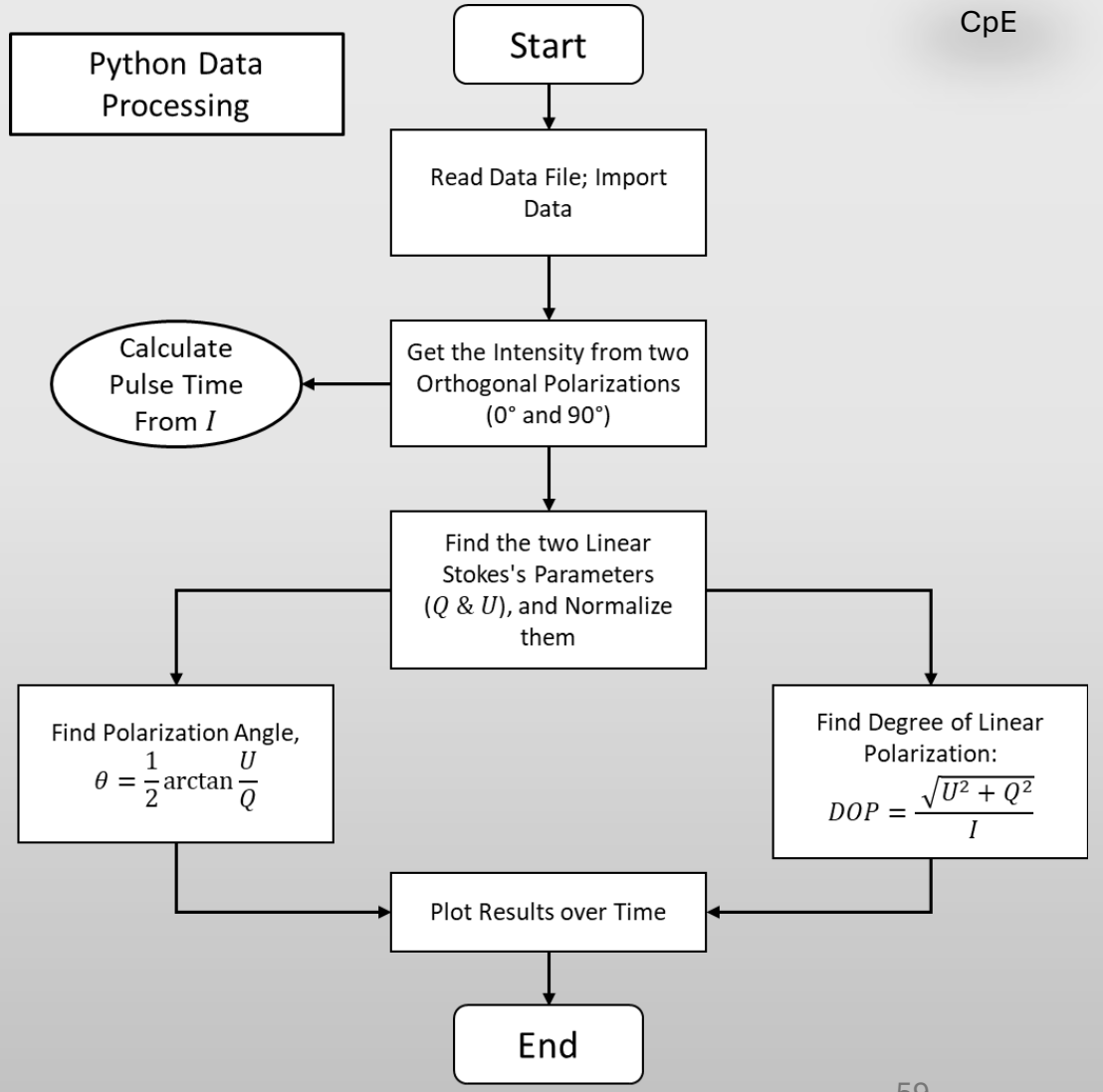


David P.
CpE & PSE

Data Processing

David U.
CpE

- Gives meaning to the data:
  - Angle of polarization
  - Degree of linear polarization
  - Pulse time and plot
  - Fourier transform
- Export data into .FITS file format
  - Preferred format for astronomers
  - Python library used for easy conversion**



Assembly & Testing

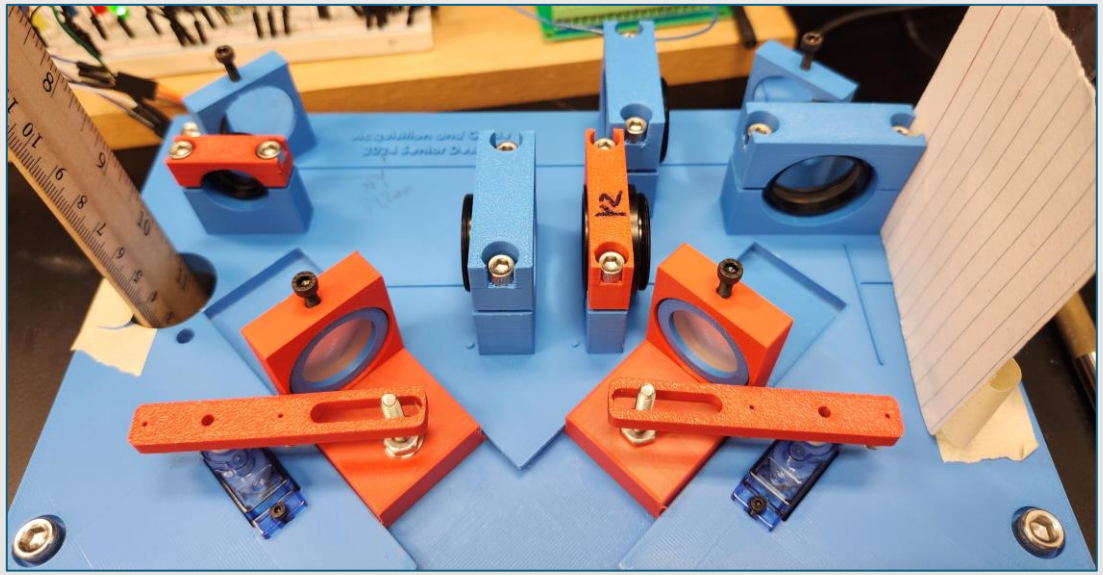
We now look at the assembled project and our testing.

Image System Testing

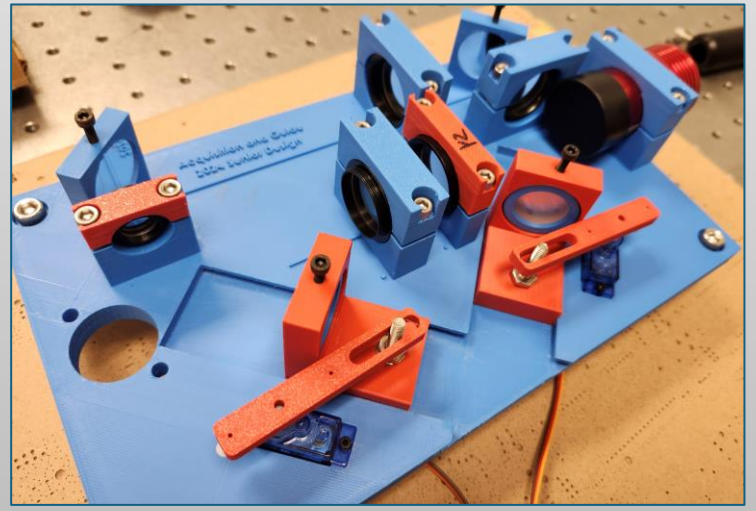
- The system is tested by imaging a ruler and finding the size of the image on the detector:

$$m = \frac{h_{img}}{h_{obj}} = \frac{w_{pixel} \cdot d_{pixel}}{1\ \text{mm}}$$

Where $d_{pixel} = 4\ \mu m$ and w_{pixel} is the width of a millimeter in pixels.



Shown above, is how we tested alignment of lenses. Below is how the images were captured.

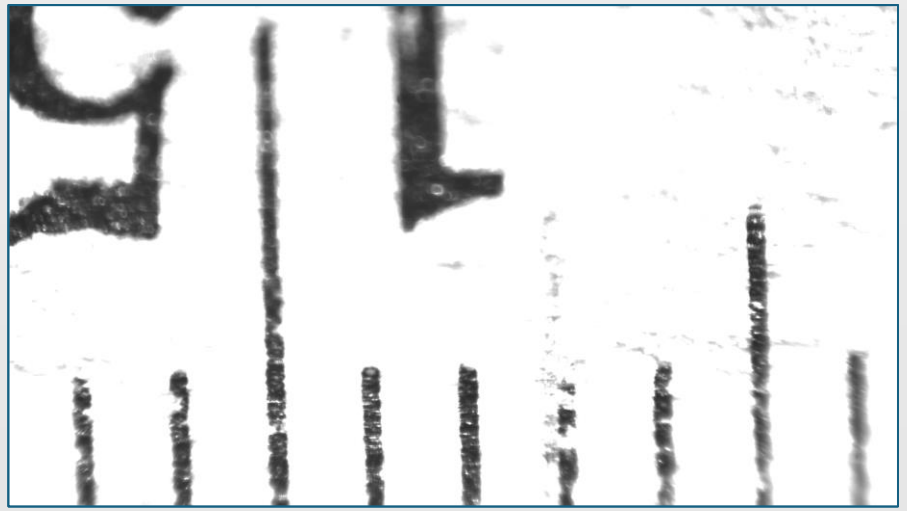


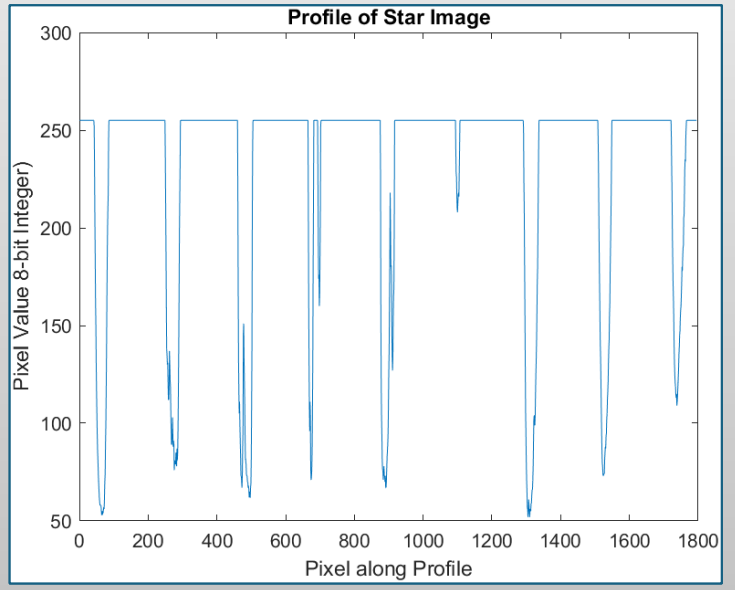
David P.
CpE & PSE

Magnification Results

- From the profiles, the magnification is found, and averaged
- Pupil samples: 60 from 3 images
- Star samples: 24 from 3 images

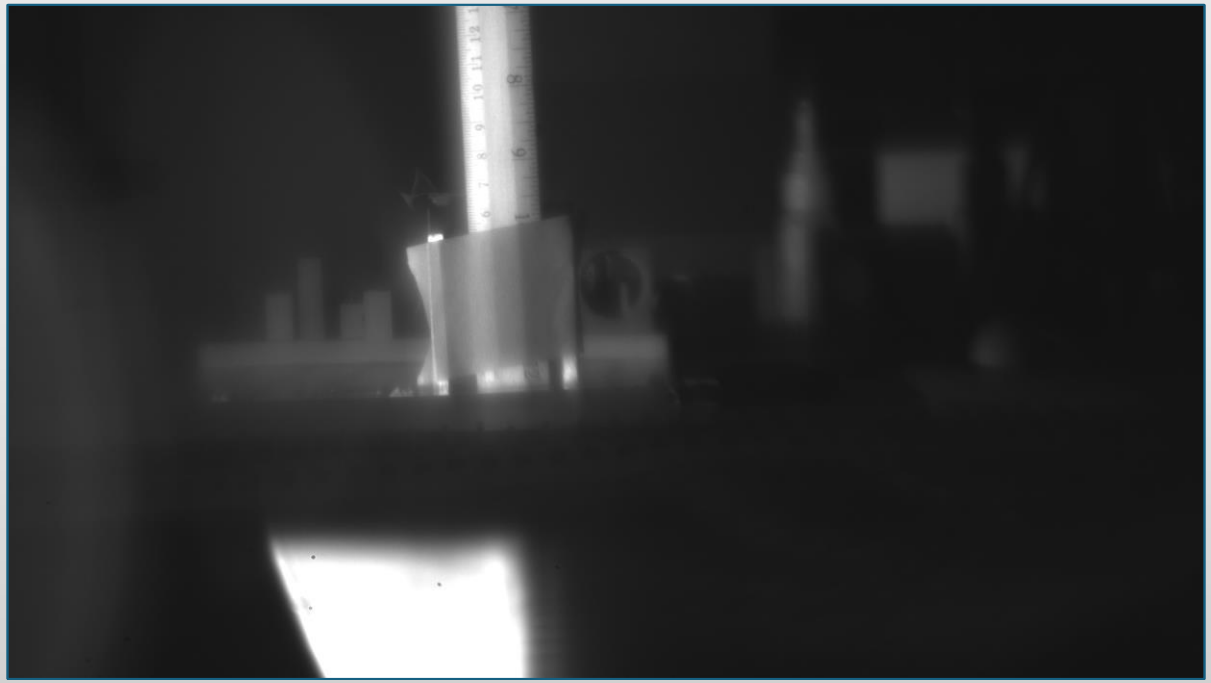
Metric	Pupil Image	Star Image
Magnification	0.0186	0.837
Designed Mag.	0.0189	0.863
Error	1.59%	3.02%

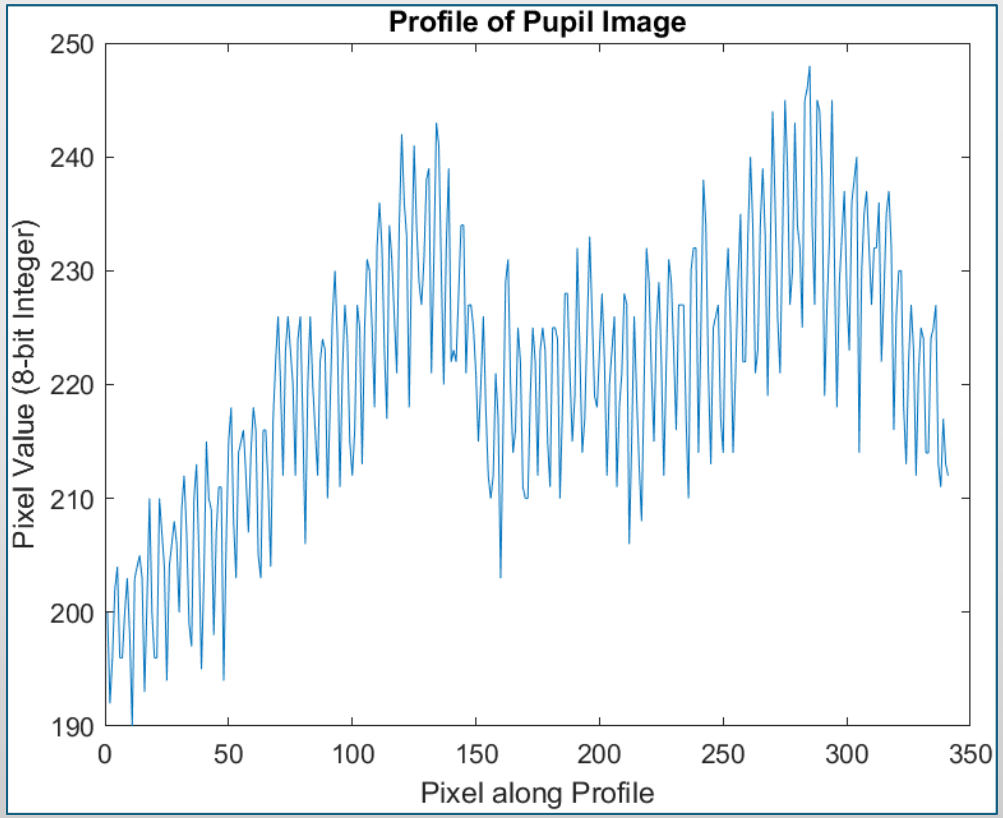




David P.
CpE & PSE

Pupil Images and Profiles



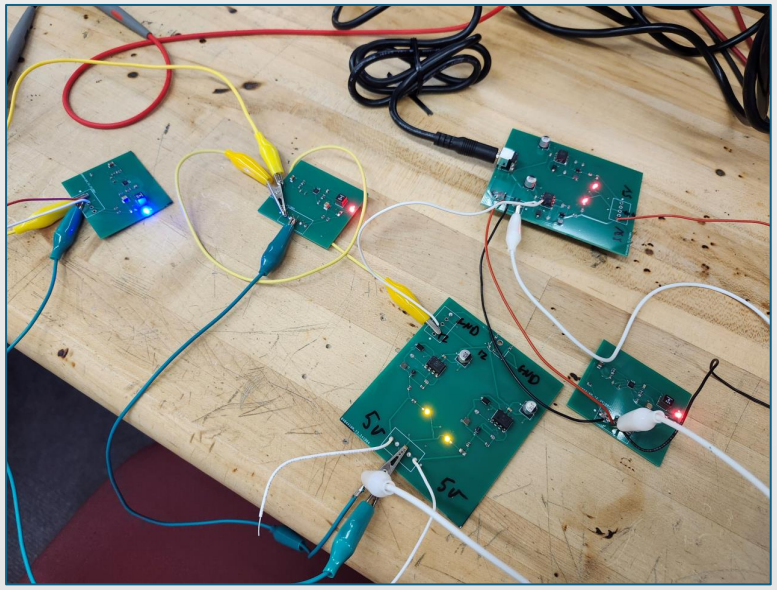


David P.
CpE & PSE

Power Supply Unit

Ethan
EE

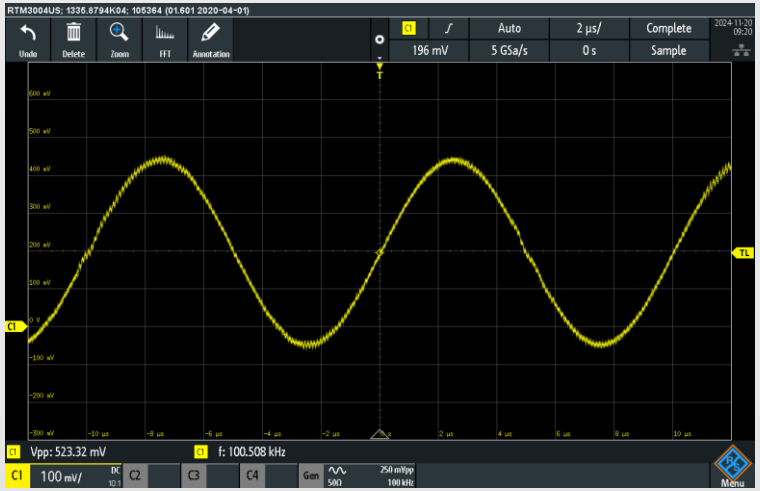
For testing the power supply, all regulator boards were connected to a common ground. Regulators with the same output voltage were then wired in parallel for max current output. Lastly, once connected to the 12V wall plug we used a DC electronic load to properly simulated the current draw that would occur at a maximum power usage

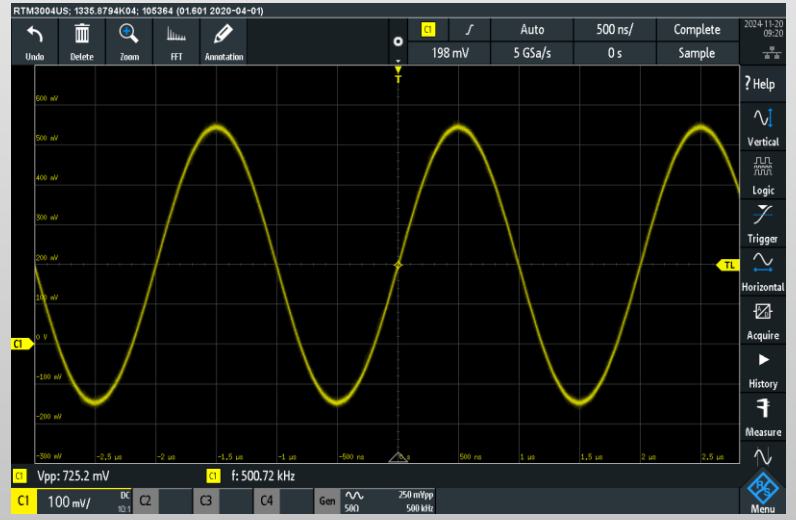


Voltage	Max Current	Test Currents	Load Type
3.3V	100 mA	10 mA, 50 mA, 100 mA	DC Electronic Load
5V	800 mA	100 mA, 400 mA, 800 mA	DC Electronic Load
12V	230 mA	50 mA, 150 mA, 230 mA	DC Electronic Load
-12V	230 mA	50 mA, 150 mA, 230 mA	DC Electronic Load

Testing: Original AFE Design

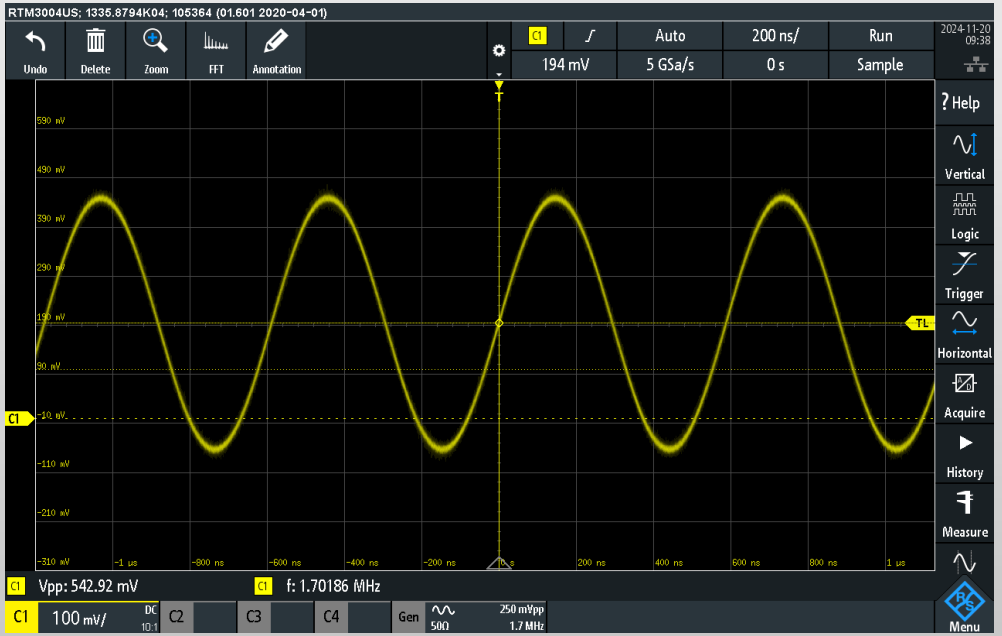
Ethan
EE





100 (Top) & 500 (Bottom) kHz; Sampleable Signal

Tested AFE by setting 3 different test input sinusoids. The sine wave was 250 mVp-p at: 100 kHz , 500 kHz (max we can sample at 1 MSPS), and 1.7 MHz (maximum signal frequency before attenuation).



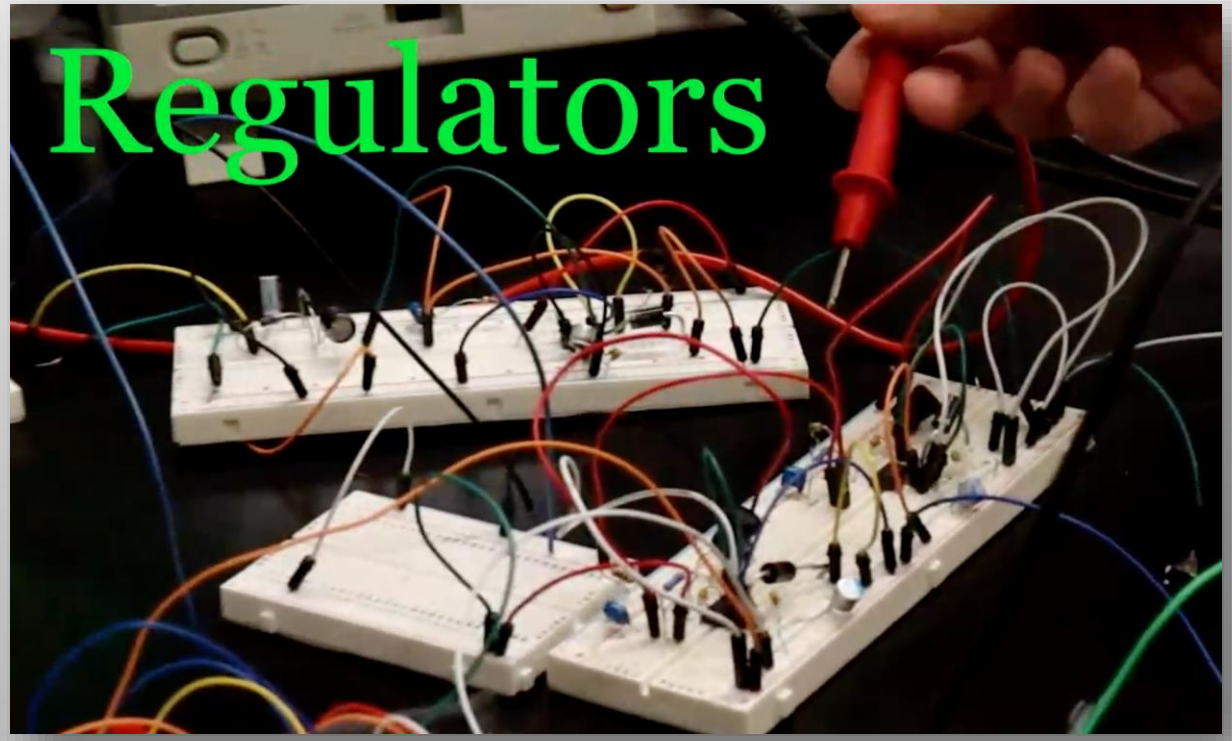
1.7 MHz; Max Amplifier output

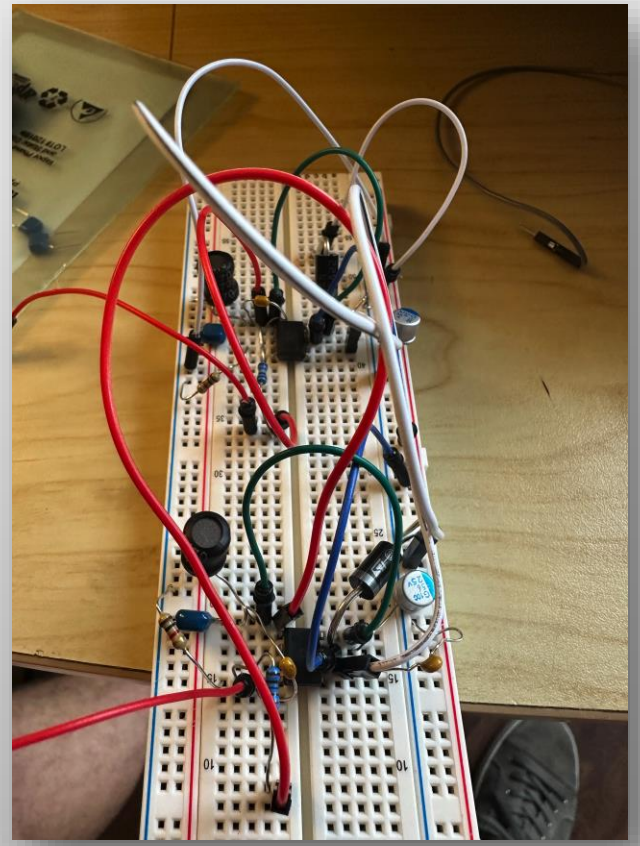
Prototyping: Power Supply Unit

David U.
CpE

Regulator scheme breadboard construction 3.3V, 5V, and –12V

Utilized through-hole components with values as specified by the regulator manufacturer and following application instructions

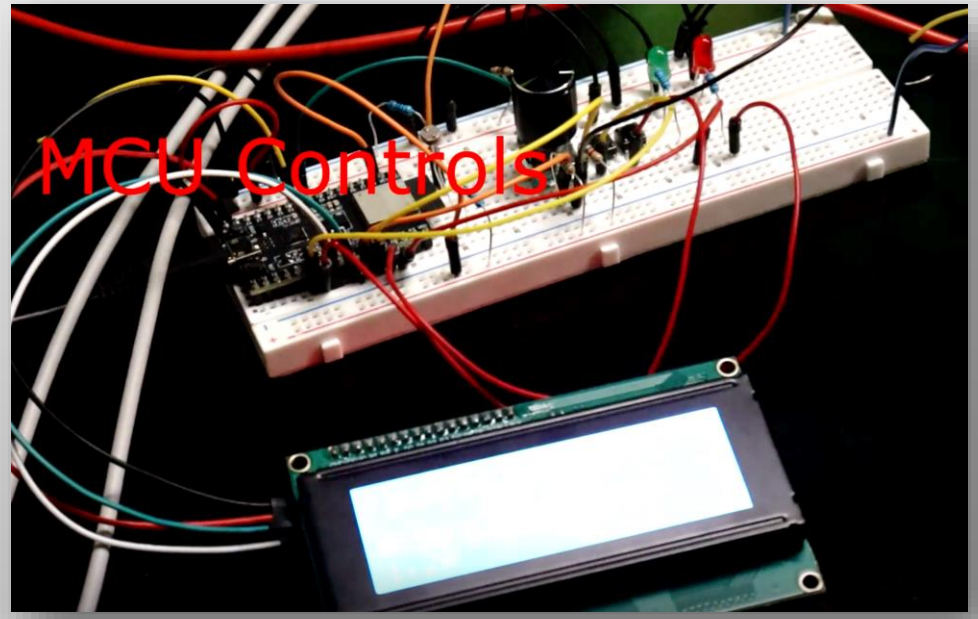


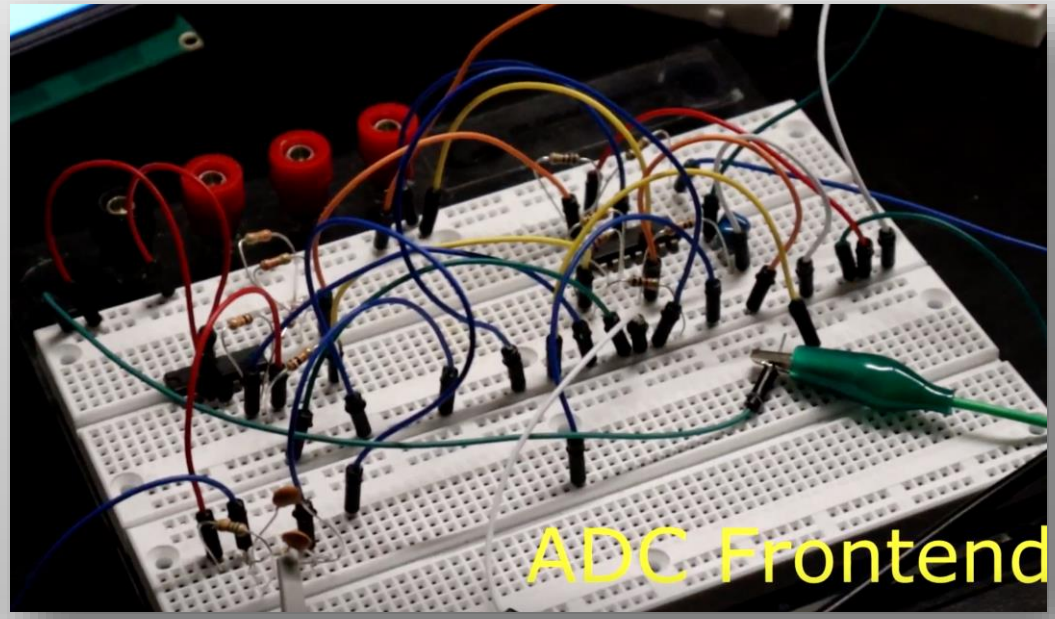


Prototyping: MCU Interfaced With Controls and Peripherals

David U.
CpE

- Electronics: AFE circuit construction, and MCU Dev board interfacing.





Prototyping: Optics

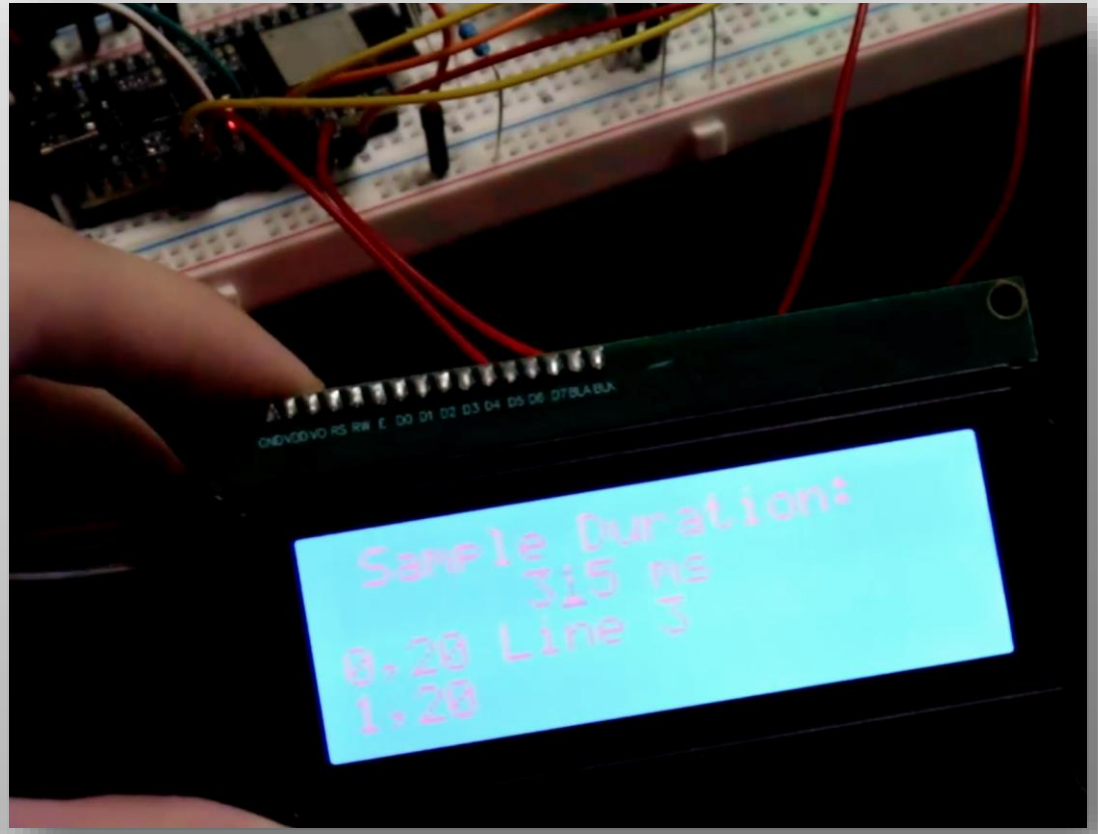
David P.
CpE & PSE

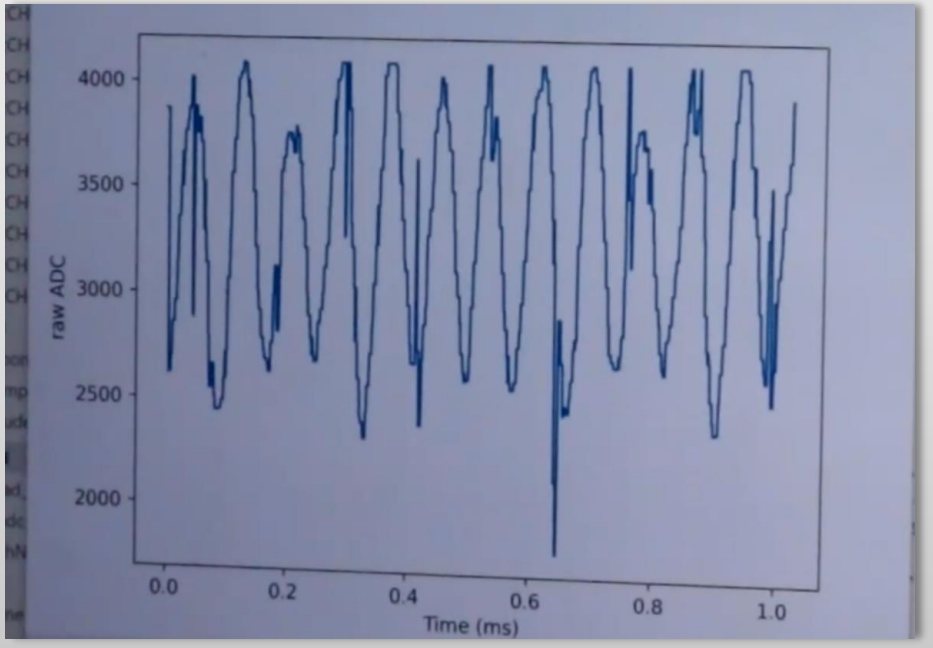
- Use of lenses to match the telescope's f/# and simulate its output.
- Use of a Wollaston prism to take polarization measurements of a test light source, in combination with a rotating half wave plate to affect polarization at a rate of 1 Hz.
- Measuring the response of photodetectors to a known source.
- Demonstrating multiple imaging paths by use of a flip-able mirror.

Testing: MCU, Peripherals, and AFE Prototype

David P.
CpE & PSE

- Controls and display, AFE testing, ADC sampling at 1 µs, Rotation mount testing
- What we learned: AFE adjustment, ADC buffer/memory management





Plotted data from the ADC sampling at 1MHz for a 100kHz sine wave

Testing: PSU Prototype

Ethan
EE

- 3.3V and 5V regulators had successful output
- 3.3V and 5V worked when implemented with the MCU prototype board
- Inverting scheme using LM2576 failed, using inverting charge pump off a 12V LM2675-ADJ regulator failed
- MAX17577 was ideal regulator for allowing inverting output with sufficient current output. Multiple inverting modules will be needed in final project to meet requirements

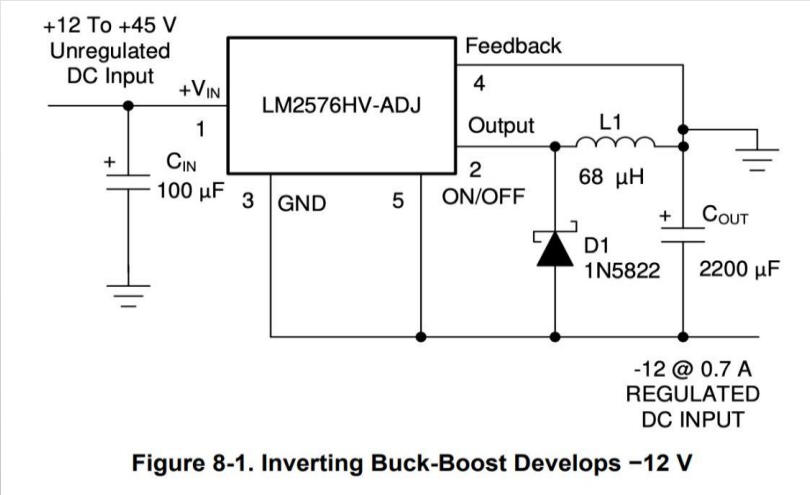
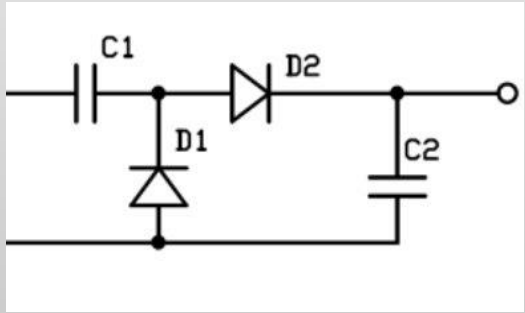
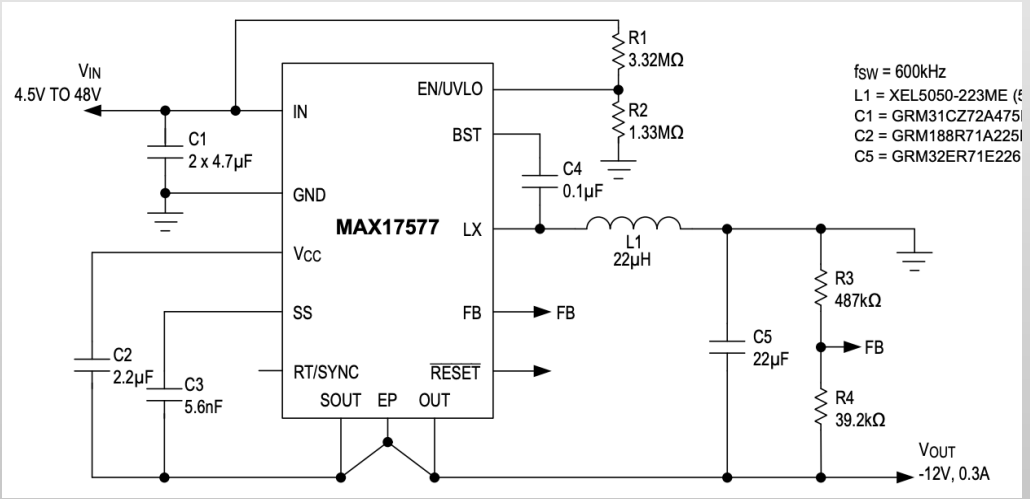


Figure 8-1. Inverting Buck-Boost Develops −12 V

LM2576 inverting output scheme
Original design (failed)



Inverting charge pump which connected to LM2675-ADJ PWM output
Secondary plan (failed)



MAX17577 inverting output scheme

Budget

Vincent
PSE

Item	Qty.	Cost	Item	Qty.	Cost
Photodetectors	4	$6400	PCB Printing	5	$70
Lenses / Mirrors	18	$600	Circuit Components	-	$100
Wollaston	2	$1200	Housing Materials	1	$100
Waveplate	1	$1600	Mechanical Components	3	$650
Camera	1	$250	**TOTAL**	**-**	**$10,990**
Chips		$20			

Distribution of Labor/Work


Ethan
EE

General Breakdown:

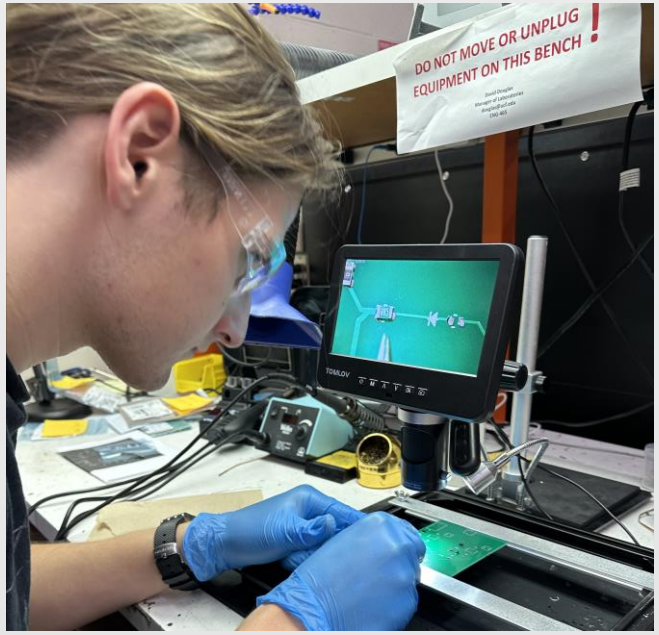
- Optics Design: Vincent Miller (Polarimeter) and David Patenaude (Dual Imaging System)
- Hardware Design: Ethan Tomczak (Analog processing and PCB design)
- Software Design: David Patenaude and David Urrego

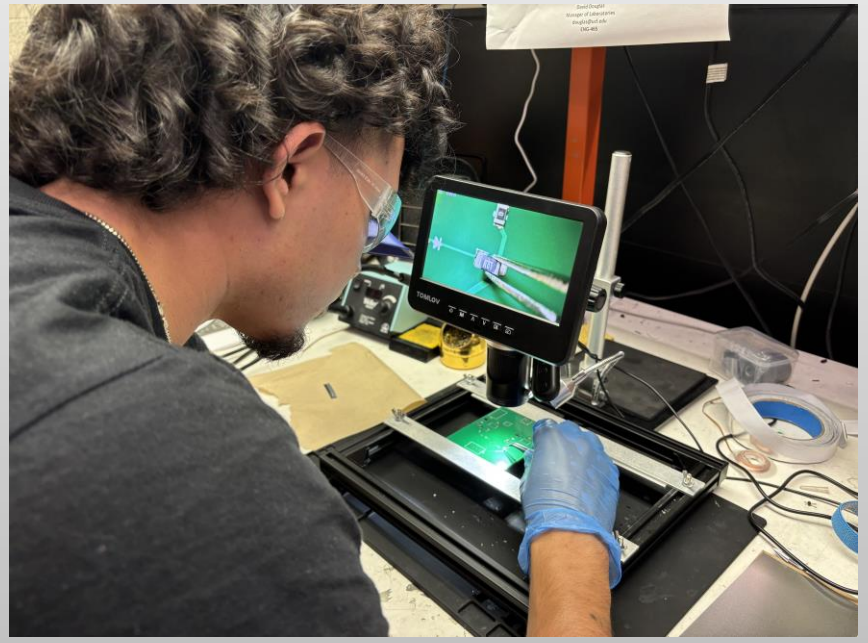
Detailed breakdown:

Area	Primary	Secondary
Project Manager	David P.	Vincent
Website Design & Management	David P.	David U.
Polarimeter	Vincent	David P.
Image Acquisition	David P.	Vincent
Embedded Coding	David P.	David U.
Python Package	David U.	David P.
Power Supply	Ethan	David U.
PCB	Ethan	David P.

Progression

- Additional 5v
- AFE Redesign
- MCU Module
- Data processing with threading and user input
- Pulse Counting and Buffering
- Communication between MCU and Waveplate
- Finalizing optical assemblies and calibration
- Housing for PCB's and Optical components





Ethan
EE

David U.
CpE

Here was our Plan to Finish

- Weekly tasks planned out
- Testing and integration activities included
- Includes submission deadlines

#4, 9/9	- PCB Review Meeting by 9/13	- CDR power point - Waveplate w/ MCU - MCU ADC -> sample desired amount and print - (SW) Testing of the above
#5, 9/16	- CDR Presentation (video) Due 9/18 - Our CDR Presentation Lecture 9/20	1. Record CDR slides 2. SD card speed testing/implementation 3. Start housing assembly? 4. Start designing/CAD of assemblies.
#6, 9/23	- CDR Lecture part 2	- Start Assembling optical components
#7, 9/30		- Start Assembling electrical components (mounting and wiring) - Test Optical. - Test electrical - Schedule Midterm meeting
#8, 10/7		1. Film midterm demo video 2. Integration testing carry over
#9, 10/14	- **Midterm Demo (video) due 10/19 (5pm)**	- Filming carry over
#10, 10/21	- Midterm Demo Meeting (from 10/21 to 10/23) Zoom	-
#11, 10/28		
#12, 11/4	- Conference Paper due 11/8 (12pm)	- BE DONE BY NOW!!
#13, 11/11	- Reserve Time Slot for Final Pres. by 11/15	-
#14, 11/18	- **Live Demo (CREOL) Friday, 11/22**	-
#15, 11/25	- Final Documentation due 11/26 (12pm)	-

David P.
CpE & PSE

How we Actually Finished

- Losing a week to a hurricane when PCBs were supposed to arrive de-railed the plan.
- Despite weekly meetings and weekly progress, the project fell behind.
- A design flaw/oversight was found last minute

David P.
CpE & PSE

		- **Begin making housing assembly base (9/30)**	**Weekly Goals**
#7, 9/30	Events: Internship / Career Fair Thursday 1-4:30pm, Additions Arena	- *Start Assembling electrical components (mounting and wiring) – moved to 10/7* - **Test Optical (from 9/23).** - Test electrical - ~~Schedule Midterm meeting~~	- Software is ready to be integrated with Hardware - Housing and assembly are planned - Critical parts are ordered (PCBs) ASAP
#8, 10/7 (Hurricane)	- PCB Acquisition (show Dr. Weeks) due 10/11 (5pm) - Schedule Midterm Demo Meeting by 10/11	1. Verify electrical/PCB design meets specs 2. Start assembling optics and electronics into housing 3. Film midterm demo video (later) 4. Integration testing carry over	
#9, 10/14	- **Midterm Demo (video) due 10/19 (5pm)**	- Filming carry over	- Film functional software, with any hardware that is implemented in time - Begin integration testing
#10, 10/21	- Midterm Demo Meeting (from 10/21 to 10/23) Zoom - CREOL Career Fair Thursday, 1-5pm -	- (Meeting on Wednesday at 12pm) - PCB Assembly - Continue CAD assemblies o Optical Base o Mounts o PCB locations and housings - Waveplate control testing with MCU -	Python Serial Input, and rudimentary data analysis. Hammer out testing environment.
#11, 10/28		- Testing Results (optical power through system, Performance benchmarks, hard numbers!) - MCU PCB complete? - Housing Construction	-
#12, 11/4	- Conference Paper due 11/8 (12pm) [on website]	- Work on Conf. Paper - Integrating	- Be close (~90%) to finishing
#13, 11/11	- Reserve Time Slot for Final Pres. by 11/15	- Work on mounting optics - Work on PCBs and testing them - Discovered design flaw Thursday, Nov. 14th.	- Project completed, and prepared for Demo
#14, 11/18	- **Live Demo (CREOL) Friday, 11/22**	- Get Demo Video and Final Presentation footage Monday/Tuesday	-
#15, 11/25	- Final Documentation due 11/26 (12pm)	- Update 120pg Documentation.	-
#16, 12/2	Finals Week		

Bibliography

Thorlabs beamsplitter images from:
https://www.thorlabs.com/newgrouppage9.cfm?objectgroup_id=9028

Thank You for Watching!