UCF DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCEINCE

Spring 2015 Seminar Series

Presented by the ECE Division

NEXT-GENERATION ARRAY & TAPE ORGANIZATIONS FOR REVOLUTIONARY SPINTRONIC TECHNOLOGY

FRIDAY APRIL 17, 2015 • 2:00 PM – HEC 113

The continuously increasing technical challenges for the scaling of mainstream memory technologies inspired the recent tremendous investments on next-generation nonvolatile memory (NVM) technologies. Many candidates, i.e., phase change memory, magnetic memory, and resistive memory, have been identified and extensively studied. Various new applications are also invented by leveraging their attractive characteristics such as non-volatility, high integration density, nanosecond access time, etc. In this presentation, I will give a comprehensive overview on the revolutionary spintronic technologies and the application of on-chip caches. I will start with spin-transfer torque random access memory (STT-RAM) at the early of stage of commercialization and then extend the talk to emerging racetrack memory that has been successfully demonstrated at device and small array level. In STT-RAM development, multi-level cell (MLC) that doubles the data storage density and hence has gained great attention. The use of MLC in STT-RAM caches, however, encounters a number of design challenges, including the limited density benefit of the MLC design and the degraded performance and reliability induced by the multi-step accesses. Advanced spintronic technology, i.e., racetrack memory, enables an extremely high storage density and offers a "faster-than-Moore's law" scaling path. However, potentially unorthodox new memory hierarchies are necessary to take maximum advantages of the fast but pseudo-sequential access of racetrack memory. Our latest research outcomes on these topics will be presented and discussed.

DR. HAI (HELEN) LI

University of Pittsburgh

Hai (Helen) Li received B.S and M.S. from Tsinghua University (both with early graduation) and Ph.D. from Purdue University. She has been an Assistant Professor in the Department of Electrical and Computer Engineering at University of Pittsburgh since 2012. She was faculty member of Polytechnic Institute of New York University in 2009-2012. Before that, she worked with Qualcomm Inc., Intel Corp., and Seagate Technology. Her research interests include memory design and architecture, brain-inspired computing and neuromorphic systems, and device/circuit/architecture co-optimization for low power and high performance. She has published 1book, a few book

Chapters, and about 140 research papers in journals and refereed conference proceedings, in the area of EDA, computer architecture, VLSI circuit designs, and embedded systems. Dr. Li is the associate editors of IEEE TVLSI, ACM TODAES, IEEE TMSCS, and served on the technical and organization committees of more than 20 conferences. She received five best paper awards from ISQED'08, ISLPED'10, GLSVLS'13, ISVLSI'14, ASPDAC'15 and several other nominations in ICCAD, DATE, etc. Dr. Li is recipient of the NSF CAREER award in 2012 and DARPA Young Faculty Award (YFA) in 2013.

Hosted by: Dr. Yuan and Dr. DeMara

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