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THE DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE, ECE DIVISION

Presents the 2012 EECS Spring Seminar Series

Dr. Fernando Guarín

Semiconductor Research & Development Center, IBM Systems & Technology Group

"Semiconductor Reliability Topics for the Qualification of Advanced CMOS Technologies"

Thursday, April 19, 2012 1:10 p.m. HEC 450

Abstract

As we continue the relentless drive towards smaller semiconductor device feature sizes and higher levels of integration at the chip level for the 14nm node and beyond, it has become increasingly evident that a judicious review and a very complete understanding of the reliability mechanisms that contribute to the degradation of each of the technology elements will be crucial for the successful development of the most advanced leading edge technologies.

The increased device count, and process complexity, coupled with ever decreasing margins in voltage, geometry and the incorporation of new material systems such as; high and low k dielectrics, stress/strain layers. The path to maintaining the scaling cadence and new limiting factors will be discussed from the reliability perspective. A closer look will be given to Hot Carriers, Bias Temperature Instabilities and statistical variations (process and geometric). This talk will present the reliability issues driven by the latest trends and state of the art in semiconductor fabrication as we continue to scale; it will also present the considerations necessary along with a practical approach to the qualification methodology required for leading edge CMOS technologies while providing a review of the specifications and implications of the above mentioned reliability mechanisms. The impact of reliability induced parameter degradation and the mitigation of these effects will be studied for practical circuits through the analysis of switching behavior and SRAM circuit applications. The characterization, models and methodology will be put in the required perspective for the successful technology transfer of leading edge technologies to a manufacturing environment.

Biography

Dr. Guarin works as a Senior Engineer/Scientist at the IBM Microelectronics Semiconductor Research Development Center SRDC in East Fishkill N.Y. His current assignment is as team leader for the qualification of IBM's 14nm technology. He received his BSEE from the "Pontificia Universidad Javeriana", in Bogotá, Colombia, the M.S.E.E. degree from the University of Arizona, and the Ph.D. in Electrical Engineering from Columbia University, NY. His doctoral research studied the Molecular Beam Epitaxial growth of Silicon based alloys for device applications. He has been actively working in microelectronic reliability for over 30 years.

From 1980 until 1988 he was a member of the Military and Aerospace Operations division of National Semiconductor Corporation where he held positions both in engineering and management. In 1988 he joined the IBM microelectronics division where he has worked in the reliability physics and modeling of Advanced Bipolar, CMOS and Silicon Germanium BiCMOS technologies. He has been the team leader for the qualification of several of IBM's leading edge CMOS and SiGe technologies. He holds 9 patents, one trade secret, has published more than 65 papers and delivered 4 tutorials at the IEEE's International Reliability Physics Symposium.

Dr. Guarín is an IEEE Fellow, Distinguished Lecturer for the IEEE Electron Device, Secretary and voting member of the IEEE EDS Ad.Com, member of EDS Education Committee. He is the Chair for the Electron Devices Society in the IEEE's MHV Chapter, and past president of the Society of Hispanic Professional Engineers SHPE for the Mid Hudson valley Region.

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