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THE DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE, ECE DIVISION

Presents the Spring 2012 EECS Seminar Series

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"Reversible Logic: Fundamentals and Applications in Emerging Nanotechnologies"

Tuesday, January 24, 2012 2:30 p.m. HEC 450

Abstract

Reversible logic is emerging as a promising computing paradigm with applications in emerging nanotechnologies such as quantum computing, quantum dot cellular automata, optical computing, low power nanocomputing, etc. Reversible circuits are similar to conventional logic circuits except that they are built from reversible gates. In reversible gates, there is a unique, one-to-one mapping between the inputs and outputs, not the case with conventional logic. In this presentation, the speaker will introduce fundamentals of reversible logic and its promising applications in emerging nanotechnologies. In this presentation, first, a brief overview of reversible logic basics will be given. Next, the speaker will introduce the design of a new reversible gate namely the TR gate (Thapliyal-Ranganathan) which has the unique structure that makes it ideal for the realization of arithmetic circuits such as adders, subtractors and comparators. The design methodologies proposed to optimize multiple parameters such as ancilla and garbage bits, quantum cost and delay during the design of arithmetic units are presented. Next, the application of reversible logic in online and offline testing of single as well as multiple faults in traditional and reversible nanoscale VLSI circuits is introduced. The talk will conclude with a brief outline of ongoing Postdoctoral research in the area of TSV stress-aware testing of three-dimensional integrated circuits (3D ICs), fault modeling and test generation. Future research directions, teaching philosophy and courses to be taught or developed will also be discussed.

Biography

Himanshu Thapliyal received the B.Tech. degree in Computer Engineering from G.B. Pant University, India, in 2004, and the M.S. degree in VLSI and embedded systems from IIIT Hyderabad, India, in 2006. He received the Ph.D. degree in Computer Science and Engineering from University of South Florida, Tampa, in 2011. Currently, he is working as a Postdoctoral associate at Duke University in the area of DFT of 3D ICs. He has authored or coauthored more than 40 articles in refereed conferences and journals, 1 tutorial, and is a co-owner of a U.S. patent issued recently. His current research interests include reversible logic, conservative logic, emerging nanotechnologies, ASIC and digital design, Vedic mathematics, and design and test of three-dimensional integrated circuits (3D ICs). He is the recipient of Distinguished Graduate Achievement Award at University of South Florida, the IEEE Computer Society Richard E. Merwin Scholarship, and the UPE/CS Award for Academic Excellence. His Ph.D. dissertation work on reversible logic has been featured in MIT Technology Review, ACM TechNews, etc.

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