UCF DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Spring 2016 Seminar Series

OPTIMIZATION OF LARGE COMPLEX SYSTEMS

FRIDAY FEBRUARY 26, 2016

1:30 PM – HEC 356

The fabrication of sub 20 nm transistors and the effectiveness of computer-aided design (CAD) for very large scale integration (VLSI) have enabled the assembly of billions of transistors into a single integrated circuit (IC) at low cost. These ICs have made available and affordable various electronic devices to the general public. Many emerging areas of research involve facilitating human interaction with these devices and enabling these devices to interact as a loosely connected entity (known as the internet of things (IoT)). In this talk, I will first present CAD techniques developed for VLSI. Next, I will continue with how these techniques can be leveraged to address challenges encountered within these emerging domains.

Every sequential circuit operates in synchrony, with a clock network delivering a clock signal to the sequential elements to coordinate the computation. The physical synthesis of the clock network is one of the most challenging design steps within CAD for VLSI because the clock network is typically the second largest network on a chip and its quality affects the overall performance of the chip. In my research, I have proposed techniques to reduce the negative effects of on-chip variations by incorporating essential quality measures and design constraints in a graph formulation, thereby transforming the optimization problem into the problems of finding shortest paths and detecting negative cycles in a weighted graph. Moreover, I have also proposed essential techniques based on mathematical and graph formulations for the synthesis of clock networks that require support for multiple-corners and multiple-mode (MCMM).

The optimization techniques used within CAD have a few salient features. They are based on transformation of an optimization problem to a relevant graph formulation or mathematical formulation. Special properties or structures of the optimization problem are used to enhance the efficiency of the solution approach or to improve the quality of the synthesized solution. These features are also relevant to problems encountered in emerging domains, as these problems also are large and complex. I will wrap up the presentation by showing how the problem of routing droplets on a biochip and load balancing for cloud computing share similar challenges as encountered in VLSI CAD.

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Rickard Ewetz is a Ph.D. candidate at the ECE department at Purdue University. He obtained a combined bachelor and masters degree in Applied Physics and Electrical Engineering from Linkoping University in Sweden in 2011. He was the recipient of the “Scania Student” fellowship in 2010 and he received the fellowship for “Industrial developments” from the Future of Stockholm Foundation in both 2012 and 2014. His current research interests lie within the broad area of optimization. His dissertation research is focused on CAD for VLSI and in particular on the physical design of clock networks for sequential circuits.