UCF DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCEINCE

Summer 2015 Seminar Series
Presented by the ECE Division

ENERGY-EFFICIENT ARCHITECTURES USING THREE-DIMENTIONAL INTEGRATION AND NEAR-THRESHOLD COMPUTING

FRIDAY JUNE 5, 2015
1:30 PM – HEC 356

Energy constrained computing has become an important design constraint for a wide range of computing paradigms. For example, the exascale goals of the DOE are for a system that achieves an ExaFLOP of performance in a 20MW power budget, setting an ambitious goal of 50 GFLOPS/W. DARPA's PERFECT program has set an even higher goal of 75 GFLOPS/W for future embedded military applications, such as unmanned aerial vehicles. At the same time the emergence of the Internet of Things has continued the need for energy and power constrained computing in the mobile marketplace. This talk will look at two emerging techniques to help improve energy-efficiency for this broad range of computing platforms, three-dimensional (3D) integration and near-threshold computing (NTC). 3D integration allows for high-bandwidth low-latency interconnect from compute to memory and allows architects to explore more efficient memory systems. NTC operation reduces supply voltage to 100-200mV above the threshold voltage of the transistors, allowing for significant improvements in energy-efficiency. This talk will conclude with a description and evaluation of the Centip3De test chip, a 64-Core silicon prototype that explores an architecture that leverages the synergies of 3D and NTC.

DR. RONALD DRESLINSKI, JR.

University of Michigan

Ron Dreslinski received a Ph.D. in computer science and engineering from the University of Michigan, Ann Arbor. Dr. Dreslinski is currently an assistant research scientist at the University of Michigan. His research focuses on architectures that enable emerging low-power circuit techniques.

UCF