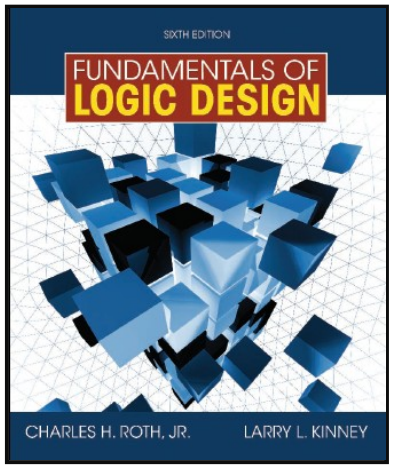
# CHAPTER 18

# CIRCUITS FOR ARITHMETIC OPERATIONS




***This chapter in the book includes:***

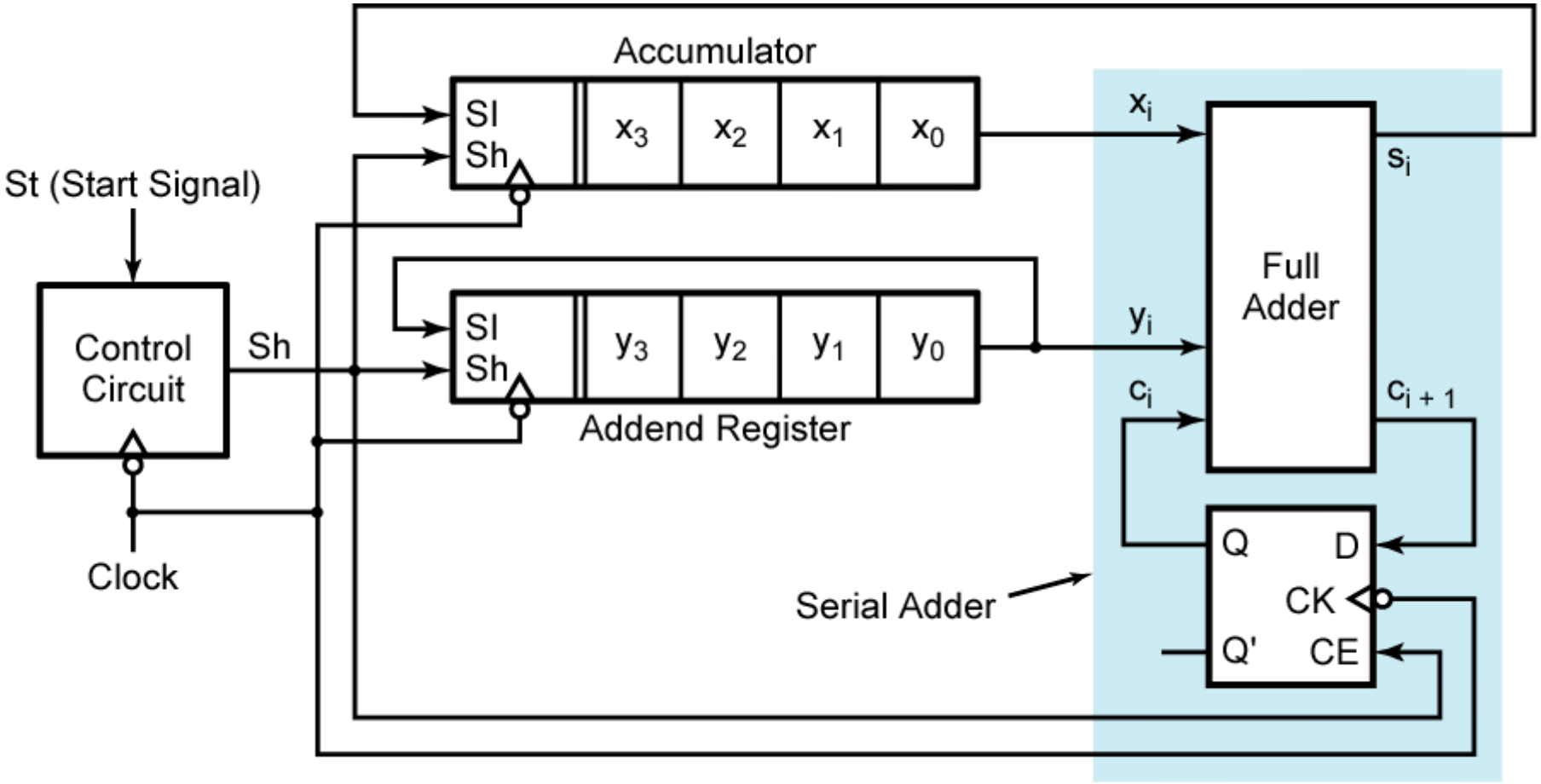



***Figure 18-1:*** **Block Diagram for Serial Adder with Accumulator**

***Figure 18-2ab:***

# Operation of Serial Adder

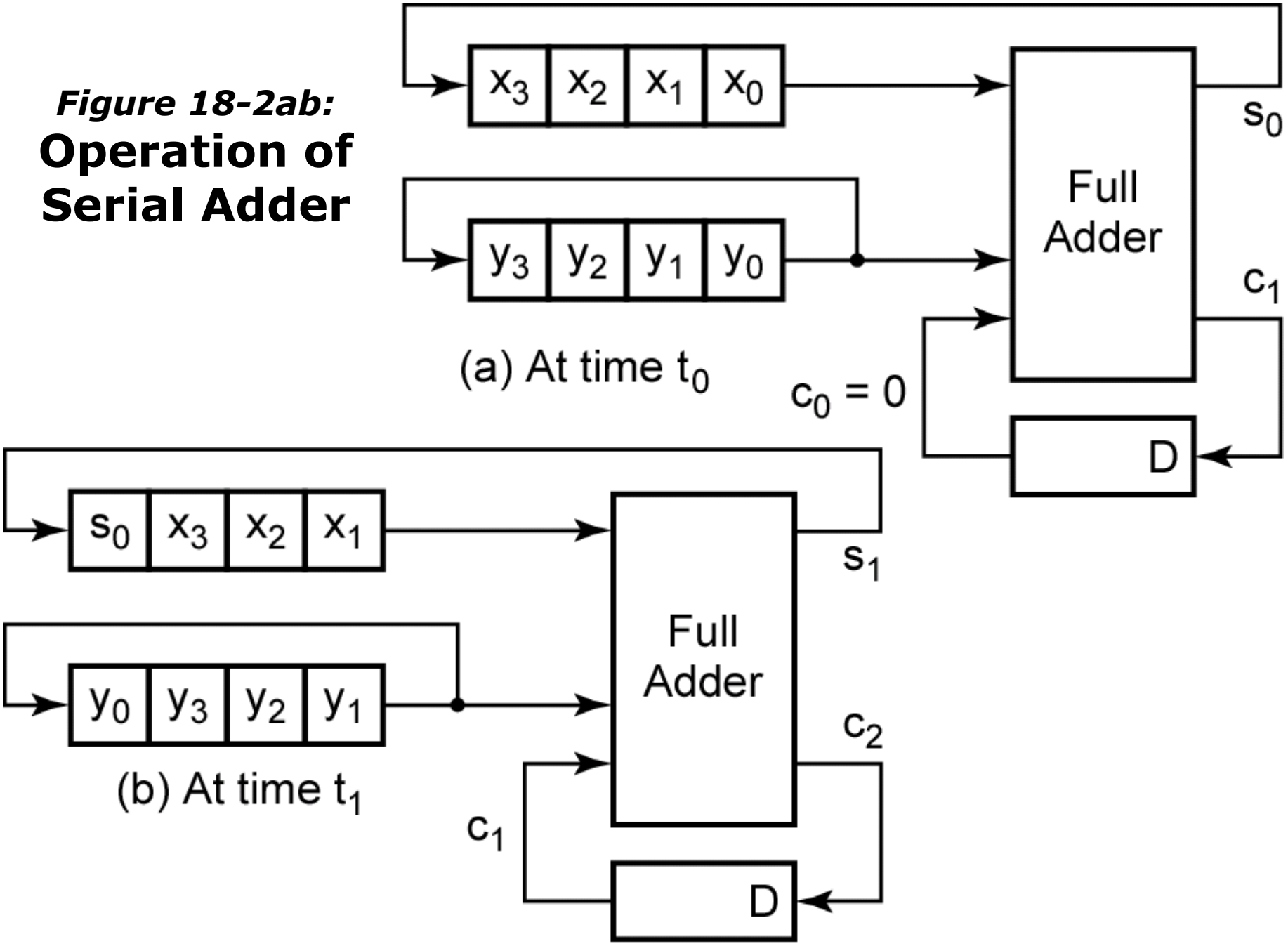
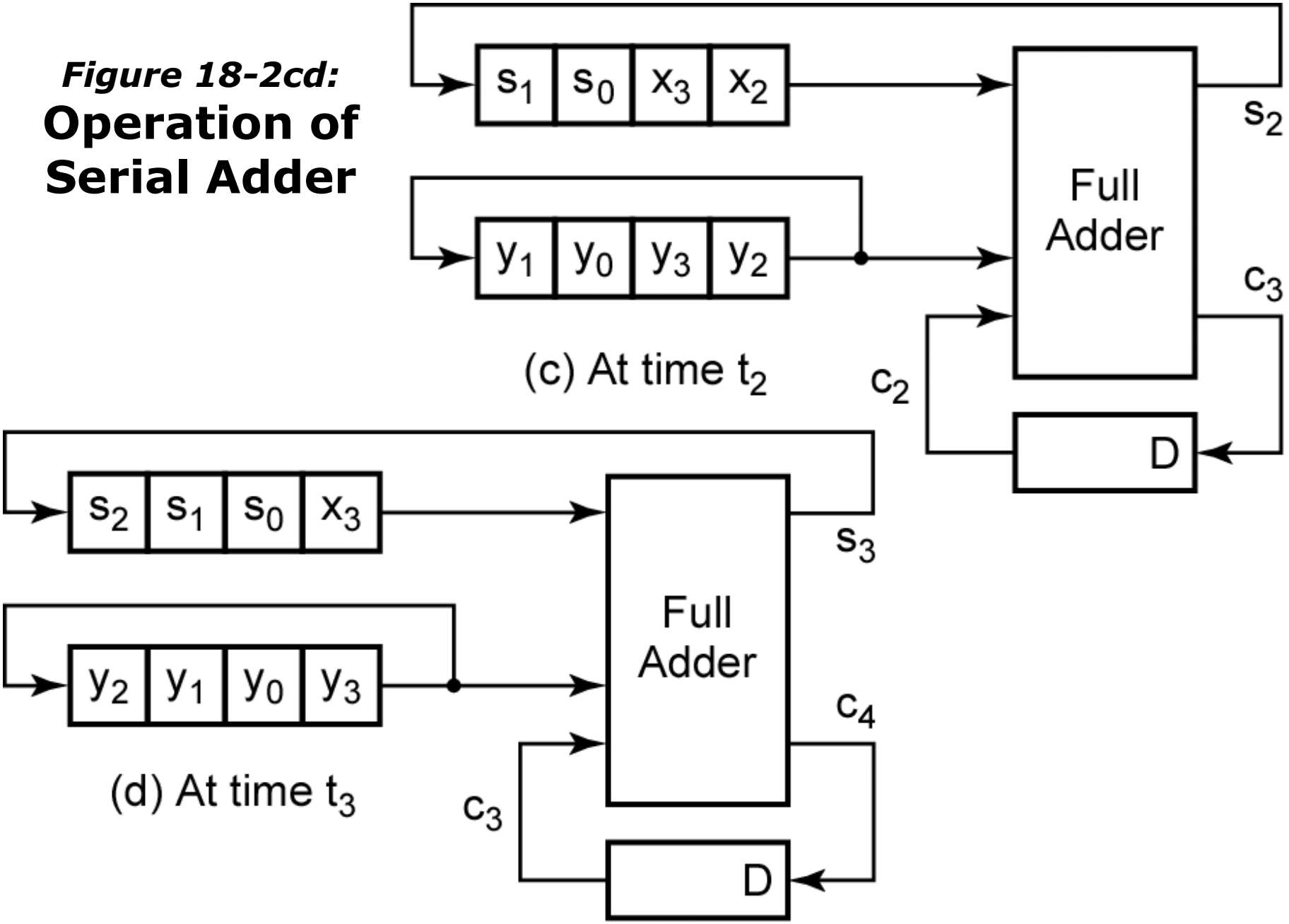


***Figure 18-2cd:***

# Operation of Serial Adder



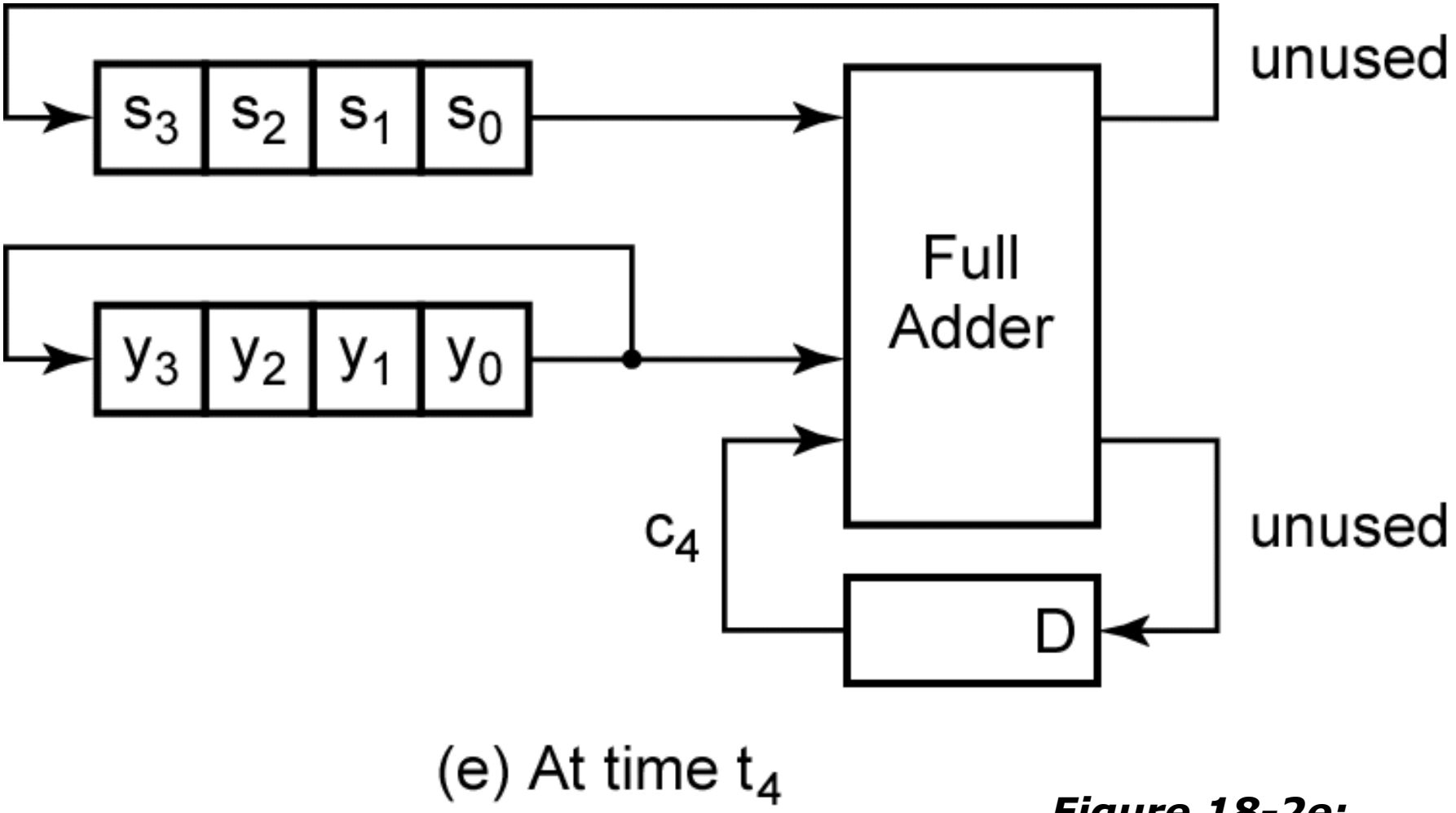
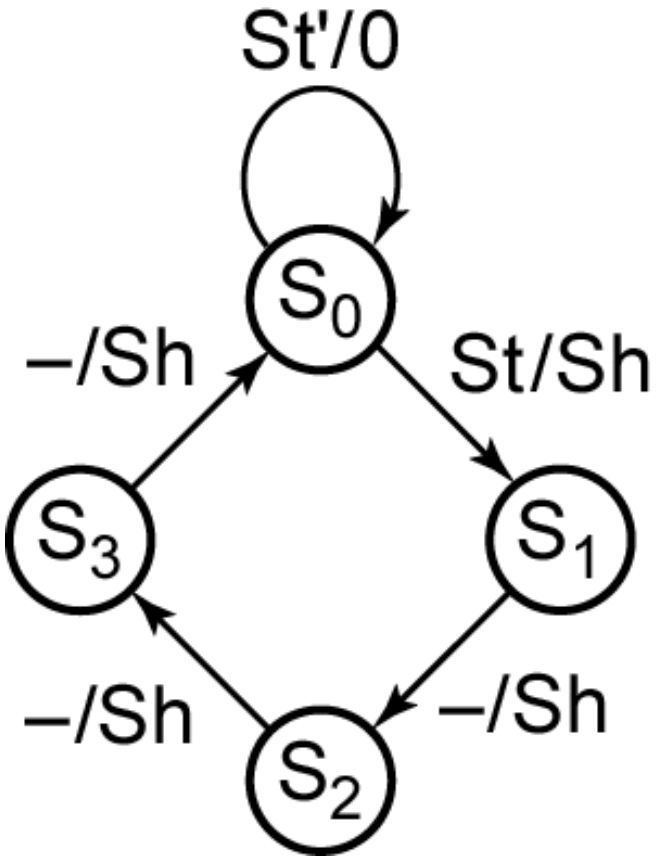



***Figure 18-2e:***
**Operation of Serial Adder**

## Table 18-1 Operation of Serial Adder

| | $X$ | $Y$ | $C_i$ | $S_i$ | $C_i^+$ |
|---|---|---|---|---|---|
| $t_0$ | 0101 | 0111 | 0 | 0 | 1 |
| $t_1$ | 0010 | 1011 | 1 | 0 | 1 |
| $t_2$ | 0001 | 1101 | 1 | 1 | 1 |
| $t_3$ | 1000 | 1110 | 1 | 1 | 0 |
| $t_4$ | 1100 | 0111 | 0 | (1) | (0) |




| | Next State | | Sh | |
|---|---|---|---|---|
| | St = 0 | 1 | 0 | 1 |
| $S_0$ | $S_0$ | $S_1$ | 0 | 1 |
| $S_1$ | $S_2$ | $S_2$ | 1 | 1 |
| $S_2$ | $S_3$ | $S_3$ | 1 | 1 |
| $S_3$ | $S_0$ | $S_0$ | 1 | 1 |

***Figure 18-3:*** **State Graph for Serial Adder Control**

| | AB | $A^+B^+$ | |
|---|---|---|---|
| | | 0 | 1 |
| $S_0$ | 00 | 00 | 01 |
| $S_1$ | 01 | 10 | 10 |
| $S_2$ | 10 | 11 | 11 |
| $S_3$ | 11 | 00 | 00 |

***Figure 18-4a:*** **Derivation of Control Circuit Equations**

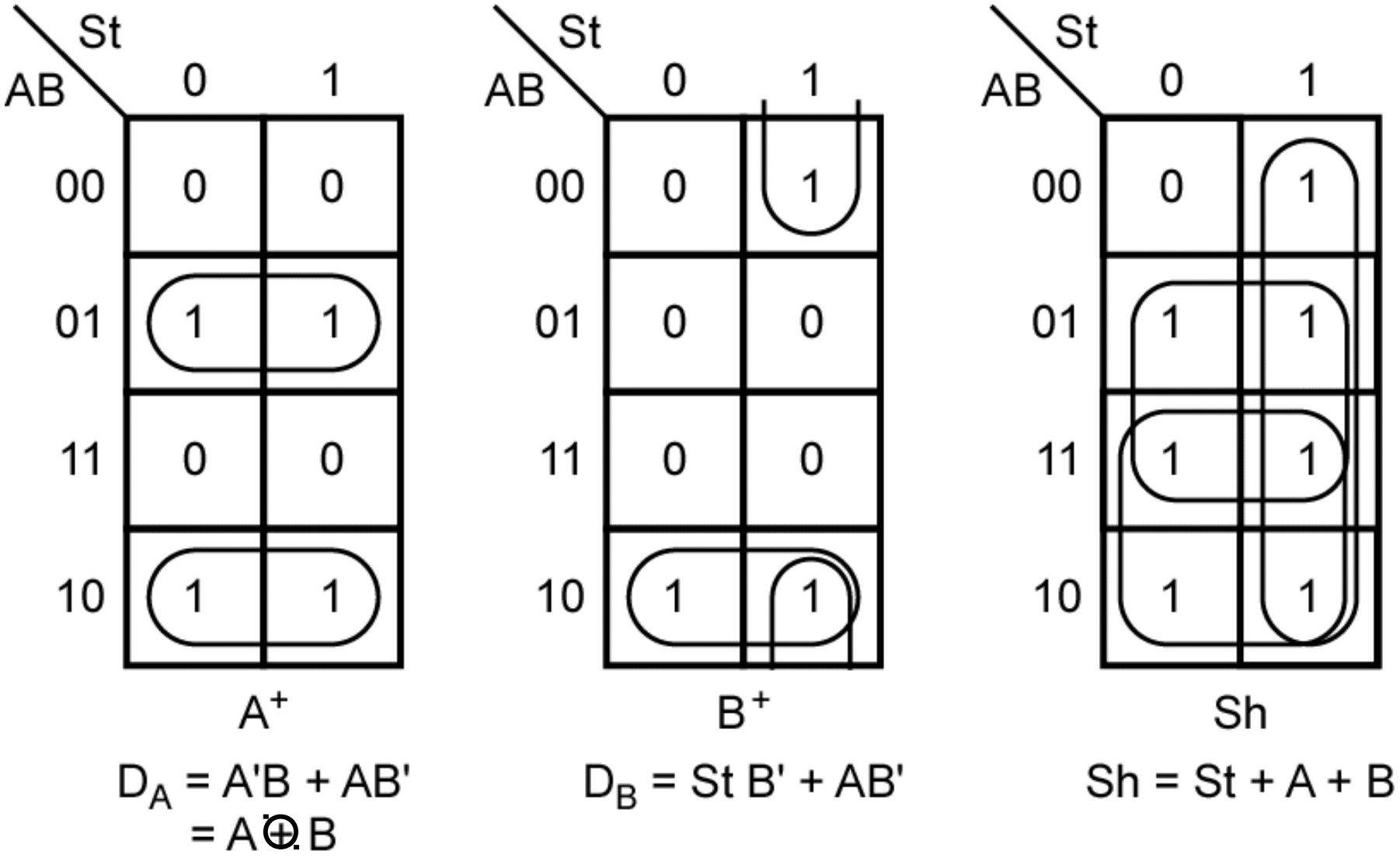



***Figure 18-4b:*** **Derivation of Control Circuit Equations**

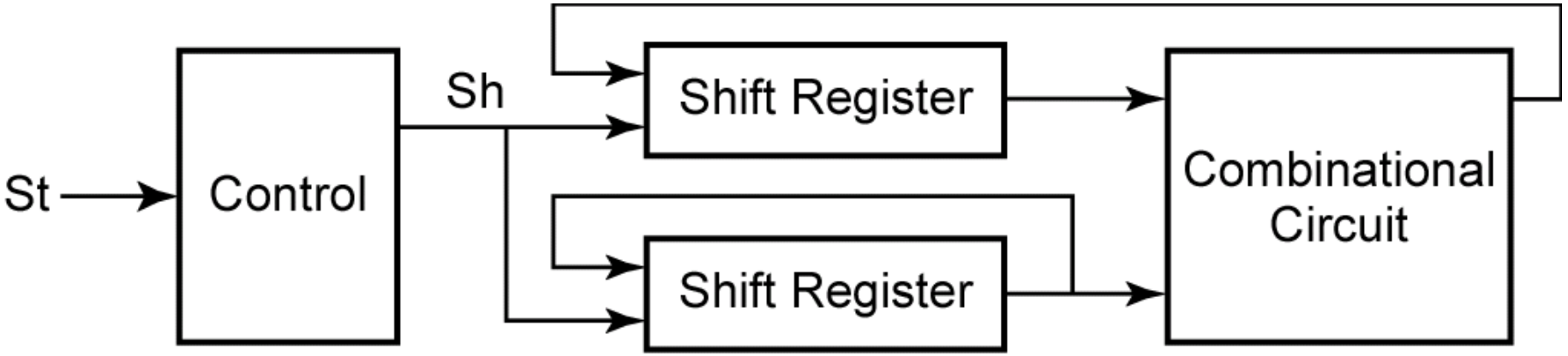



***Figure 18-5:*** **Typical Serial Processing Unit**

The output bits from the shift register are inputs to a combinational circuit.

The combinational circuit generates at least one output bit which is fed into the input of a shift register.

When the active clock edge occurs, this bit is stored in the first bit of the shift register at the same time the register bits are shifted to the right.

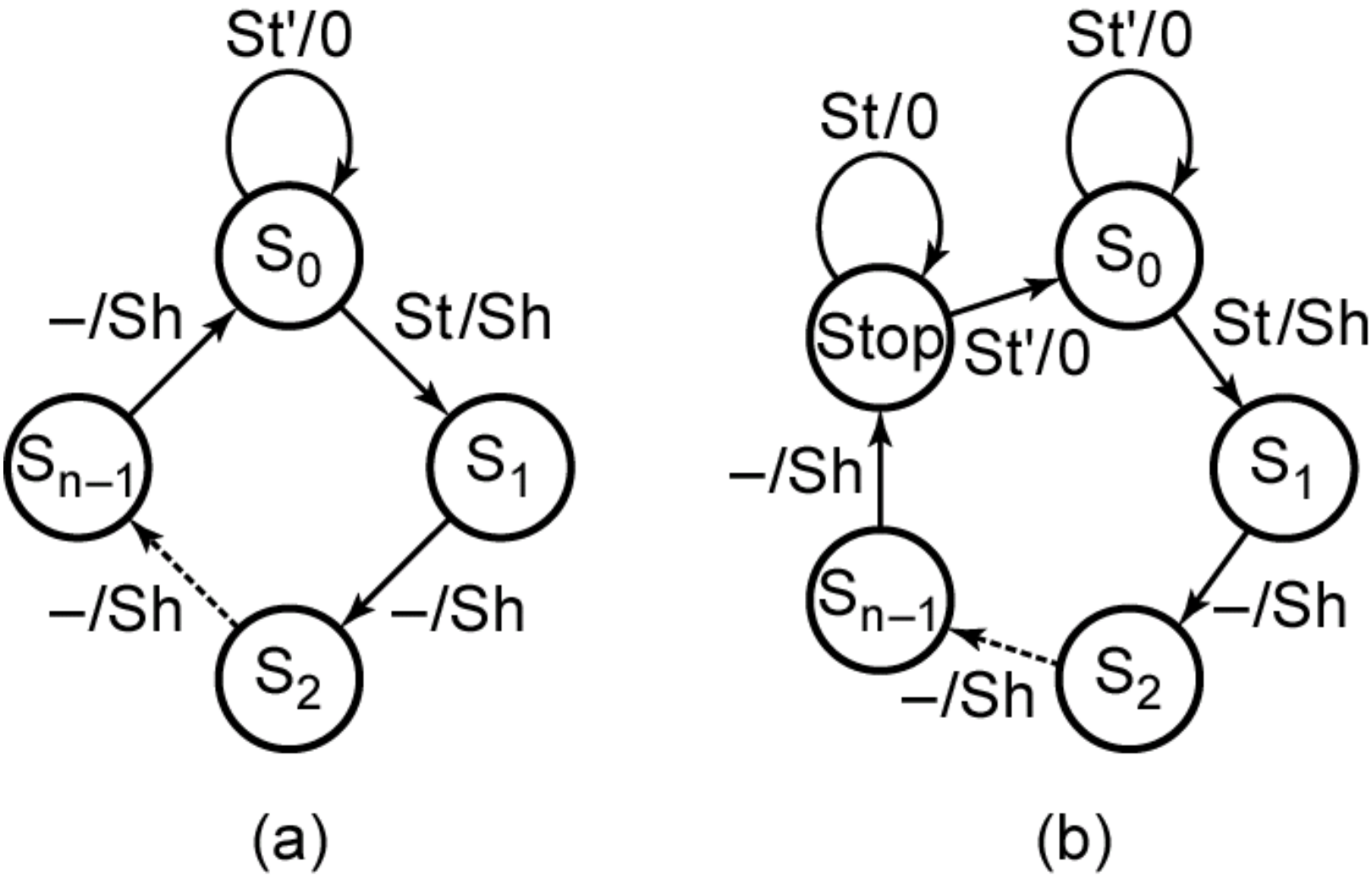
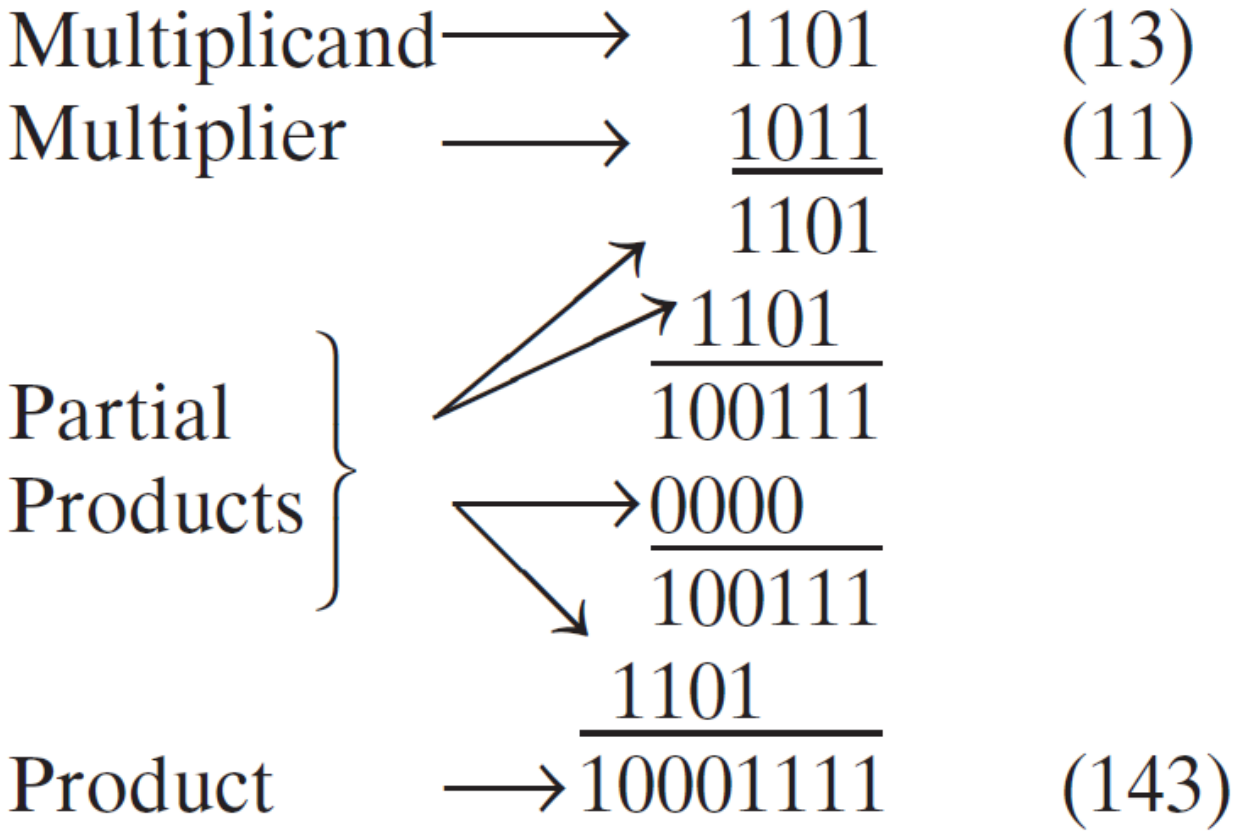



***Figure 18-6:*** **State Graphs for Serial Processing Unit**

# Design of Parallel Multiplier

Multiplication with partial products added in as soon as they are formed:




**Section 18.2 (p. 598)**

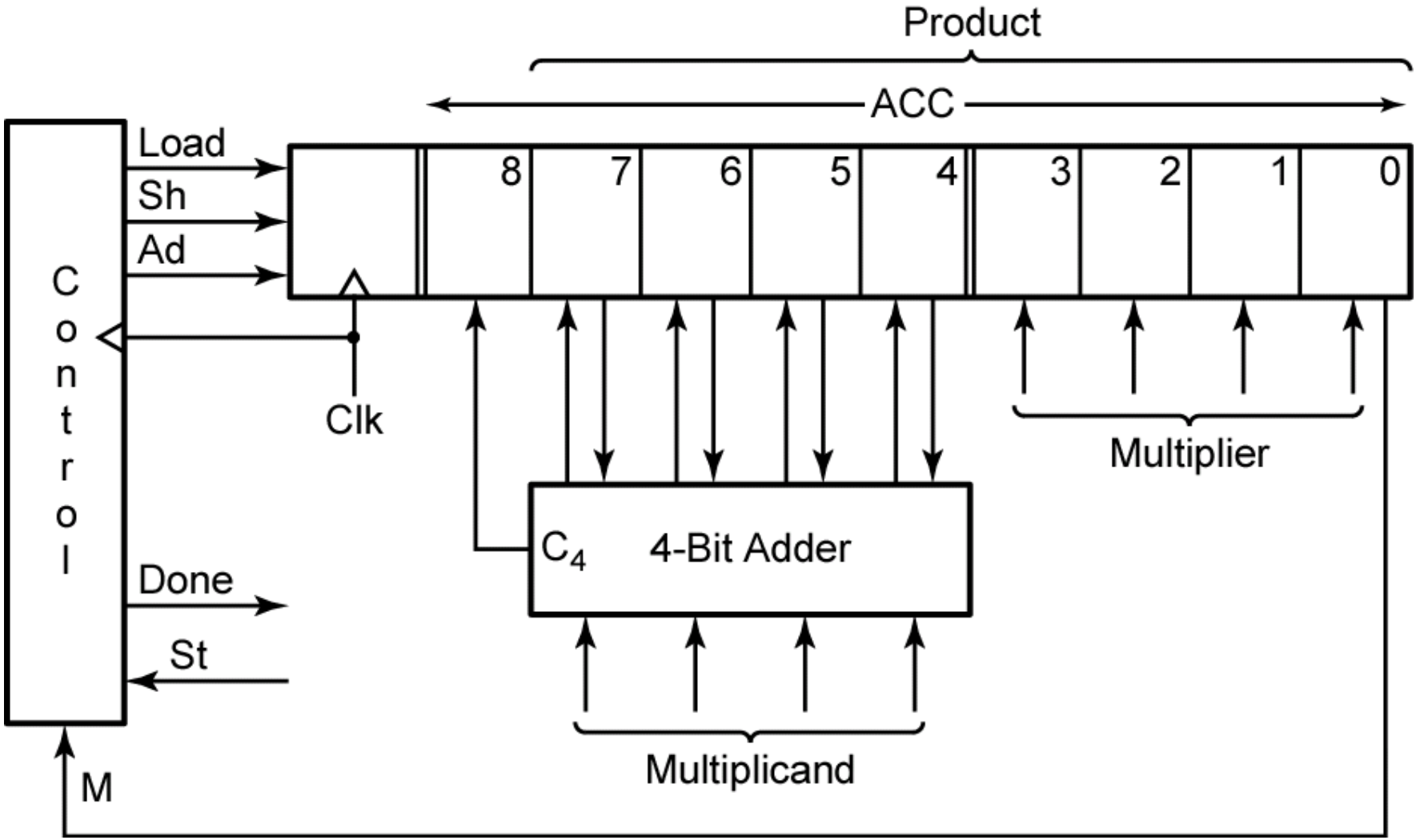
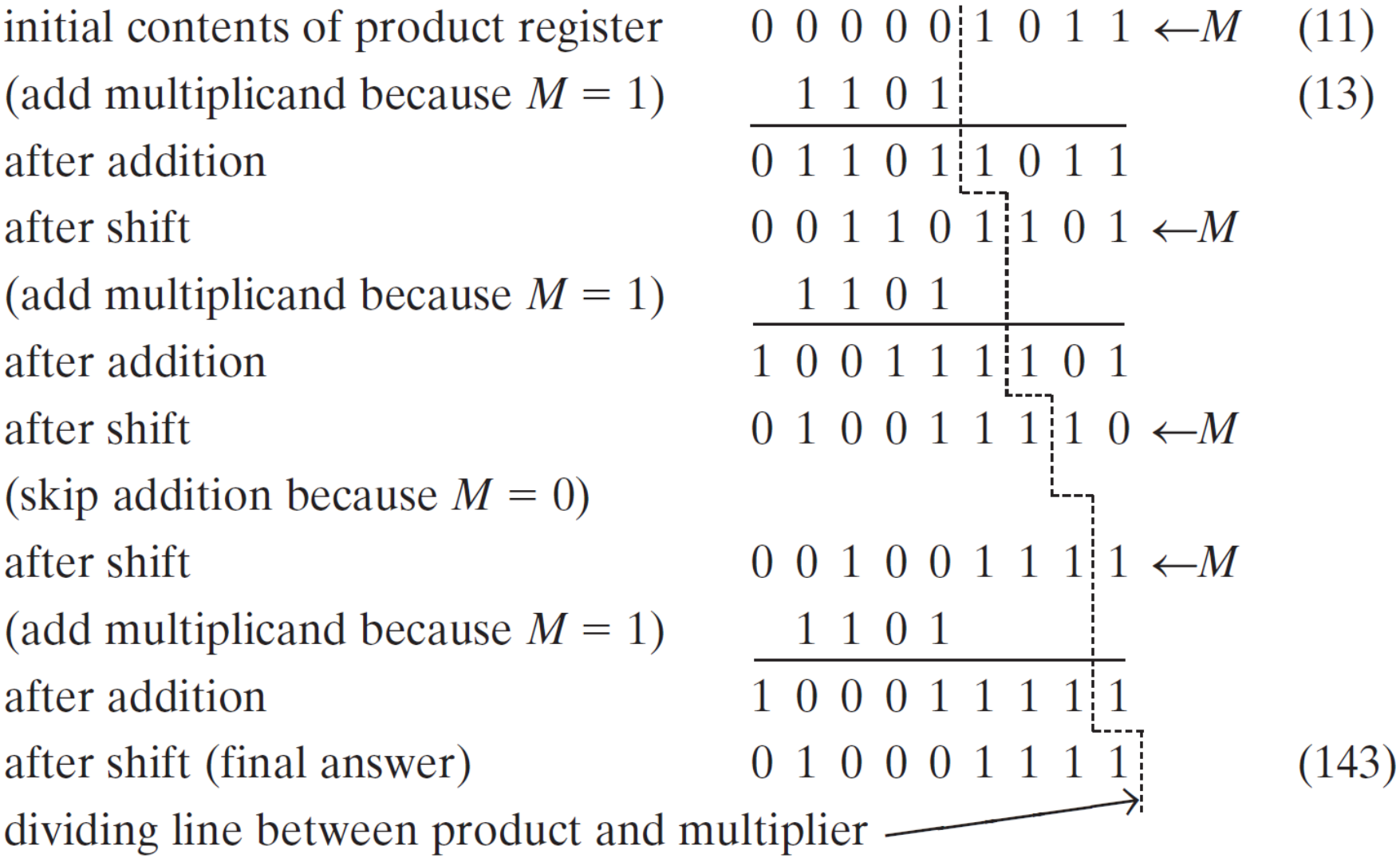



***Figure 18-7:*** **Block Diagram for Parallel Binary Multiplier**

# Parallel Binary Multiplication




**Section 18.2 (p. 600)**

4-bit Multiplier

4-bit Multiplicand

8-bit Product

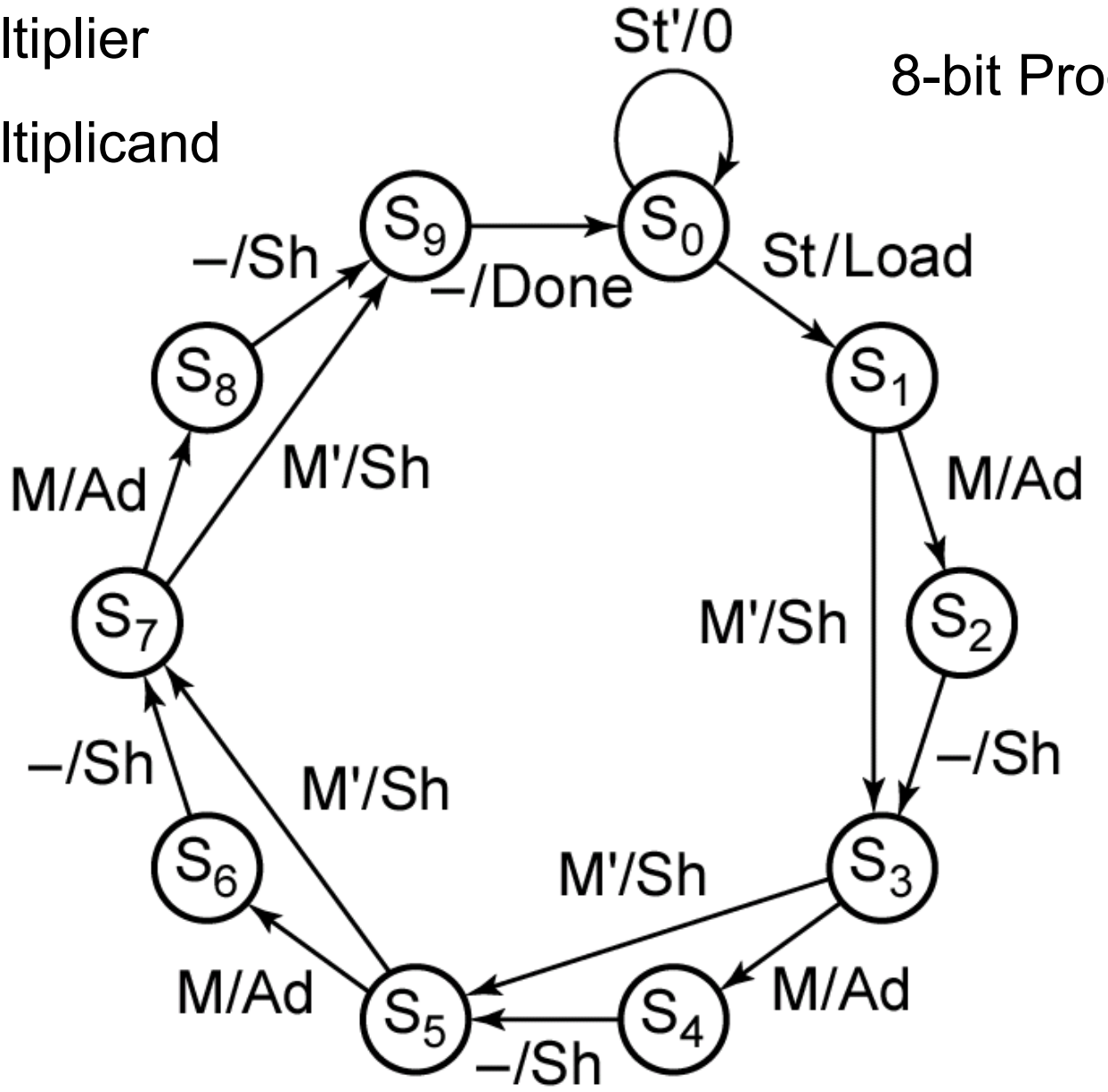
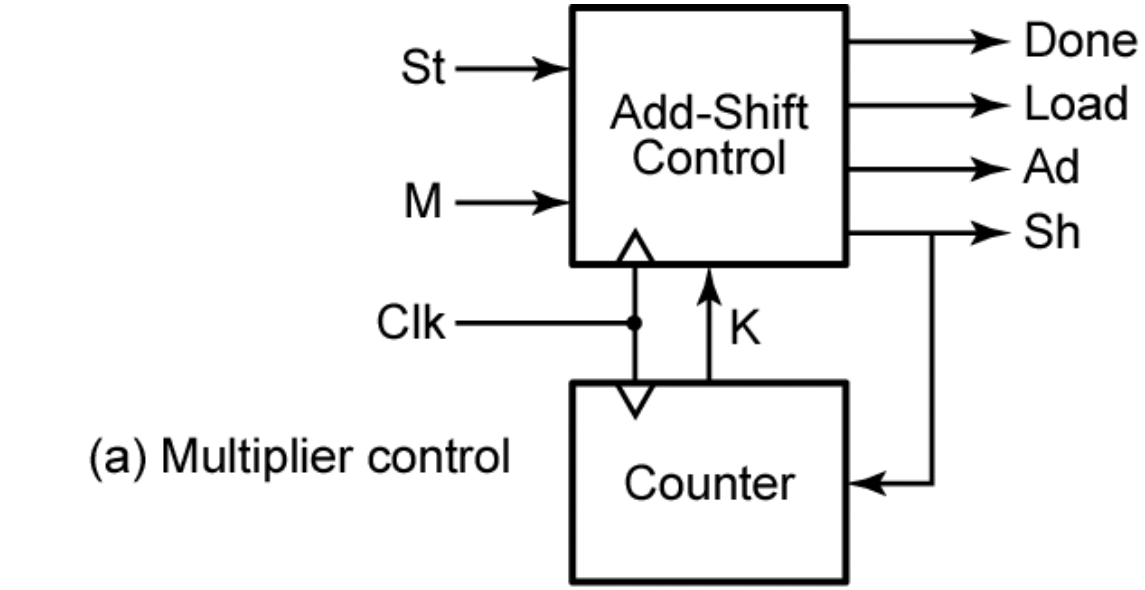
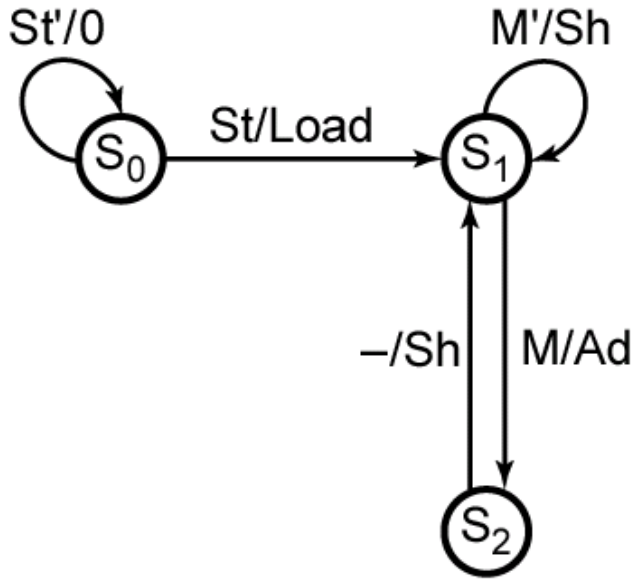



***Figure 18-8:*** **State Graph for Multiplier Control**

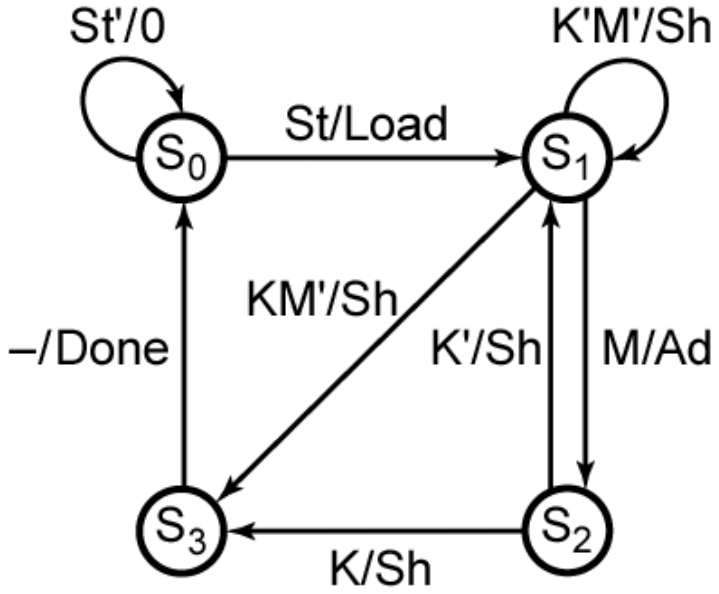



(a) Multiplier control

**Figure 18-9**




(b) State graph for add-shift control



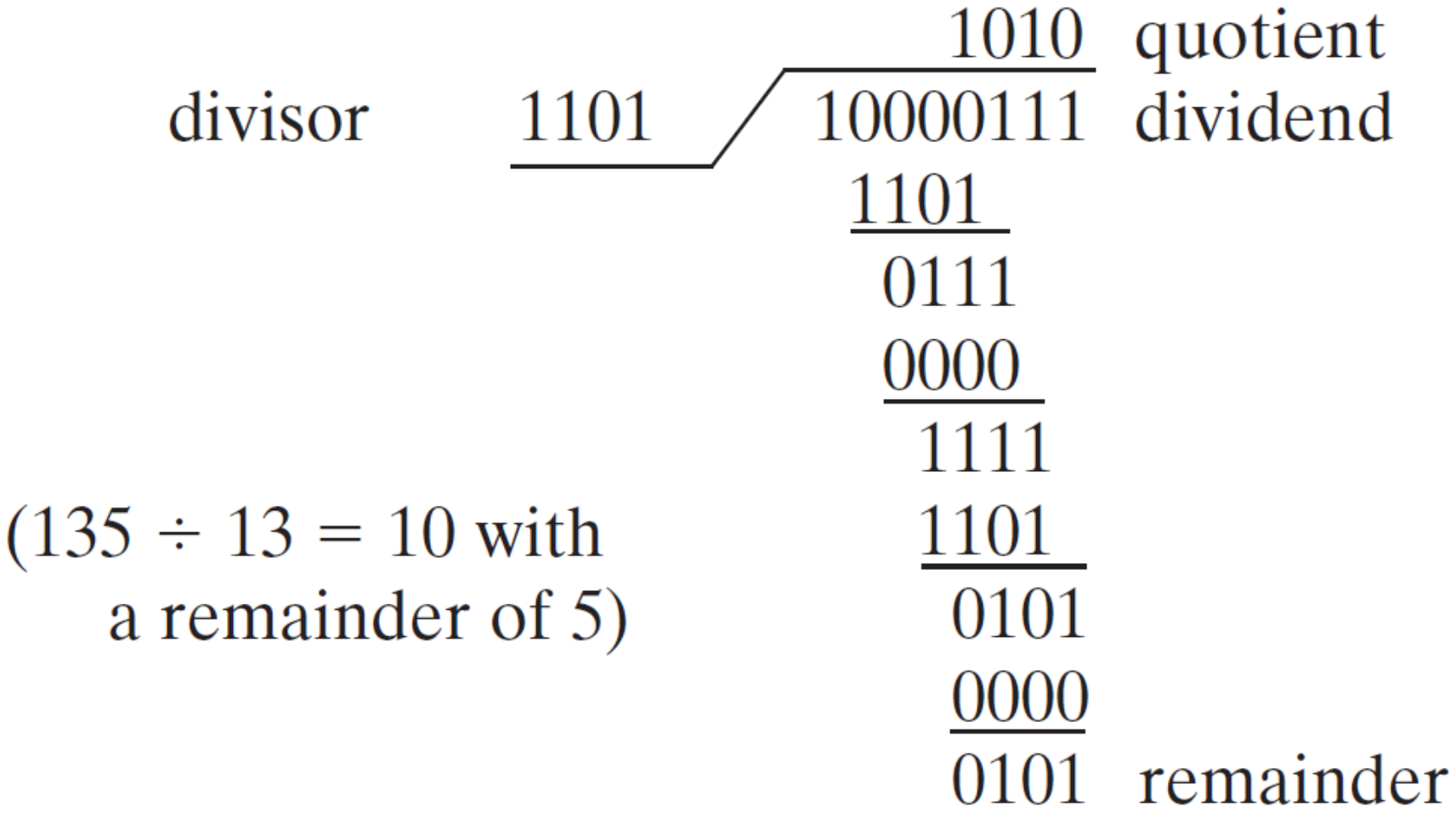

(c) Final state graph for add-shift control

# Table 18.2 Operation of a Multiplier Using a Counter

| Time | State | Counter | Product Register | St | M | K | Load | Ad | Sh | Done |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_0$ | $S_0$ | 00 | 000000000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $t_1$ | $S_0$ | 00 | 000000000 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| $t_2$ | $S_1$ | 00 | 000001011 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| $t_3$ | $S_2$ | 00 | 011011011 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| $t_4$ | $S_1$ | 01 | 001101101 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| $t_5$ | $S_2$ | 01 | 100111101 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| $t_6$ | $S_1$ | 10 | 010011110 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| $t_7$ | $S_1$ | 11 | 001001111 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| $t_8$ | $S_2$ | 11 | 100011111 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| $t_9$ | $S_3$ | 00 | 010001111 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

# Design of Binary Divider

Example of division process:




**Section 18.3 (p. 602)**

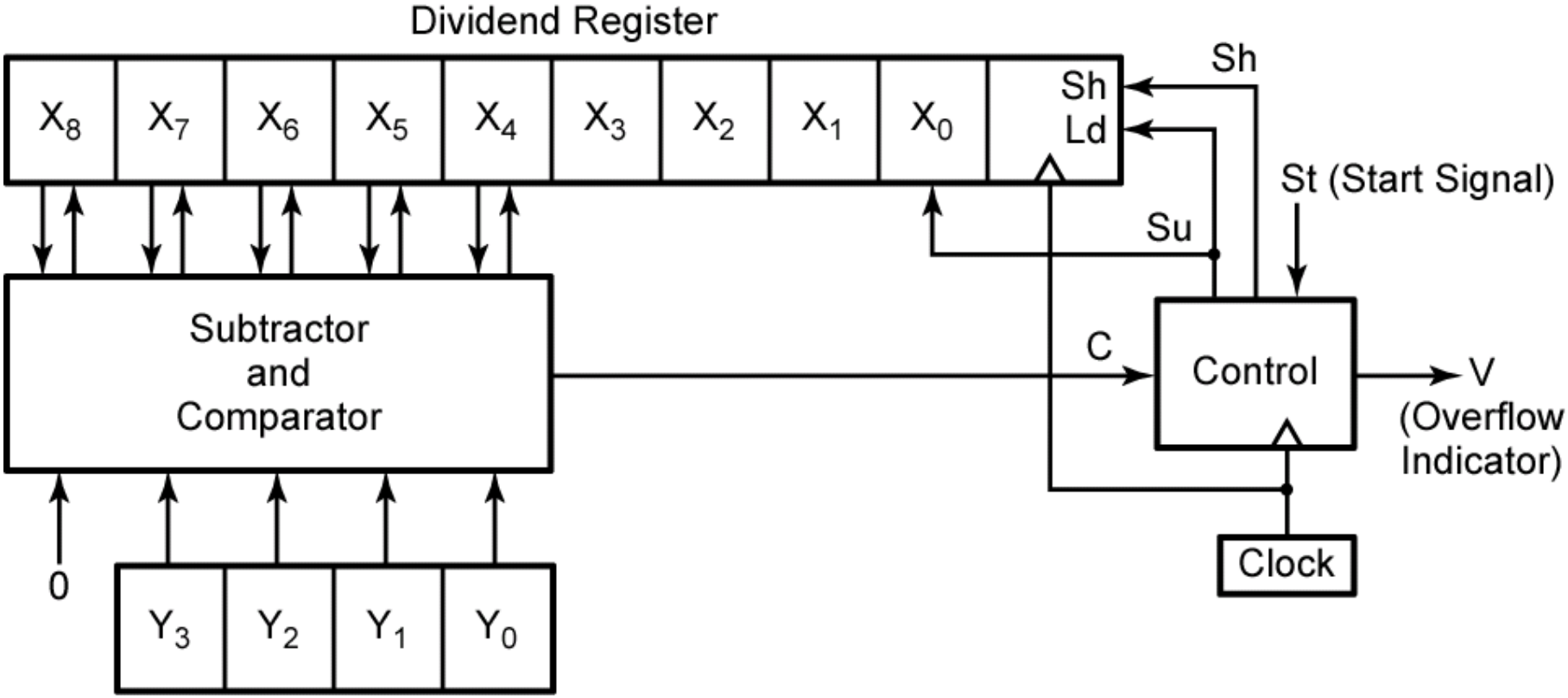
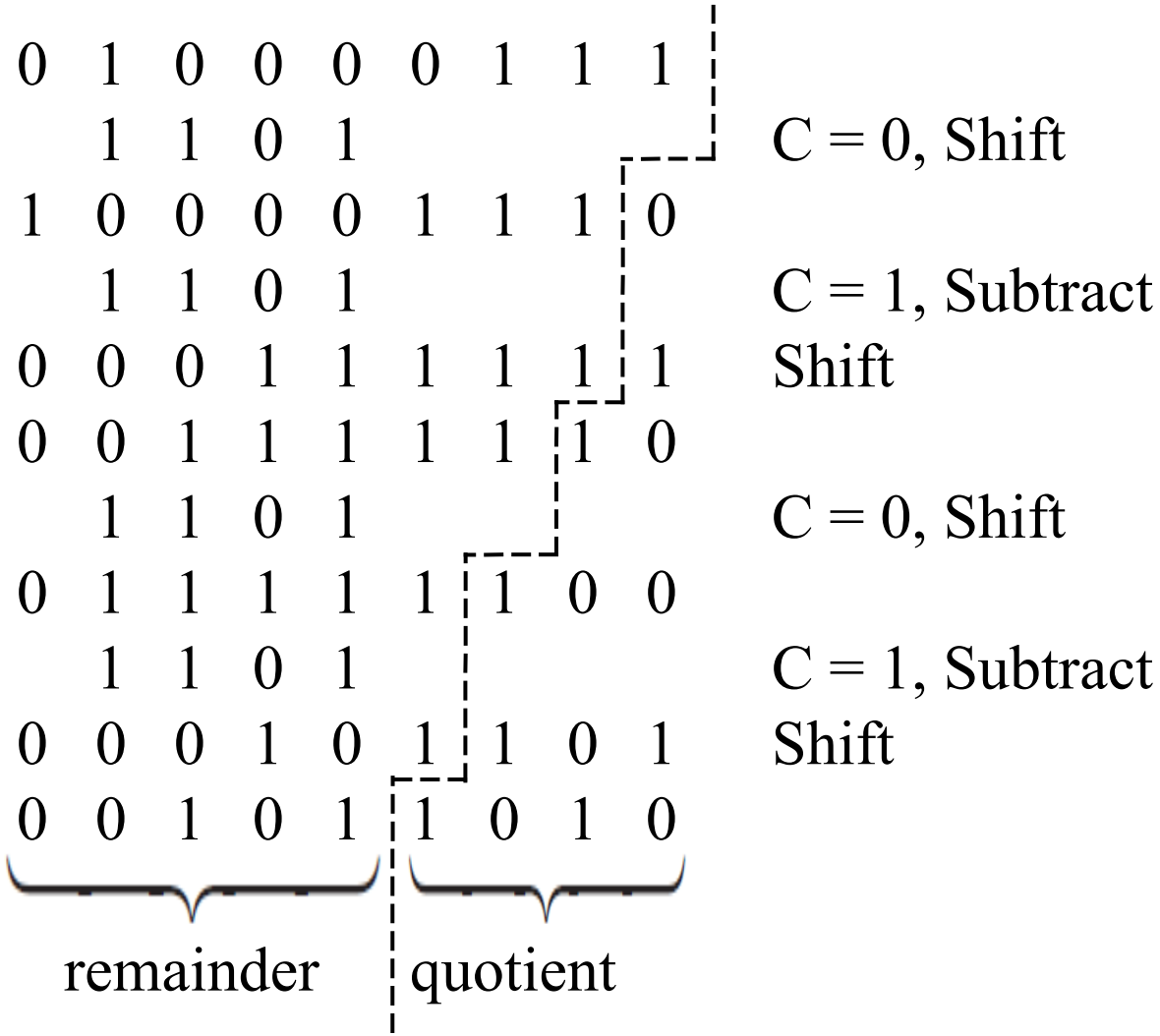



***Figure 18-10:*** **Block Diagram for Parallel Binary Divider**



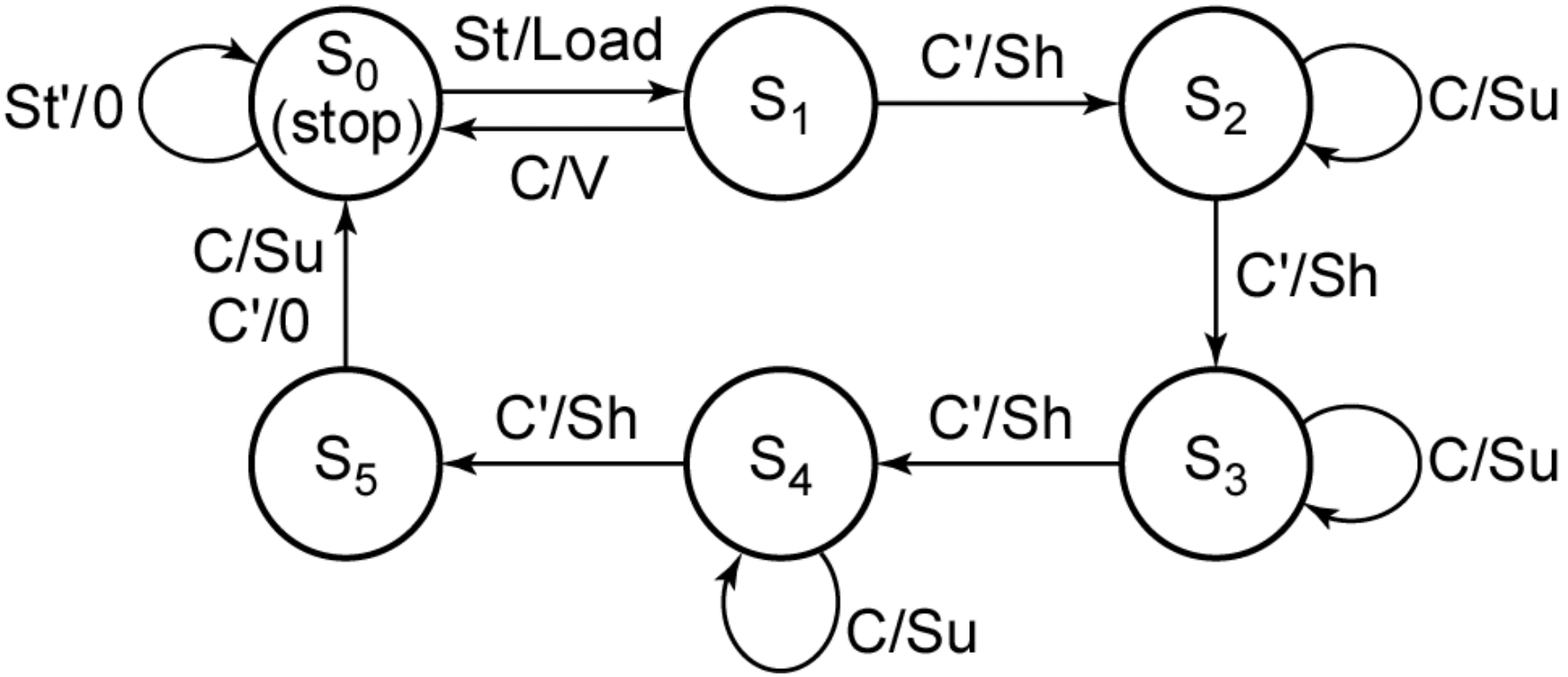
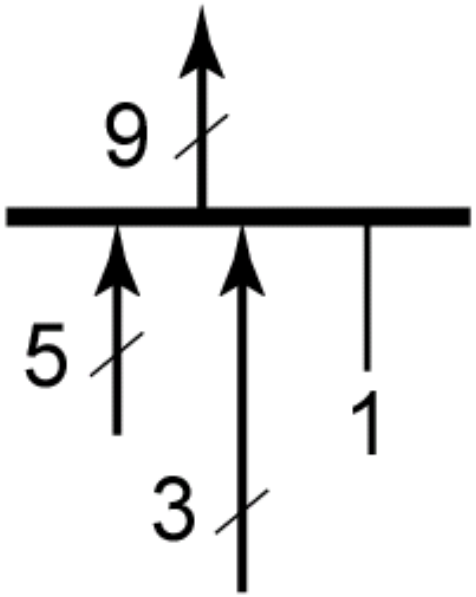
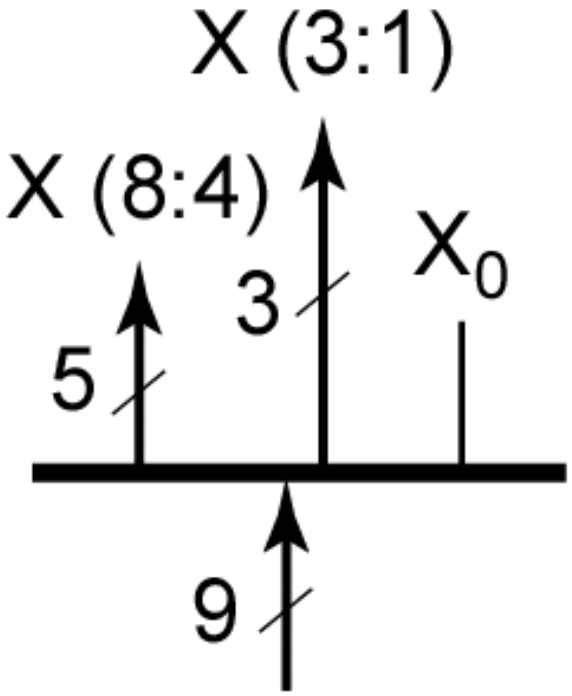



***Figure 18-11:*** **State Graph for Divider Control Circuit**




Bus Merger




Bus Splitter

**Section 18.3 (p. 606)**

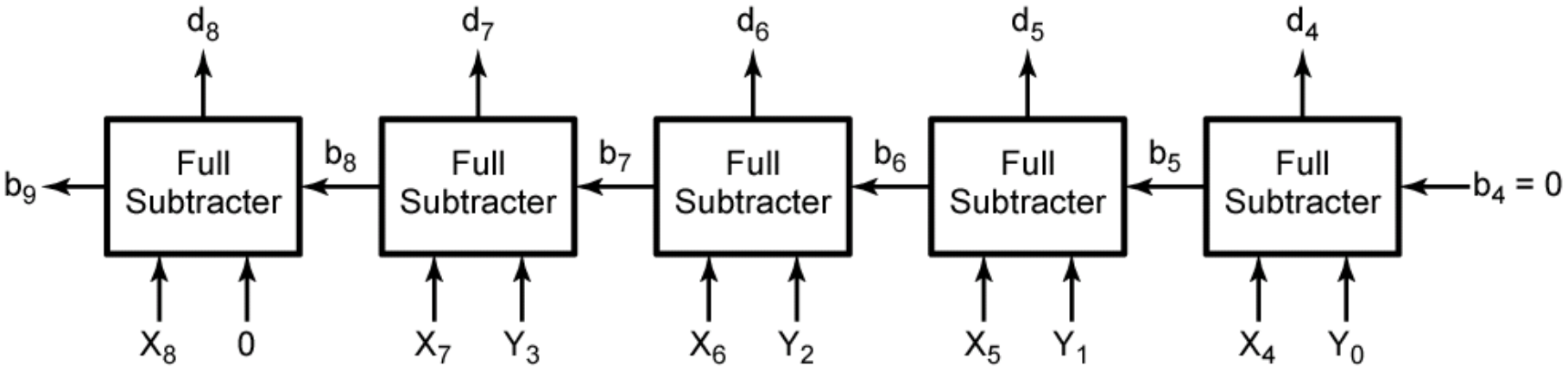



***Figure 18-12:*** **Logic Diagram for 5-Bit Subtracter**

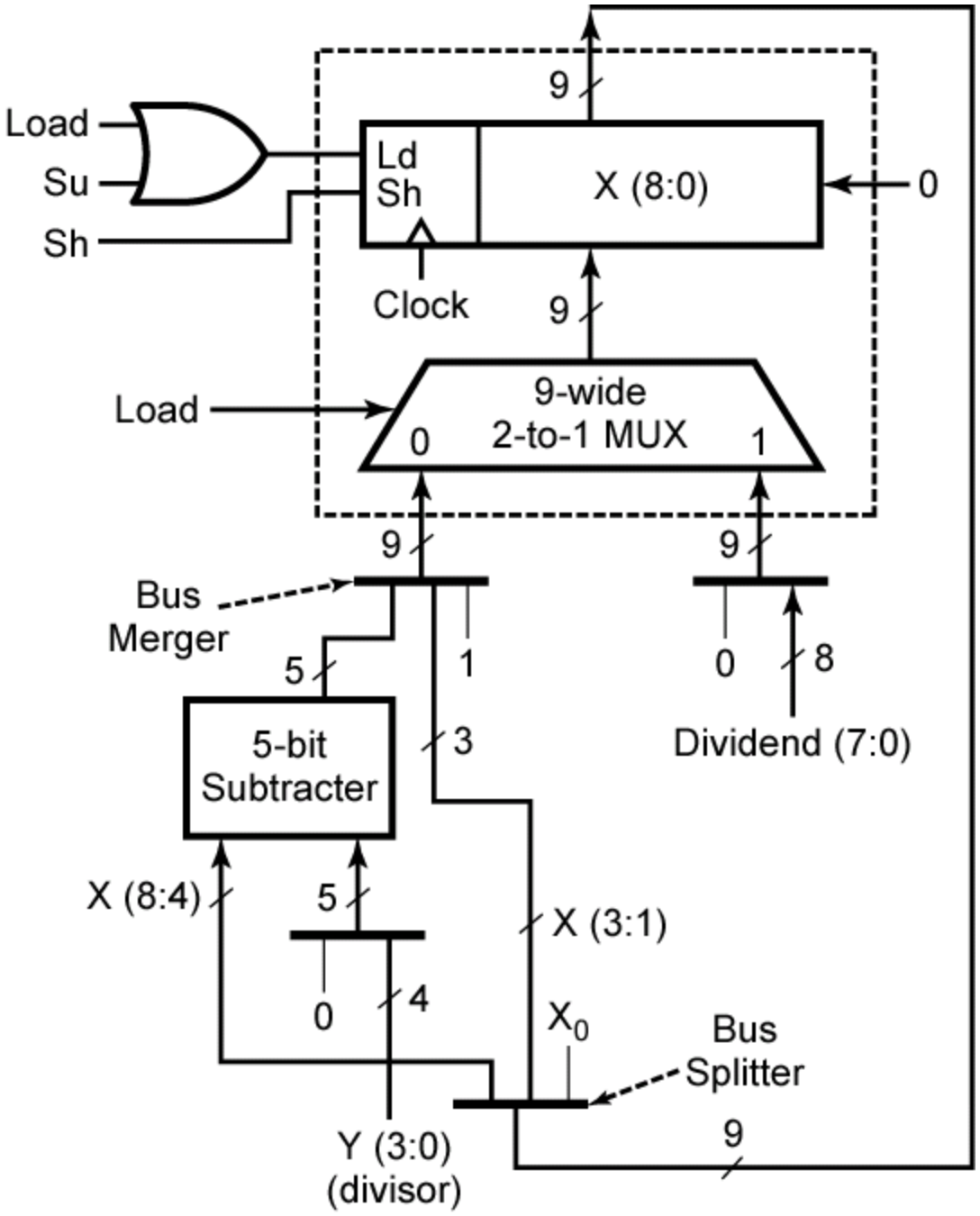



***Figure 18-13:***

**Block Diagram for Divider Using Bus Notation**