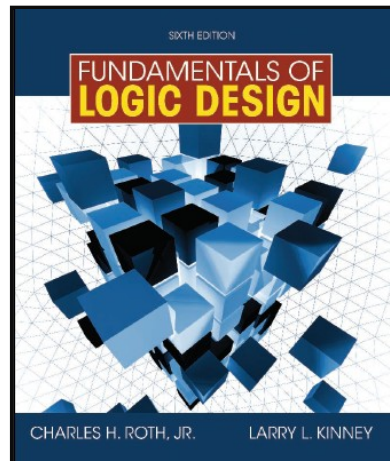


CHAPTER 18

CIRCUITS FOR ARITHMETIC OPERATIONS



This chapter in the book includes:

- Objectives
- Study Guide
- 18.1 Serial Adder with Accumulator
- 18.2 Design of a Parallel Multiplier
- 18.3 Design of a Binary Divider
- Programmed Exercises
- Problems

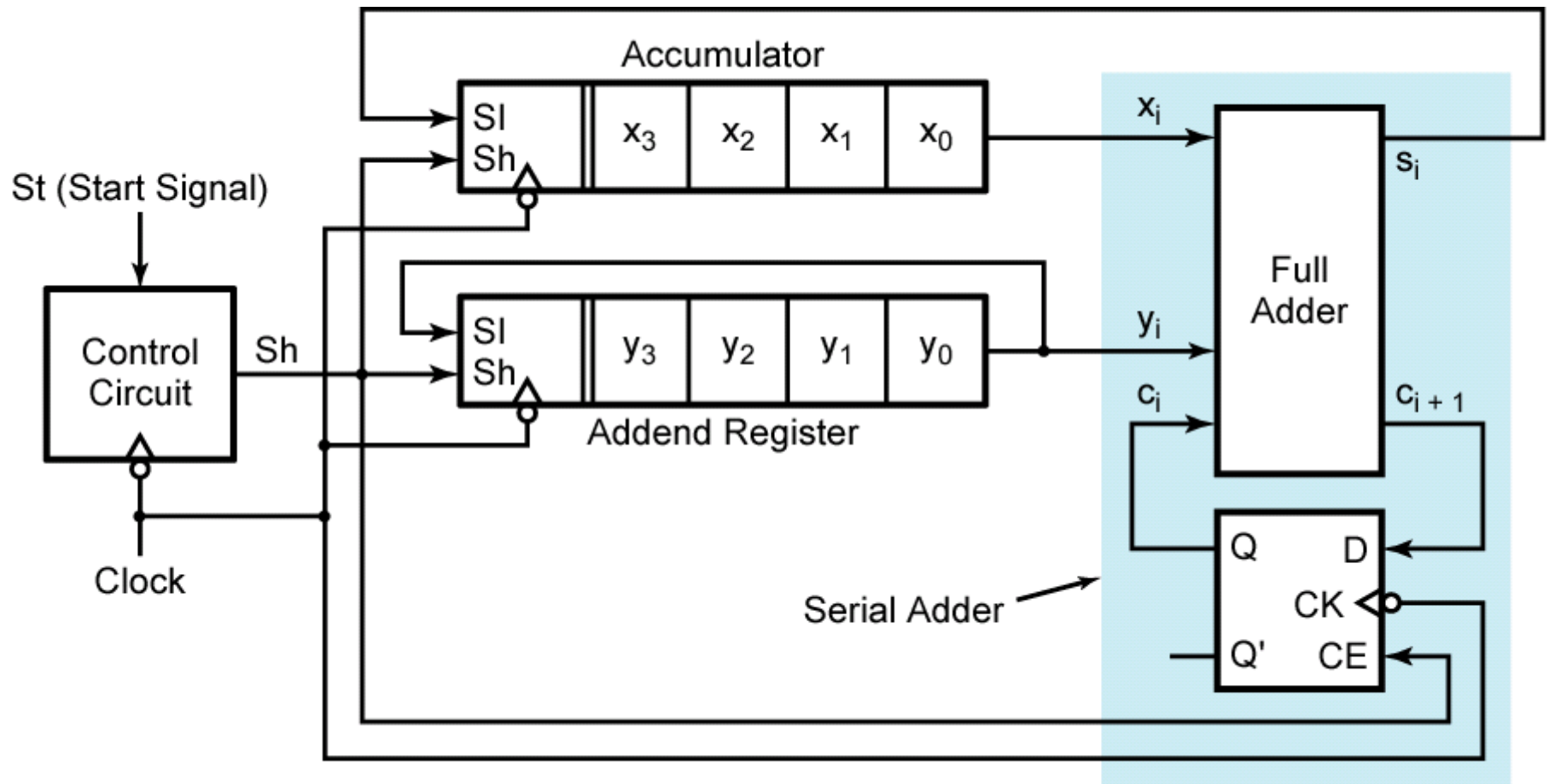


Figure 18-1: Block Diagram for Serial Adder with Accumulator

Figure 18-2ab:
Operation of
Serial Adder

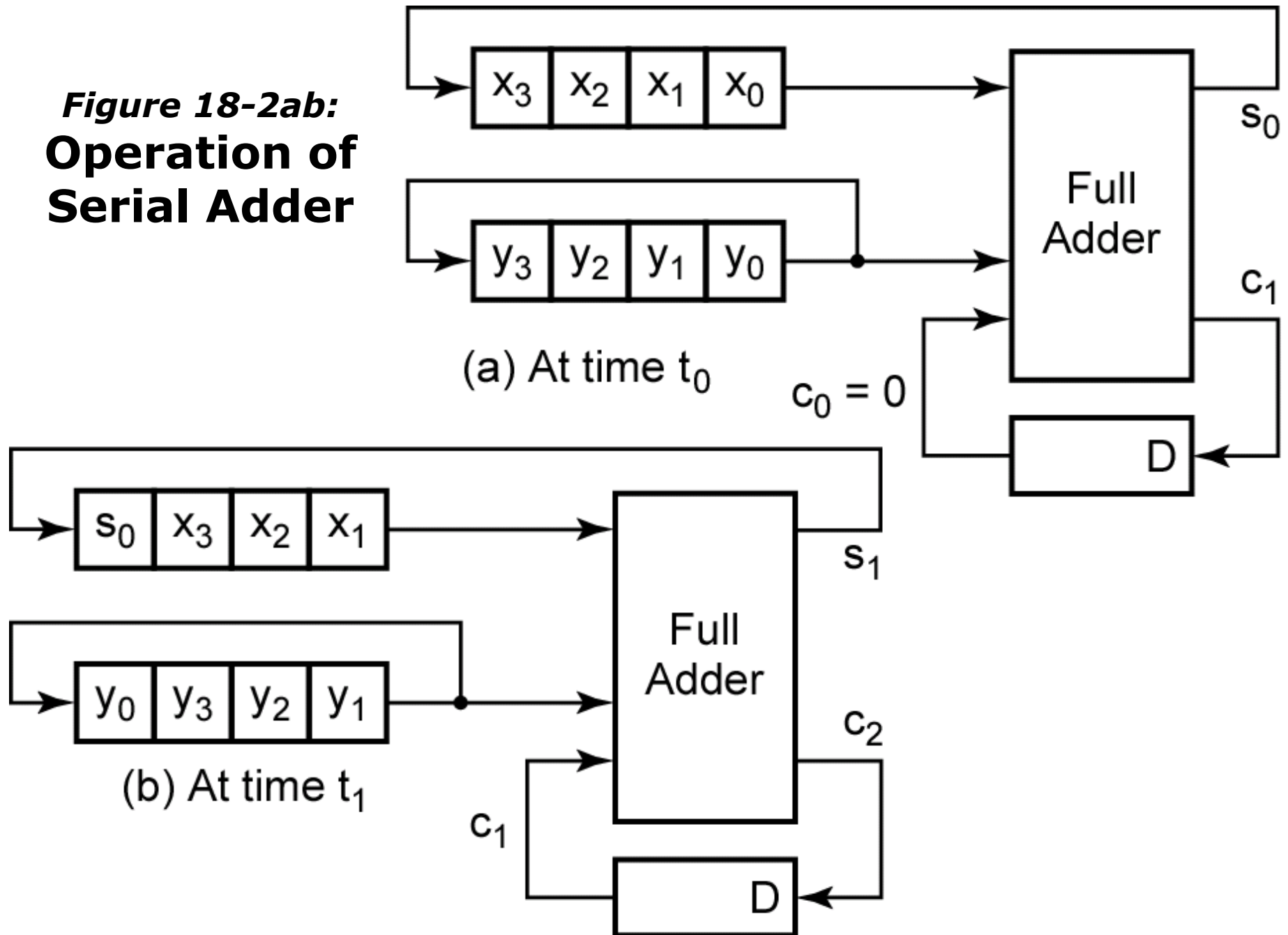
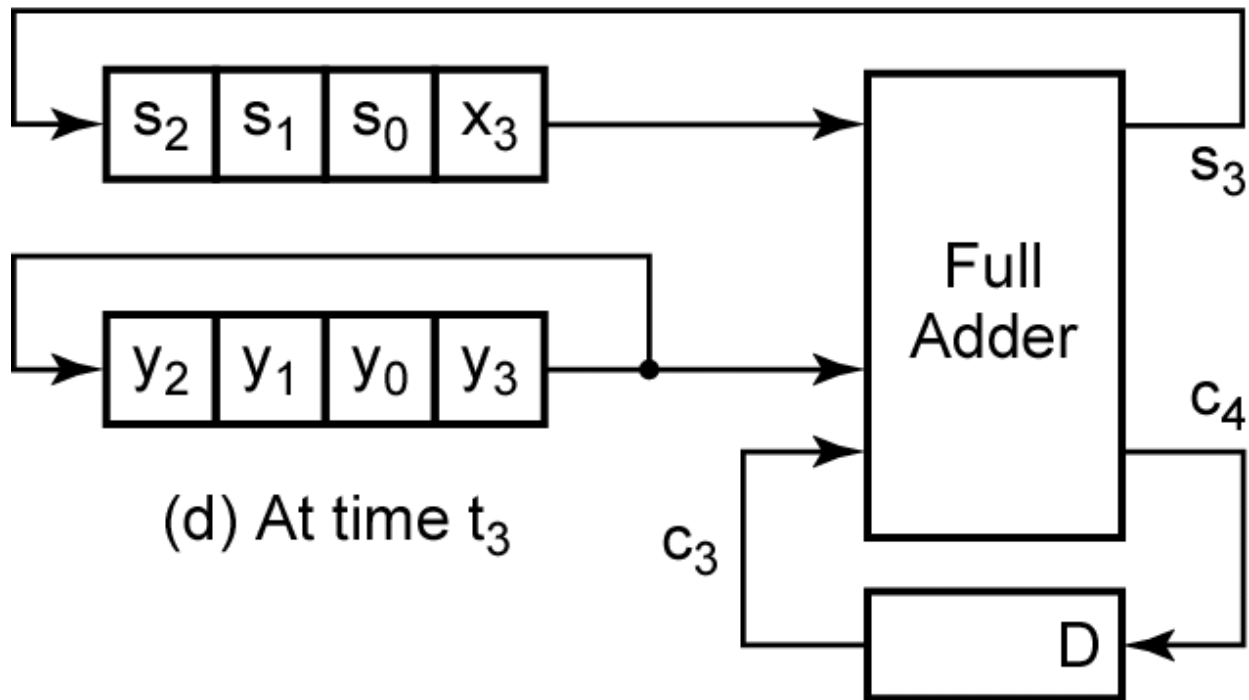
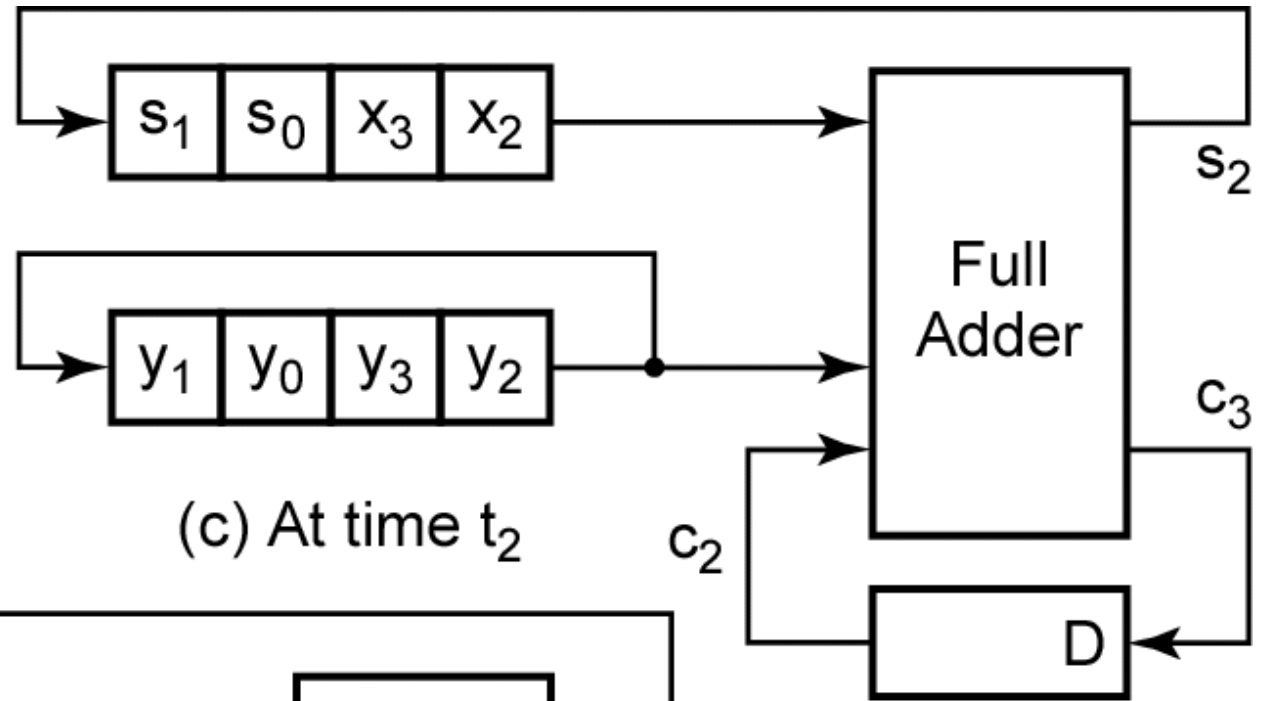
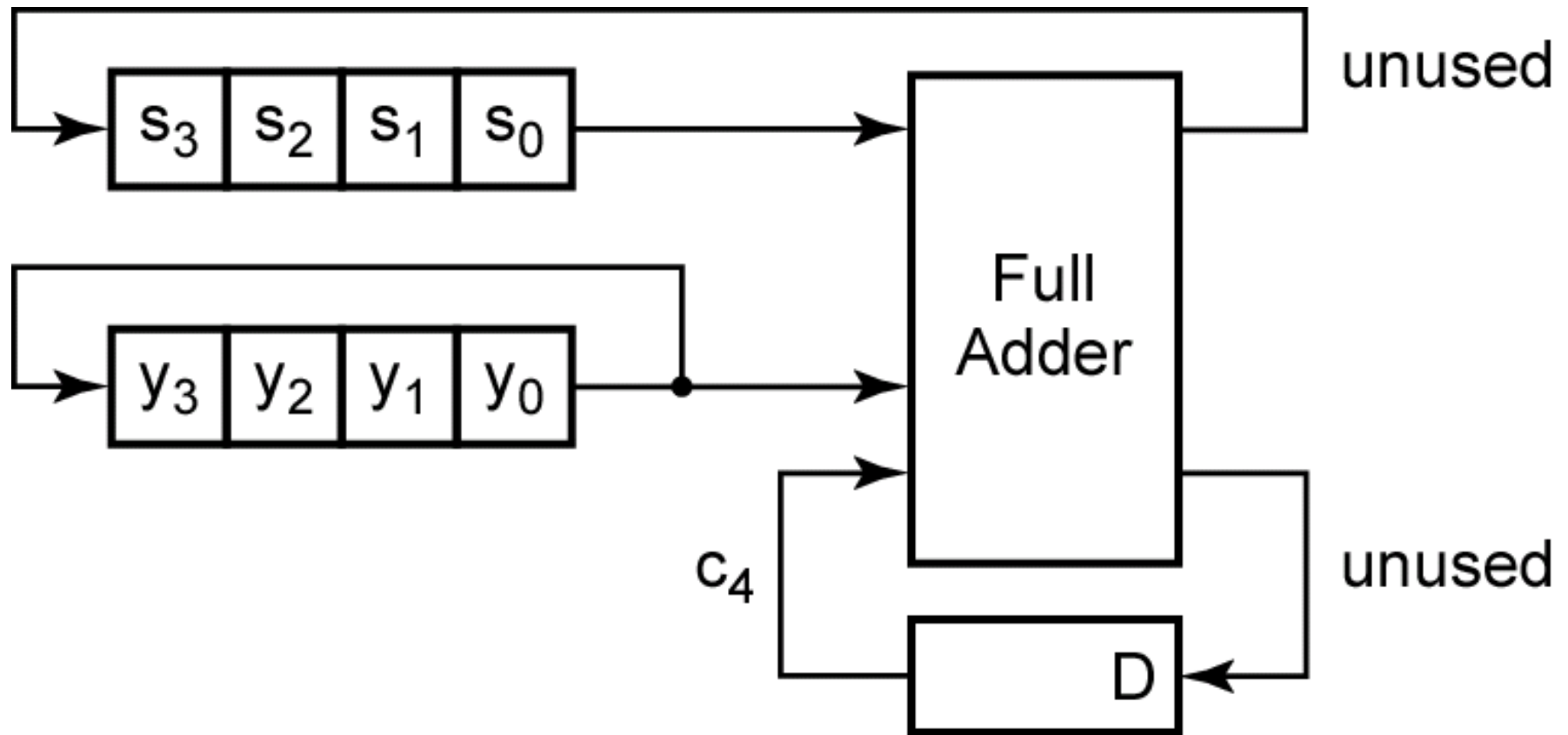


Figure 18-2cd:
Operation of
Serial Adder



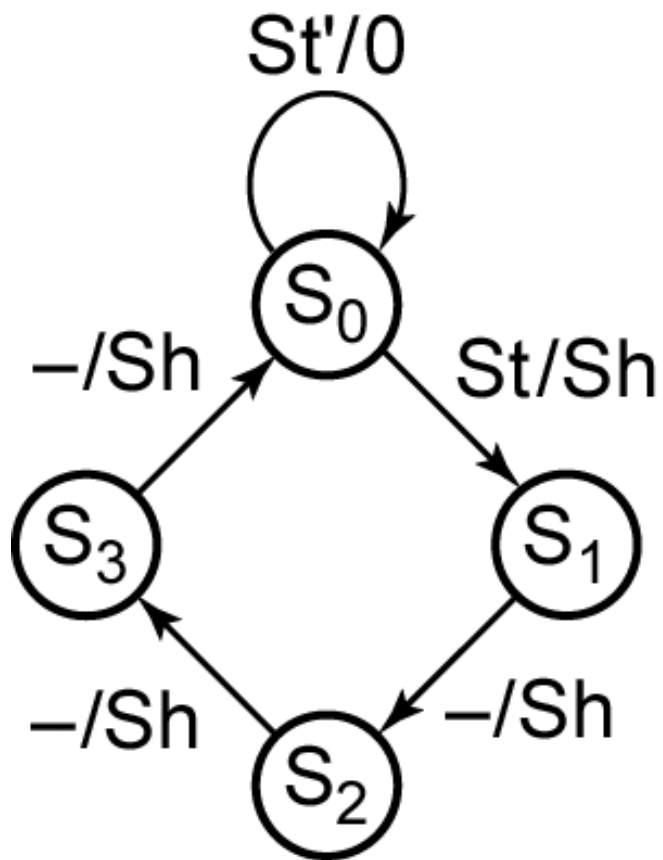


(e) At time t_4

Figure 18-2e:
Operation of
Serial Adder

Table 18-1 Operation of Serial Adder

	X	Y	C_i	S_i	C_i^+
t_0	0101	0111	0	0	1
t_1	0010	1011	1	0	1
t_2	0001	1101	1	1	1
t_3	1000	1110	1	1	0
t_4	1100	0111	0	(1)	(0)



	Next State		Sh	
	St = 0	1	0	1
S₀	S₀	S₁	0	1
S₁	S₂	S₂	1	1
S₂	S₃	S₃	1	1
S₃	S₀	S₀	1	1

Figure 18-3: State Graph for Serial Adder Control

	AB	A⁺B⁺	
		0	1
S₀	00	00	01
S₁	01	10	10
S₂	10	11	11
S₃	11	00	00

***Figure 18-4a:* Derivation of Control Circuit Equations**

		St	
		0	1
AB	00	0	0
	01	1	1
	11	0	0
	10	1	1

A^+

$$D_A = A'B + AB'$$

$$= A \oplus B$$

		St	
		0	1
AB	00	0	1
	01	0	0
	11	0	0
	10	1	1

B^+

$$D_B = St B' + AB'$$

		St	
		0	1
AB	00	0	1
	01	1	1
	11	1	1
	10	1	1

Sh

$$Sh = St + A + B$$

Figure 18-4b: Derivation of Control Circuit Equations

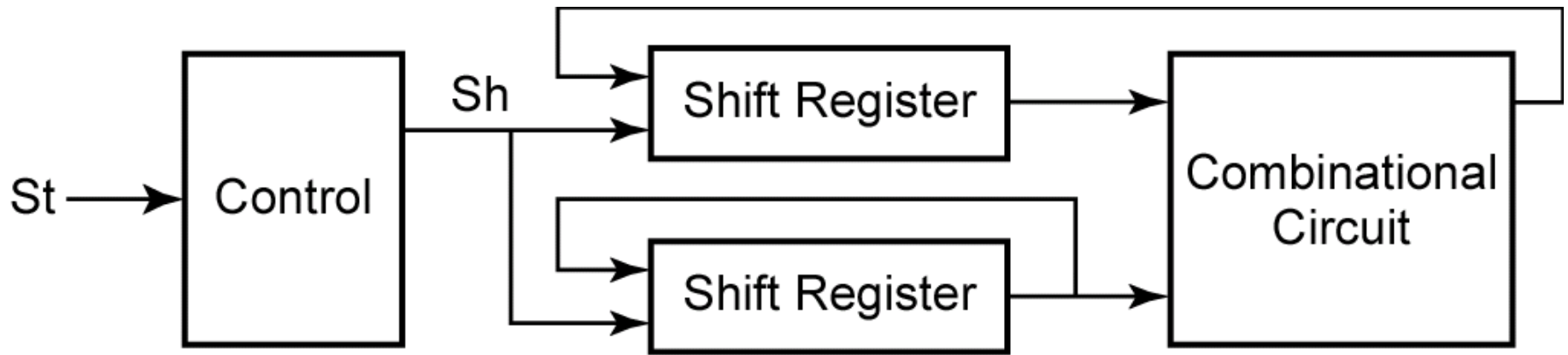
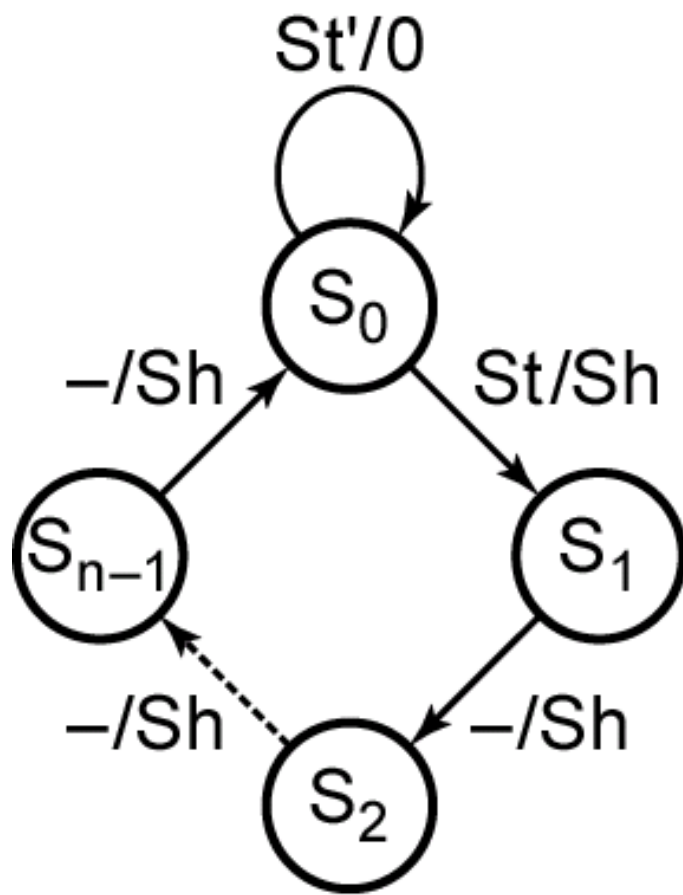


Figure 18-5: Typical Serial Processing Unit

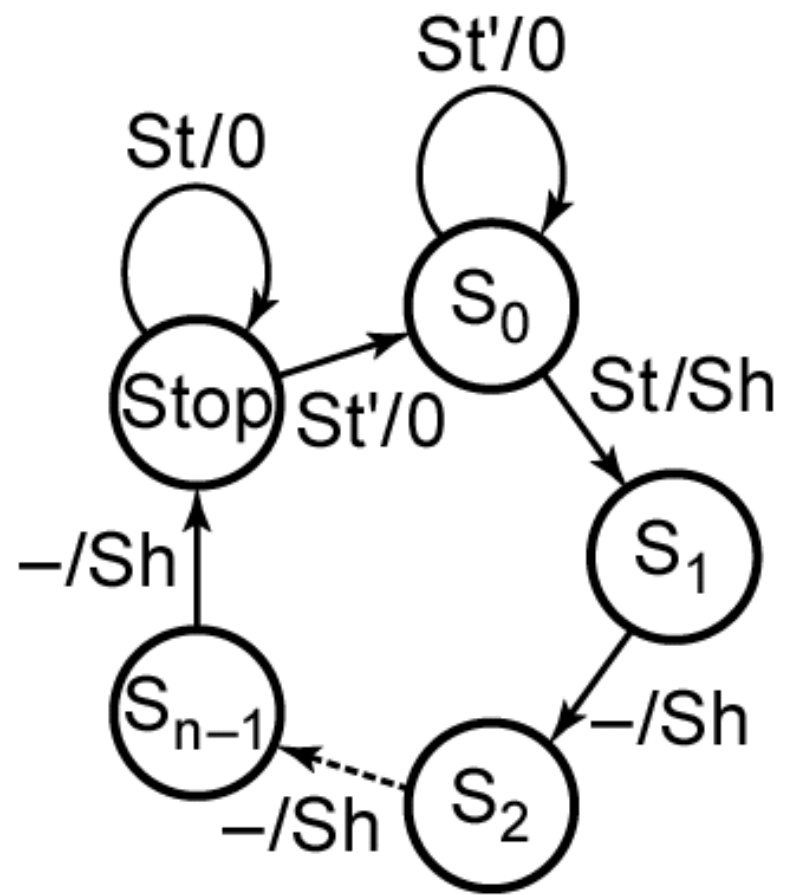
The output bits from the shift register are inputs to a combinational circuit.

The combinational circuit generates at least one output bit which is fed into the input of a shift register.

When the active clock edge occurs, this bit is stored in the first bit of the shift register at the same time the register bits are shifted to the right.



(a)



(b)

Figure 18-6: State Graphs for Serial Processing Unit

Design of Parallel Multiplier

Multiplication with partial products added in as soon as they are formed:

$$\begin{array}{rcl} \text{Multiplicand} & \longrightarrow & 1101 \quad (13) \\ \text{Multiplier} & \longrightarrow & \underline{1011} \quad (11) \\ & & 1101 \\ & \nearrow & 1101 \\ \text{Partial Products} & \left\{ \begin{array}{l} \longrightarrow \underline{100111} \\ \longrightarrow 0000 \\ \searrow \underline{100111} \end{array} \right. & \\ & & 1101 \\ \text{Product} & \longrightarrow & \underline{10001111} \quad (143) \end{array}$$

Section 18.2 (p. 598)

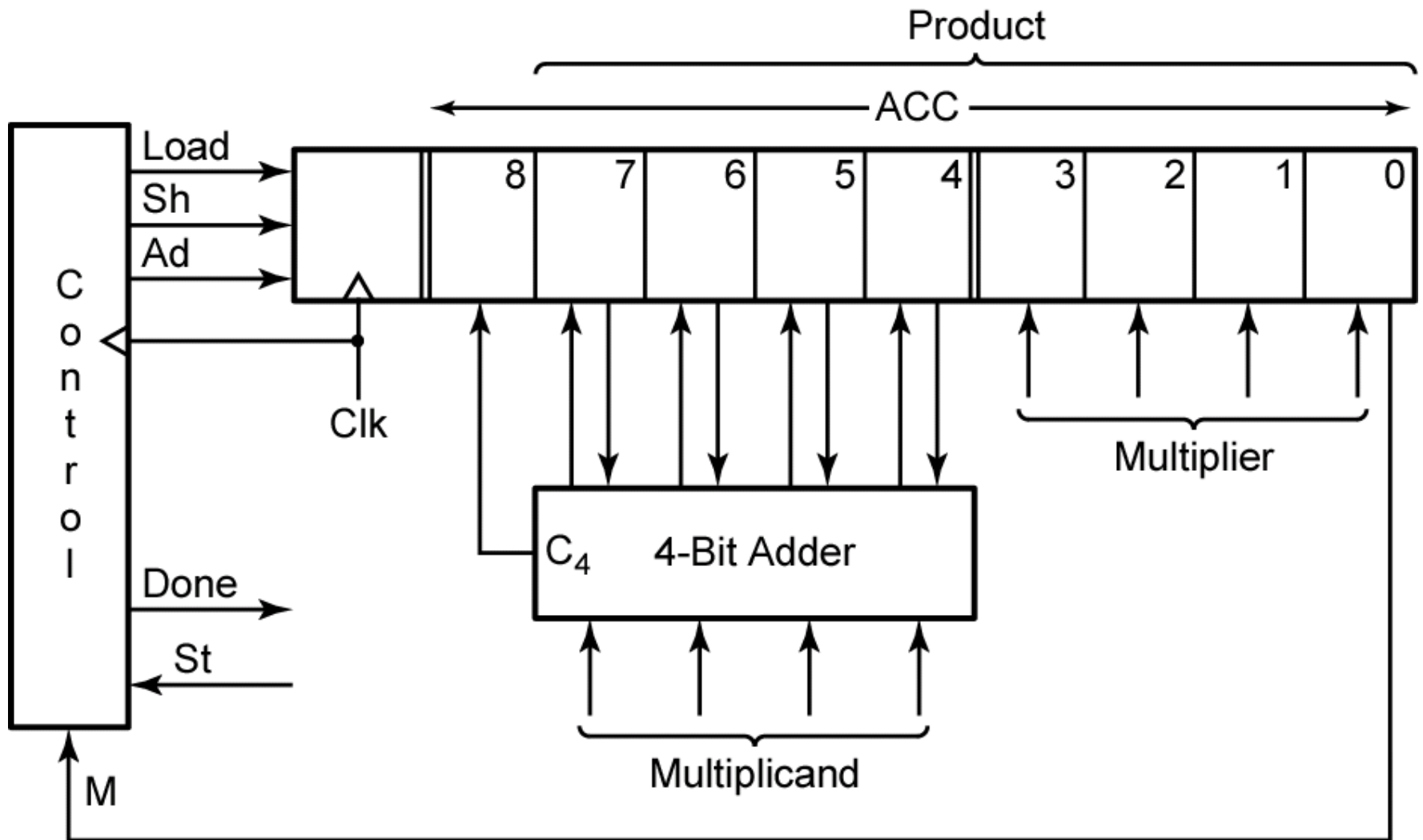



Figure 18-7: Block Diagram for Parallel Binary Multiplier

Parallel Binary Multiplication

initial contents of product register	0 0 0 0 0 1 0 1 1 $\leftarrow M$	(11)
(add multiplicand because $M = 1$)	1 1 0 1	(13)
after addition	0 1 1 0 1 1 0 1 1	
after shift	0 0 1 1 0 1 1 0 1 $\leftarrow M$	
(add multiplicand because $M = 1$)	1 1 0 1	
after addition	1 0 0 1 1 1 1 0 1	
after shift	0 1 0 0 1 1 1 1 0 $\leftarrow M$	
(skip addition because $M = 0$)		
after shift	0 0 1 0 0 1 1 1 1 $\leftarrow M$	
(add multiplicand because $M = 1$)	1 1 0 1	
after addition	1 0 0 0 1 1 1 1 1	
after shift (final answer)	0 1 0 0 0 1 1 1 1	(143)
dividing line between product and multiplier		

Section 18.2 (p. 600)

4-bit Multiplier

4-bit Multiplicand

8-bit Product

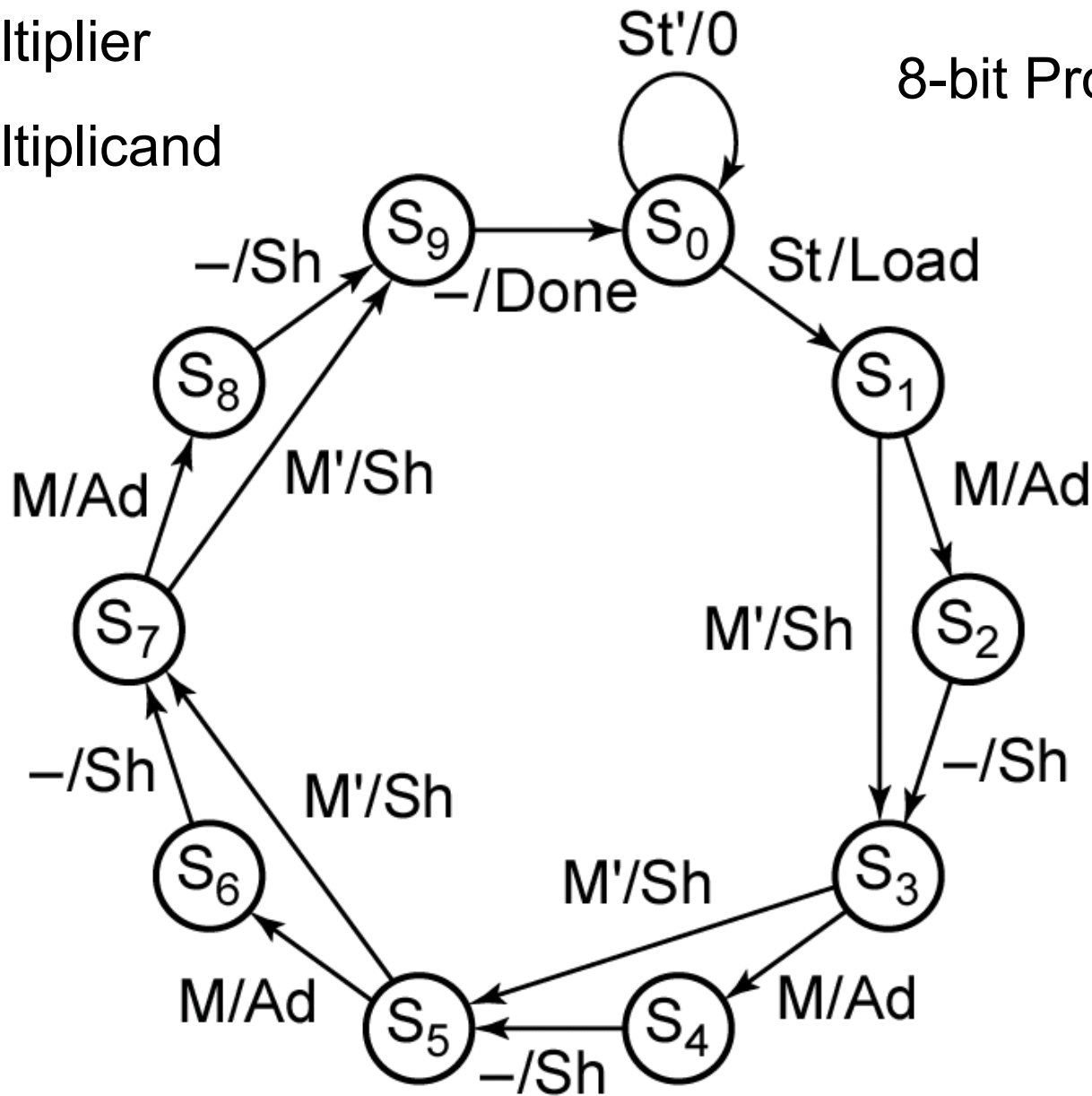
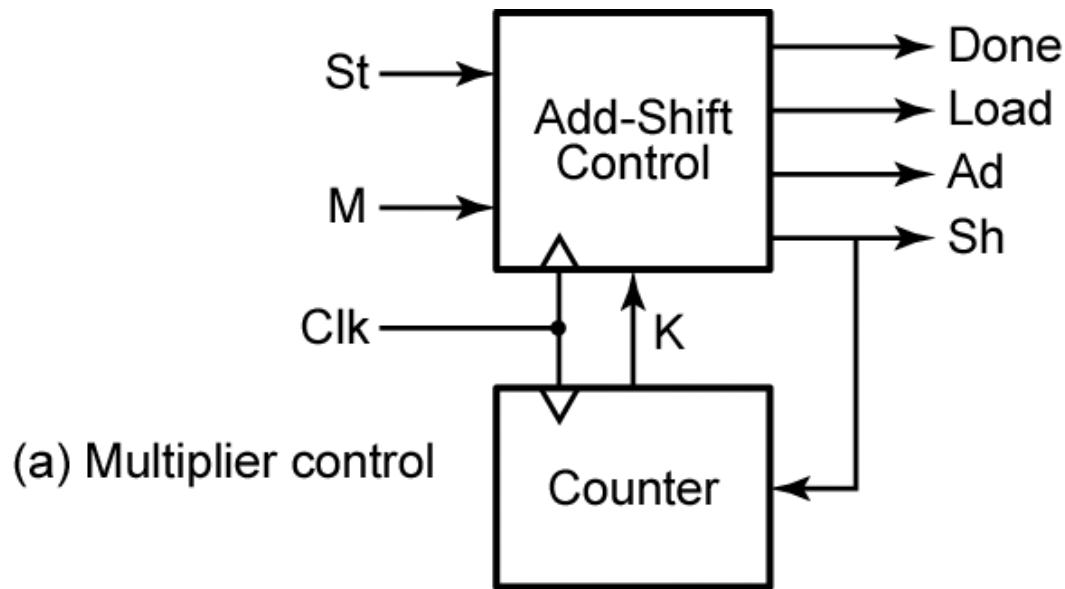
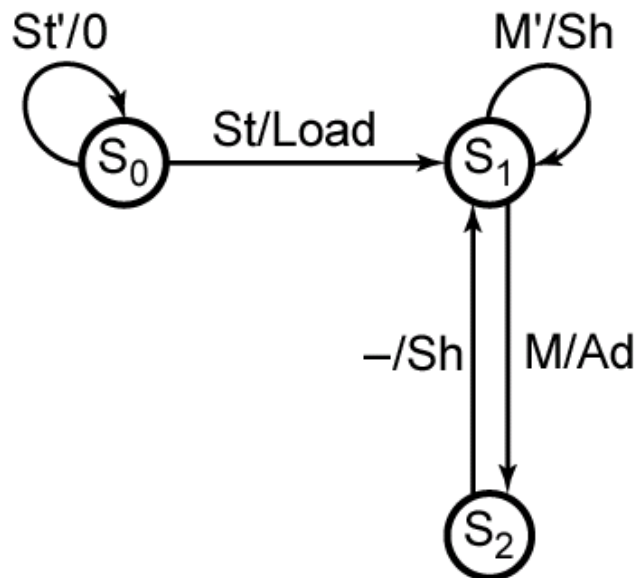


Figure 18-8: State Graph for Multiplier Control

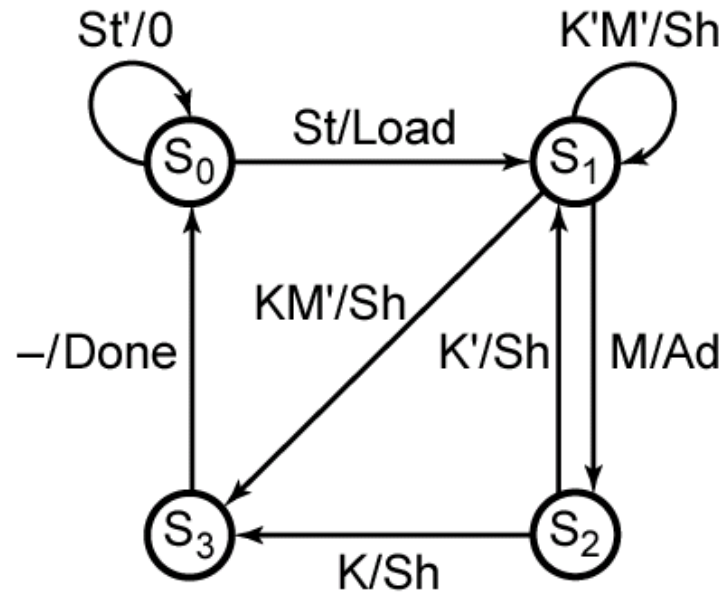


(a) Multiplier control

Figure 18-9



(b) State graph for add-shift control



(c) Final state graph for add-shift control

Table 18.2 Operation of a Multiplier Using a Counter

Time	State	Counter	Product Register	St	M	K	Load	Ad	Sh	Done
t_0	S_0	00	000000000	0	0	0	0	0	0	0
t_1	S_0	00	000000000	1	0	0	1	0	0	0
t_2	S_1	00	000001011	0	1	0	0	1	0	0
t_3	S_2	00	011011011	0	1	0	0	0	1	0
t_4	S_1	01	001101101	0	1	0	0	1	0	0
t_5	S_2	01	100111101	0	1	0	0	0	1	0
t_6	S_1	10	010011110	0	0	0	0	0	1	0
t_7	S_1	11	001001111	0	1	1	0	1	0	0
t_8	S_2	11	100011111	0	1	1	0	0	1	0
t_9	S_3	00	010001111	0	1	0	0	0	0	1

Design of Binary Divider

Example of division process:

			1010	quotient
divisor	1101	/	10000111	dividend
			<u>1101</u>	
			0111	
			<u>0000</u>	
			1111	
			<u>1101</u>	
			0101	
			<u>0000</u>	
			0101	remainder

(135 ÷ 13 = 10 with
a remainder of 5)

Section 18.3 (p. 602)

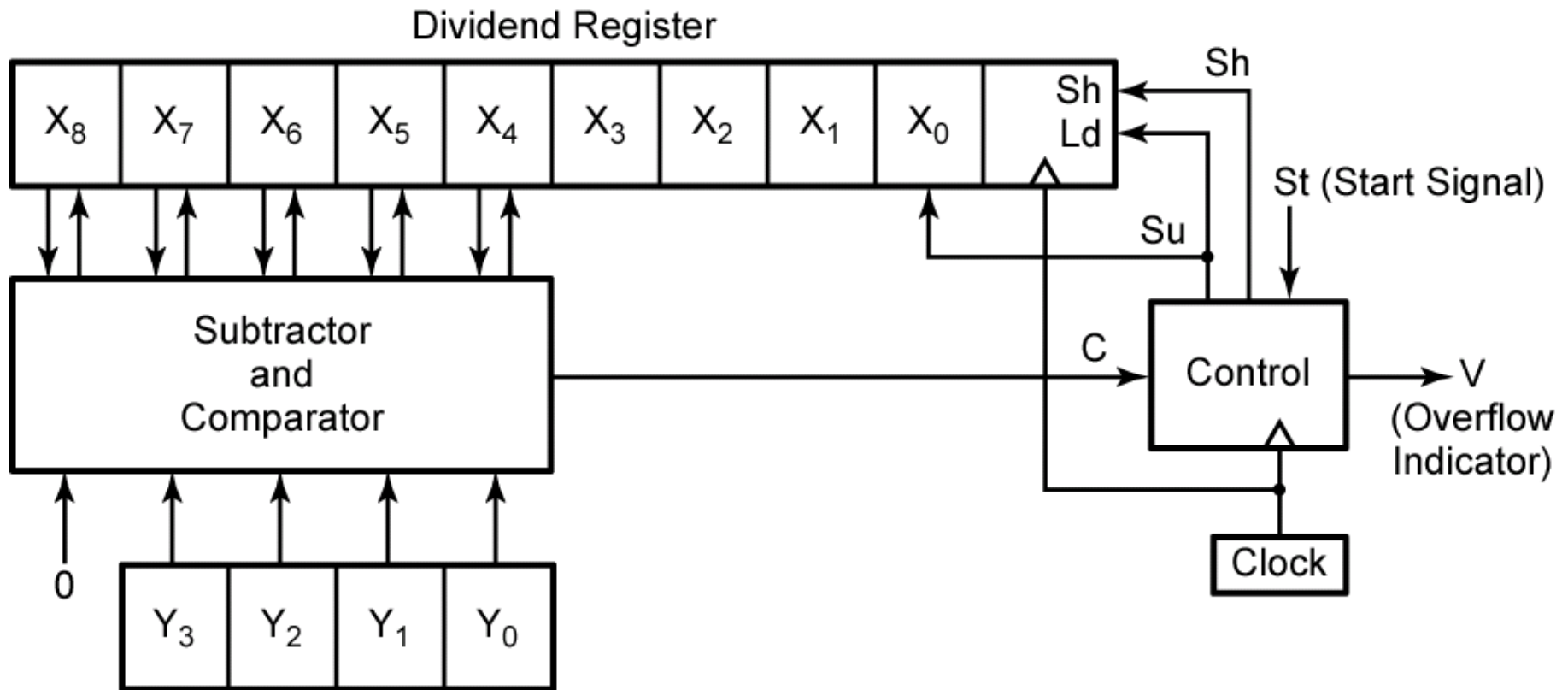
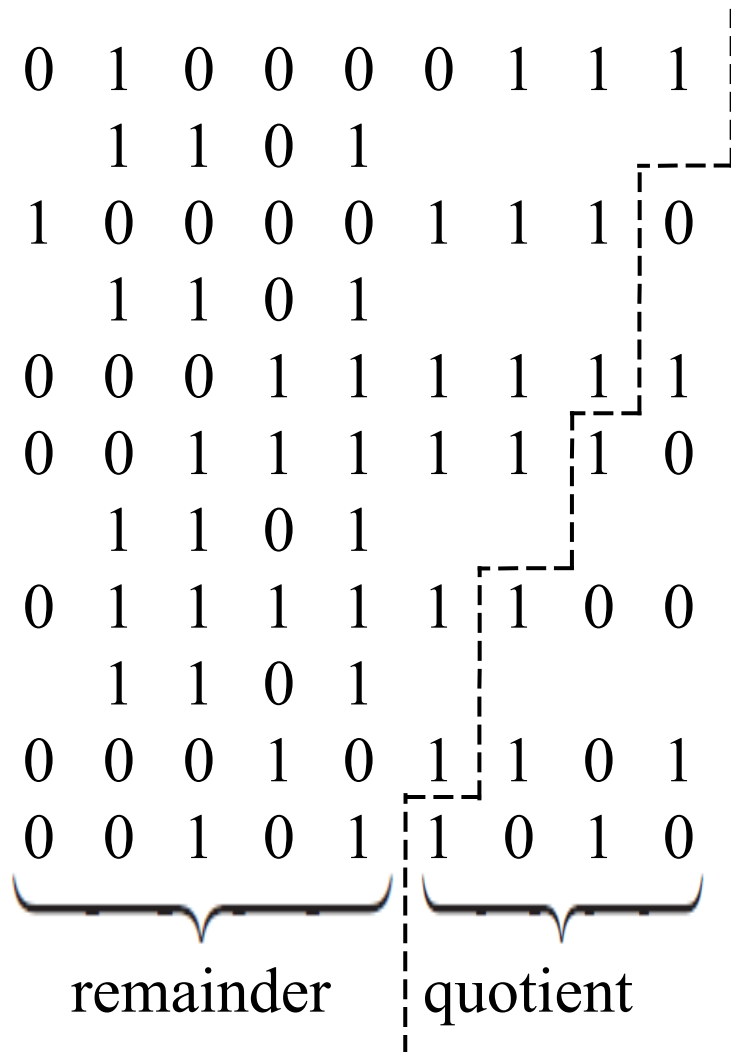


Figure 18-10: Block Diagram for Parallel Binary Divider



C = 0, Shift

C = 1, Subtract
Shift

C = 0, Shift

C = 1, Subtract
Shift

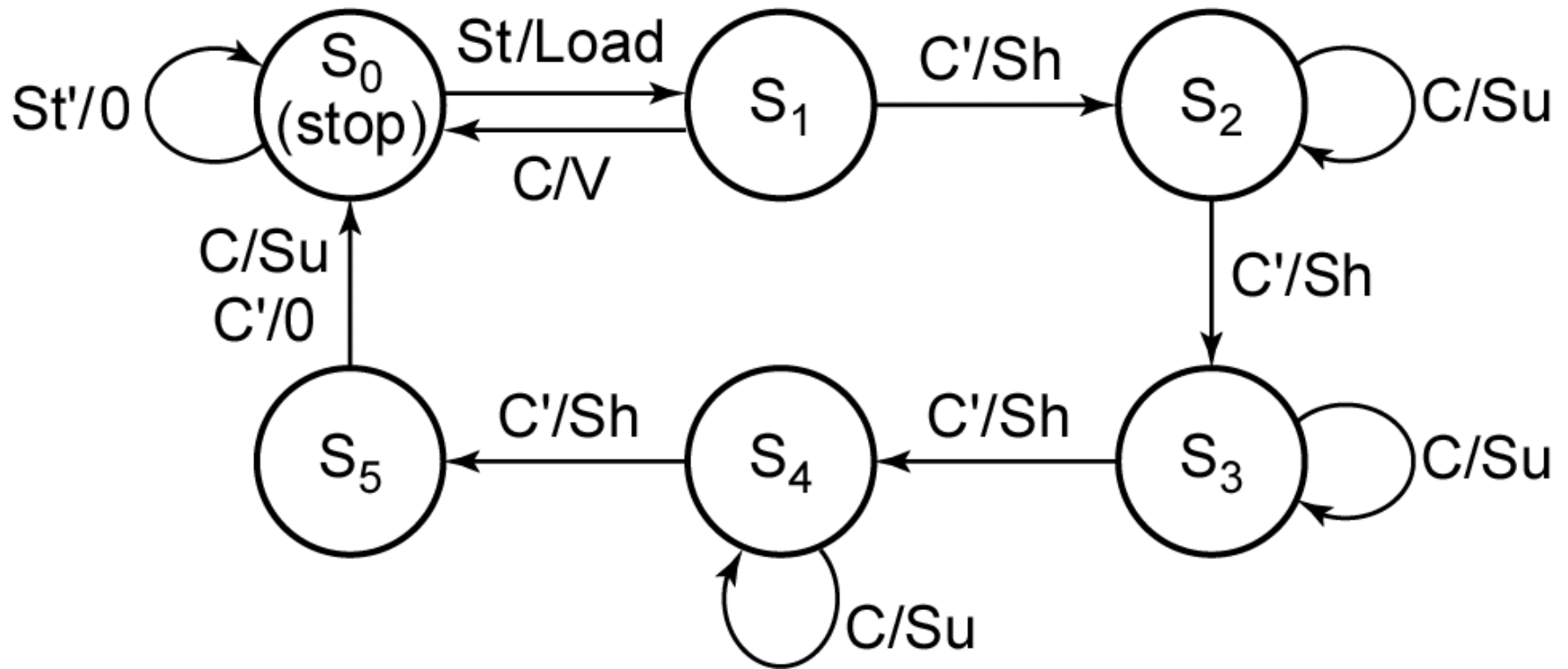
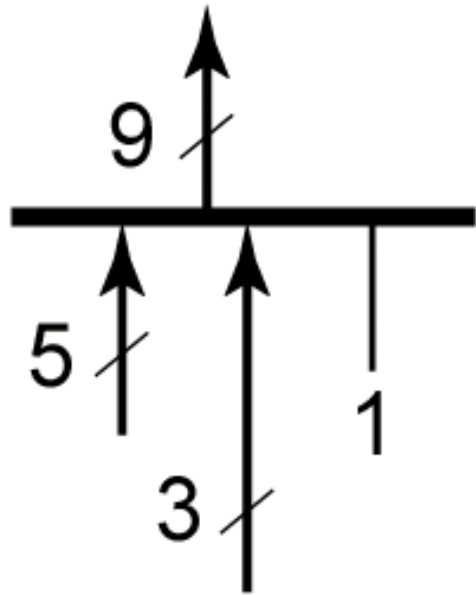
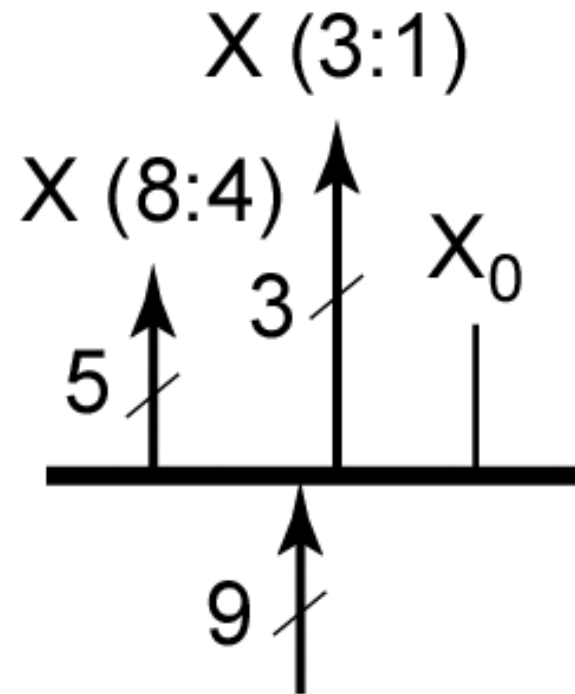


Figure 18-11: State Graph for Divider Control Circuit



Bus Merger



Bus Splitter

Section 18.3 (p. 606)

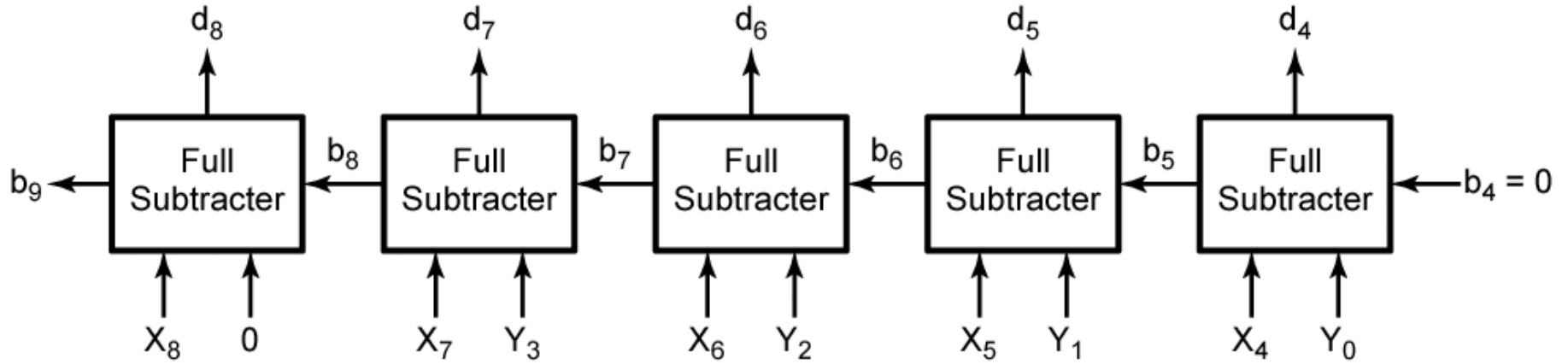


Figure 18-12: Logic Diagram for 5-Bit Subtractor

Figure 18-13:
Block Diagram for
Divider Using Bus
Notation

